3.3V CMOS 12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16271

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of – 40°C to + 85°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- V_{CC} = 2.7V to 3.6V, Extended Range
- V_{CC} = 2.5V ± 0.2V
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16271:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

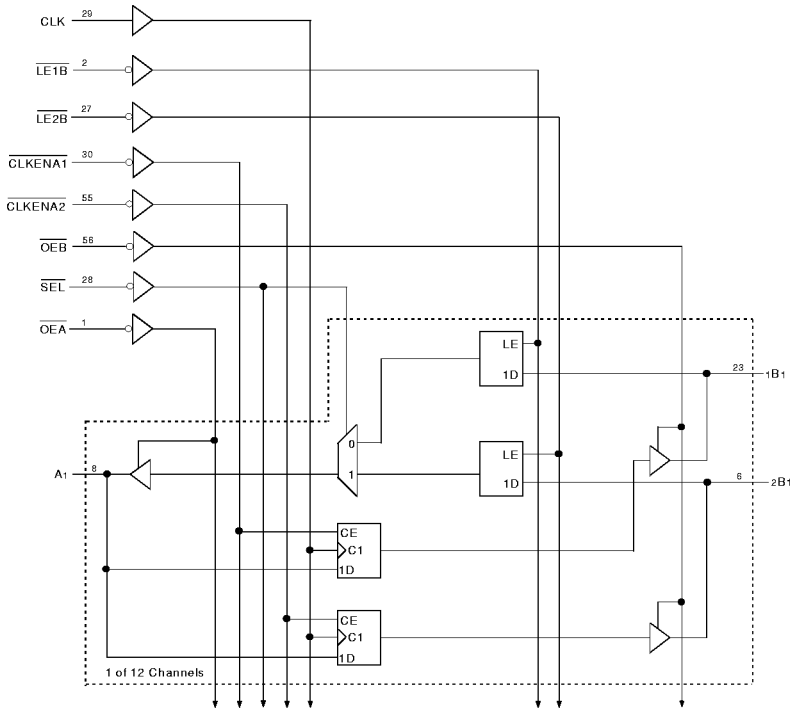
The ALVCH16271 is intended for applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the clock-enable ($\overline{CLKENA}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. Transparent latches in the B-to-A path allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable ($\overline{LE}$) inputs are low. The select ($\overline{SEL}$) line selects 1B or 2B data for the A inputs. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB}$).

The ALVCH16271 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

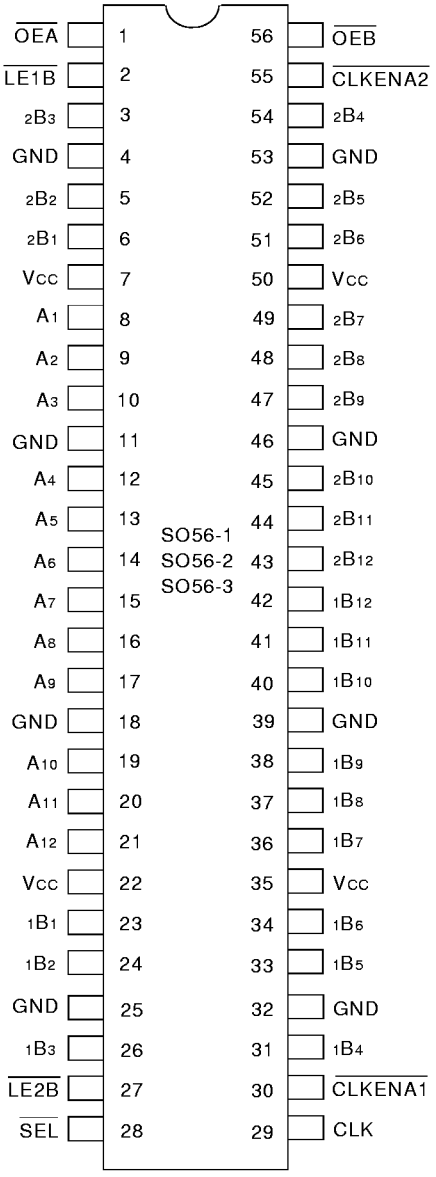
The ALVCH16271 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE **MARCH 1999**

PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

FUNCTION TABLES(1)

OUTPUT ENABLE

Inputs		Outputs	
$\overline{OEA}$	$\overline{OEB}$	Ax	1Bx, 2Bx
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB}$ = L)

Inputs				Outputs	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	Ax	1Bx	2Bx
H	H	X	X	1BO(2)	2BO(2)
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

B-TO-A STORAGE ($\overline{OEA}$ = L)

Inputs					Outputs
$\overline{LE1B}$	$\overline{LE2B}$	$\overline{SEL}$	1Bx	2Bx	Ax
H	H	X	X	X	AO(2)
H	H	X	X	X	AO(2)
L	X	H	L	X	L
L	X	H	H	X	H
X	L	L	X	L	L
X	L	L	X	H	H

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
2. Output level before the indicated steady-state input conditions were established.

PIN DESCRIPTION

Pin Names	I/O	Description
$A_{X(1:12)}$	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.[1]
$_1B_{X(1:12)}$	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory.[1]
$_2B_{X(1:12)}$	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory.[1]
CLK	I	Clock Input
$\overline{CLKENA1}$	I	Clock Enable Input for the A-1B Register. If $\overline{CLKENA1}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
$\overline{CLKENA2}$	I	Clock Enable Input for the A-2B Register. If $\overline{CLKENA2}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
$\overline{LE1B}$	I	Latch-Enable Input for the 1B-A Latch
$\overline{LE2B}$	I	Latch-Enable Input for the 2B-A Latch
$\overline{SEL}$	I	1B or 2B Port Selection. When HIGH, $\overline{SEL}$ enables data transfer from 1B Port to A Port. When LOW, $\overline{SEL}$ enables data transfer from 2B Port to A Port (Active LOW).
$\overline{OEA}$	I	Output Enable for A Port (Active LOW)
$\overline{OEB}$	I	Output Enable for B Port (Active LOW)

NOTE:
1. These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	9	pF
$C_{I/O}$	I/O Port Capacitance	V_{IN} = 0V	7	9	pF

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NOTE:
1. As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	± 10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND		—	—	750	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter(1)	Test Conditions		Min.	Typ.(2)	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 2.3V	V_I = 1.7V	– 45	—	—	µA
I_{BHL}			V_I = 0.7V	45	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

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NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V	Vcc = 3.3V ± 0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance Ax to xBx, outputs enabled	C_L = 0pF, f = 10Mhz	92	105	pF
C_{PD}	Power Dissipation Capacitance Ax to xBx, outputs disabled		61	76	pF
C_{PD}	Power Dissipation Capacitance xBx to Ax, outputs enabled		39	43	pF
C_{PD}	Power Dissipation Capacitance xBx to Ax, outputs disabled		11	13	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		130	—	130	—	130	—	Mhz
t_{PLH} t_{PHL}	Propagation Delay CLK to xBx	1	6.2	—	5	1	4.3	ns
t_{PLH} t_{PHL}	Propagation Delay xBx to Ax	1	5.3	—	4.7	1.4	4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$ to Ax	1	6	—	5.9	1.4	4.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{SEL}$ to Ax	1.1	6.4	—	6.2	1.3	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEB}$ to Ax or $\overline{OEA}$ to xBx	1	6	—	6.1	1	5.1	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEB}$ to Ax or $\overline{OEA}$ to xBx	1.4	5.4	—	4.6	1.7	4.2	ns
t_{SU}	Setup Time, Ax data before CLK↑	2.6		2.1		1.7		ns
t_{SU}	Setup Time, Bx data before $\overline{LE}$	1.7		1.5		1.3		ns
t_{SU}	Setup Time, $\overline{CLKEN}$ before CLK↑	1.6		1.3		1		ns
t_H	Hold Time, Ax data after CLK↑	0.6		0.6		0.7		ns
t_H	Hold Time, Bx data after $\overline{LE}$	0.9		0.9		1.1		ns
t_H	Hold Time, $\overline{CLKEN}$ after CLK↑	1		0.9		0.9		ns
t_W	Pulse Width, CLK HIGH or LOW	3.3		3.3		3.3		ns
t_W	Pulse Width, $\overline{LExB}$ LOW	3.3		3.3		3.3		ns
$t_{SK(o)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. $T_A = -40°C$ to $+85°C$.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V±0.3V	$V_{CC}^{(1)}$= 2.7V	$V_{CC}^{(2)}$= 2.5V±0.2V	Unit
V_{LOAD}	6	6	2 x Vcc	V
V_{IH}	2.7	2.7	Vcc	V
V_T	1.5	1.5	Vcc / 2	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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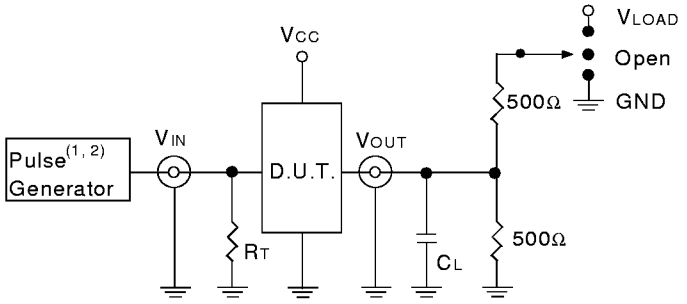
TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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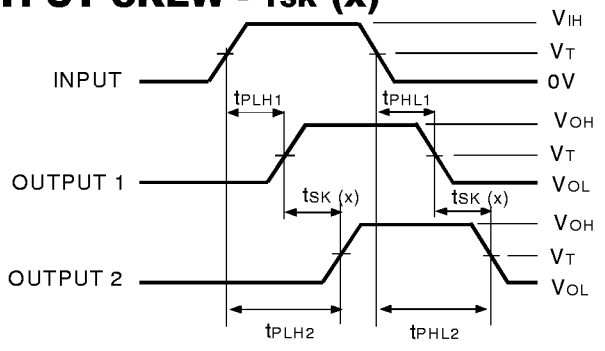
OUTPUT SKEW - t_{SK} (x)



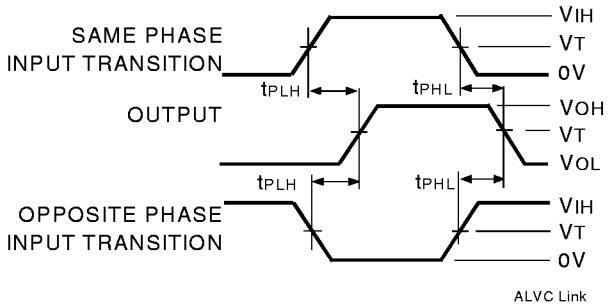
$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

ALVC Link

NOTES:

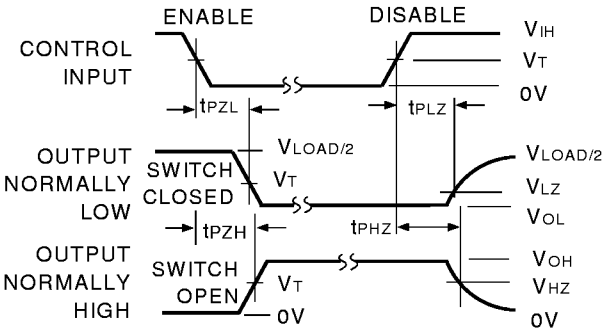
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

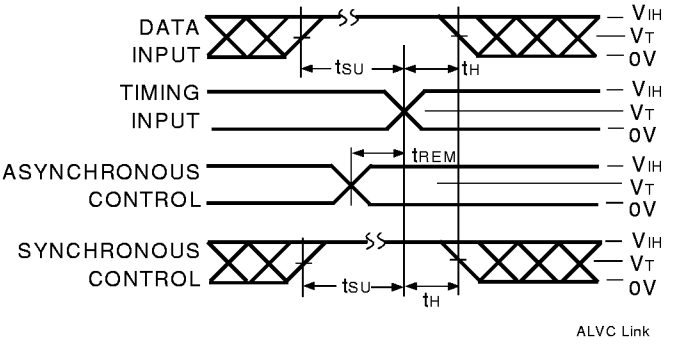


ALVC Link

NOTE:

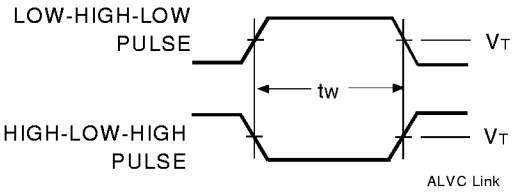
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



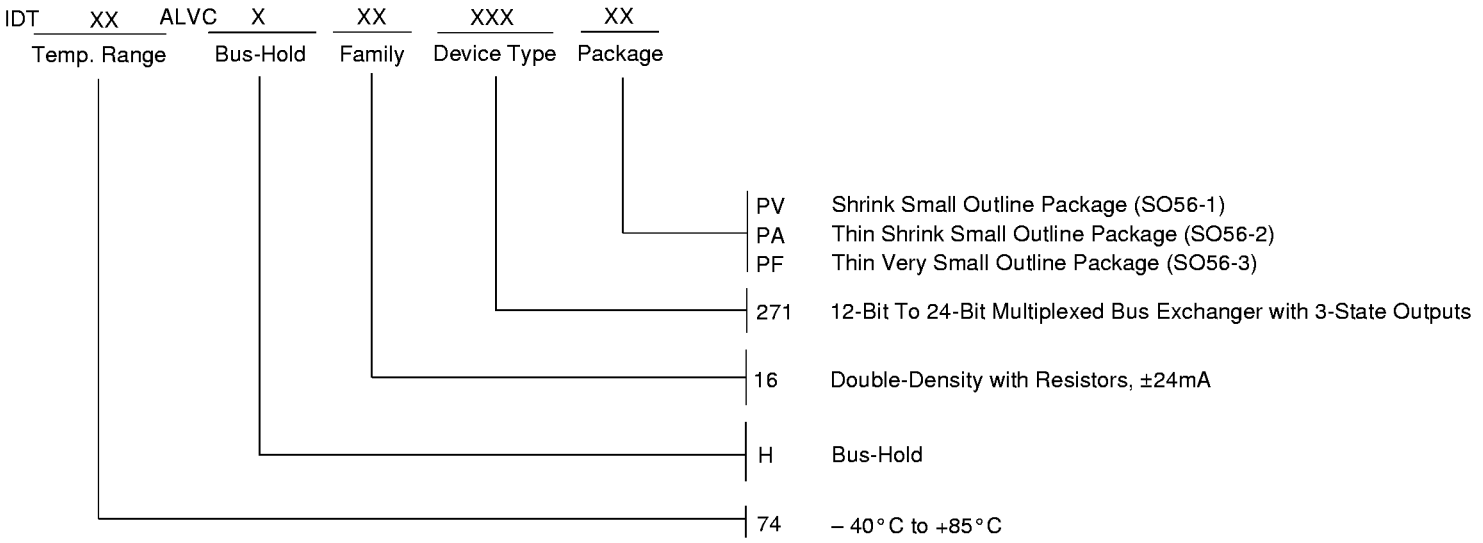
ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION



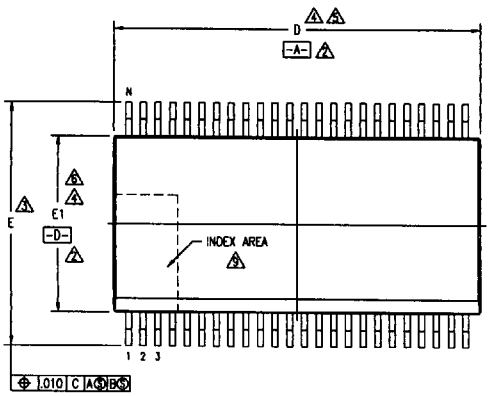
CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

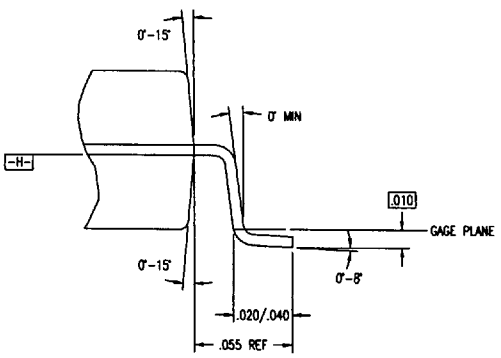
for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.

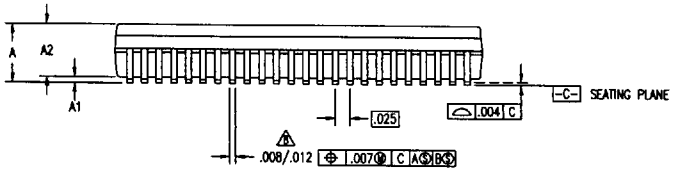
SSOP

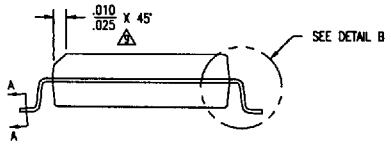
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

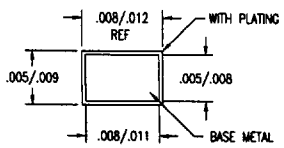




DETAIL B







SECTION A-A

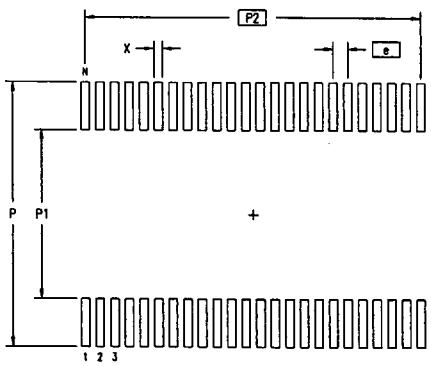
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
DRAWN AA	08/15/90		
CHECKED		SIZE C	DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING	

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1			DWG #		S056-1		
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

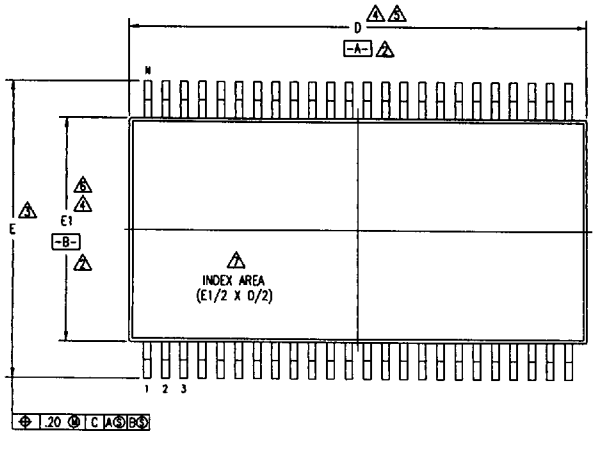
10 ALL DIMENSIONS ARE IN INCHES

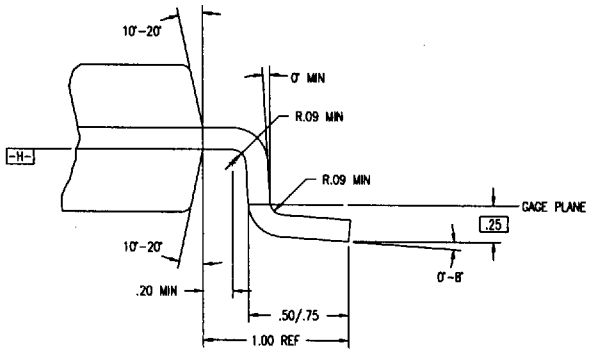
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARATION AA & AB

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL XX± XXX± XXXX±	ANGULAR ±	2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
APPROVALS	DATE	TITLE PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH
DRAWN AA	05/15/90	
CHECKED		SIZE C DRAWING No. PSC-4029 REV 02
		DO NOT SCALE DRAWING

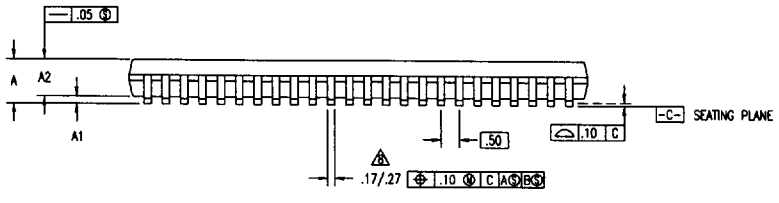
TSSOP

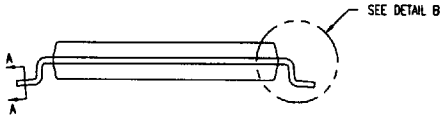
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
25490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

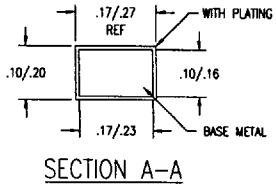




DETAIL B







SECTION A-A

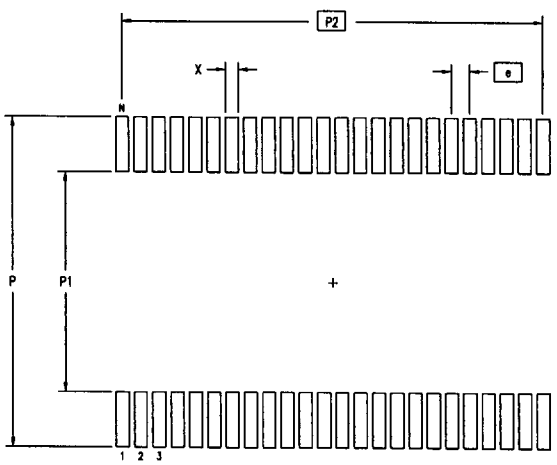
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL	ANGULAR		
XX±	±		
XXX±			
XXXX±			
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN dd	01/15/93		
CHECKED		SIZE C	DRAWING No. PSC-4039 REV 03
		DO NOT SCALE DRAWING	

TSSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

DWG #			S048-2		DWG #			S056-2	
SYMBOL	JEDEC VARIATION ED			NOTE	JEDEC VARIATION EE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.10		–	–	1.10	
A1	.05	–	.15		.05	–	.15	
A2	.85	1.00	1.05		.85	1.00	1.05	
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6
N	48				56			

LAND PATTERN DIMENSIONS



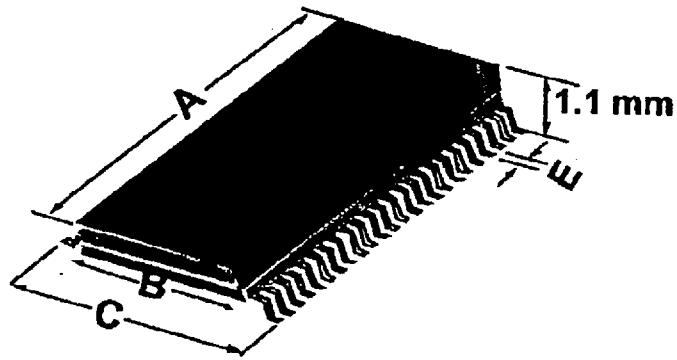
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50 BSC		13.50 BSC	
X	.30	.40	.30	.40
e	.50 BSC		.50 BSC	
N	48		56	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-
4. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
6. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
7. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION ED & EE

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL ANGULAR		2975 Stender Way, Santa Clara, CA 95054
XX± ±		PHONE: (408) 727-6116
XXX±		FAX: (408) 492-8674 TWX: 910-338-2070
XXXX±		
APPROVALS	DATE	TITLE PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN AA	01/13/93	
CHECKED		SIZE C DRAWING No. PSC-4039 REV 03
		DO NOT SCALE DRAWING

TVSOP
The Most Compact Double Density Package



TVSOP Package	Typical Dimensions (in mm)				Area (mm2)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50

Double Density Packaging

48-Pin

16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²

9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin

18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²

14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²

11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm^2)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0