



3.3V CMOS 18-BIT REGISTERED BUS TRANS- CEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16524

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16524:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

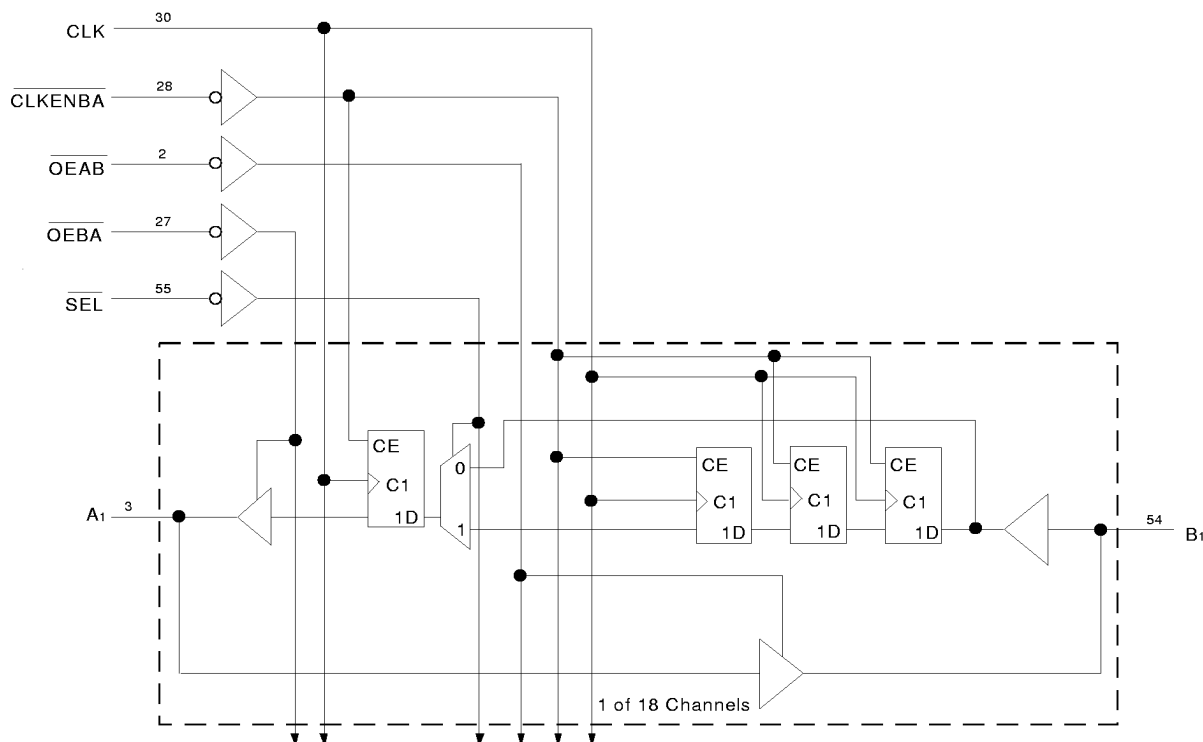
DESCRIPTION:

This 18-bit registered bus transceiver is built using advanced dual metal CMOS technology. Data flow in each direction is controlled by output-enable (OEAB and OEBA) and clock-enable (CLKENBA) inputs. For the A-to-B data flow, the data flows through a single buffer. The B-to-A data can flow through a four-stage pipeline register path, or through a single register path, depending on the state of the select ($\overline{\text{SEL}}$) input. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input, provided that the appropriate $\overline{\text{CLKENBA}}$ input is low. The B-to-A data transfer is synchronized with CLK.

The ALVCH16524 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16524 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

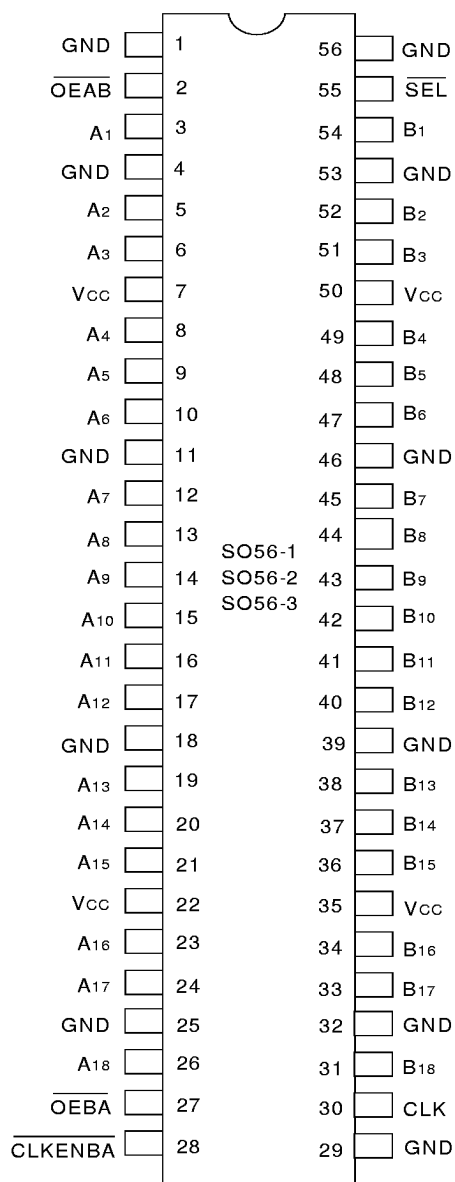
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

APRIL 1999

PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	− 0.5 to + 4.6	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	− 0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	− 65 to + 150	°C
I _{OUT}	DC Output Current	− 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	− 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
CLK	Clock Input
CLKENBA	Clock Enable for the CLK (Active LOW)
OEAB	Output Enable for the B port (Active LOW)
OEBA	Output Enable for the A port (Active LOW)
SEL	Select pin for pipelined ($\overline{SEL}$ = 0)/non-pipelined mode ($\overline{SEL}$ = 1) in the B-to-A direction (Active LOW)
Ax	A-to-B Data Inputs or B-to-A 3-State outputs ⁽¹⁾
Bx	B-to-A Data Inputs or A-to-B 3-State outputs ⁽¹⁾

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES (1)

A-TO-B STORAGE ($\overline{\text{CLKENBA}} = \text{X}$, $\overline{\text{OEBA}} = \text{H}$)				
Inputs				Output
$\overline{\text{OEAB}}$	CLK	$\overline{\text{SEL}}$	Ax	Bx
L	X	X	L	L
L	X	X	H	H
H	X	X	X	Z

B-TO-A STORAGE ($\overline{\text{OEBA}} = \text{L}$, $\overline{\text{OEAB}} = \text{H}$)				
Inputs				Output
$\overline{\text{CLKENBA}}$	CLK	$\overline{\text{SEL}}$	Bx	Ax
H	X	X	X	A0 ⁽²⁾
L	↑	H	L	L
L	↑	H	H	H
L	↑	L	L	L ⁽³⁾
L	↑	L	H	H ⁽³⁾

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = Floating Output
↑ = LOW-to-HIGH Transition
- Output level before the indicated steady-state input conditions were established.
- Four positive CLK edges are needed to propagate data from B to A when $\overline{\text{SEL}}$ is low.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

NOTE:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.

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BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	- 75	—	—	μ A
			V _I = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	- 45	—	—	μ A
			V _I = 0.7V	45	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	$\pm$ 500	μ A

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = - 0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = - 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = - 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = - 24mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

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NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Vcc = 2.5V $\pm$ 0.2V	Vcc = 3.3V $\pm$ 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	—	160	pF
CPD	Power Dissipation Capacitance Outputs disabled		—	160	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	Vcc = 2.5V $\pm$ 0.2V		Vcc = 2.7V		Vcc = 3.3V $\pm$ 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fMAX		120	—	125	—	150	—	MHz
tPLH tPHL	Propagation Delay Ax to Bx	1	3.9	—	3.8	1	3.2	ns
tPLH tPHL	Propagation Delay CLK to Ax	1	6.1	—	6.2	1	5.2	ns
tpZH tpZL	Output Enable Time $\overline{\text{OEAB}}$ to Bx or $\overline{\text{OEBA}}$ to Ax	1	6.1	—	6.1	1	5.1	ns
tPHZ tPLZ	Output Disable Time $\overline{\text{OEAB}}$ to Bx or $\overline{\text{OEBA}}$ to Ax	1	6.3	—	5.4	1	4.9	ns
tw	Pulse Duration, CLK HIGH or LOW	3.2	—	3.2	—	3	—	ns
tsu	Setup Time, Bx data before CLK $\uparrow$	1.5	—	1.2	—	1.1	—	ns
tsu	Setup Time, $\overline{\text{SEL}}$ before CLK $\uparrow$	2.7	—	2.4	—	2.1	—	ns
tsu	Setup Time, $\overline{\text{CLKENBA}}$ before CLK $\uparrow$	2.7	—	2.6	—	2	—	ns
tH	Hold Time, Bx data after CLK $\uparrow$	1	—	0.6	—	1.2	—	ns
tH	Hold Time, $\overline{\text{SEL}}$ after CLK $\uparrow$	0.5	—	0.2	—	0.8	—	ns
tH	Hold Time, $\overline{\text{CLKENBA}}$ after CLK $\uparrow$	0.1	—	0.1	—	0.3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
2. Skew between any two outputs of the same package and switching in the same direction.

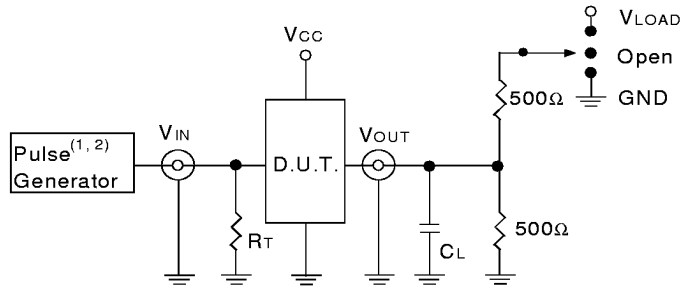
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

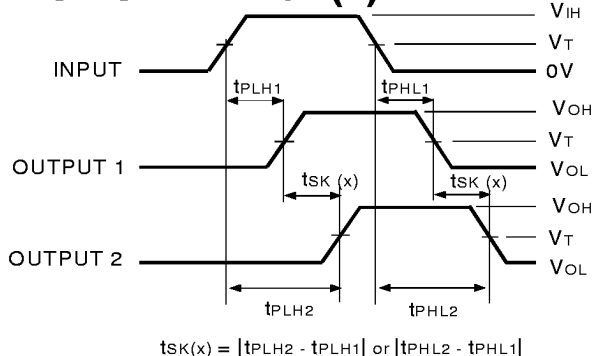
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

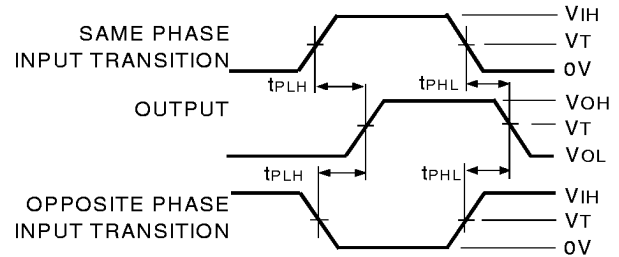


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NOTES:

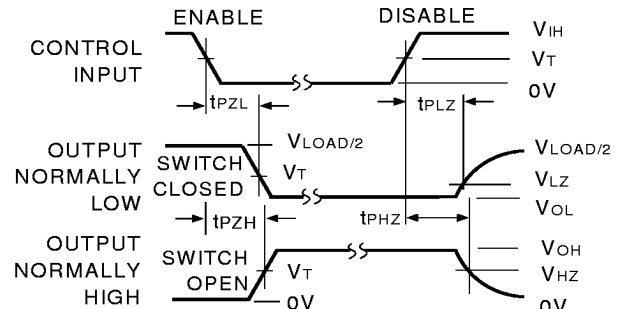
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

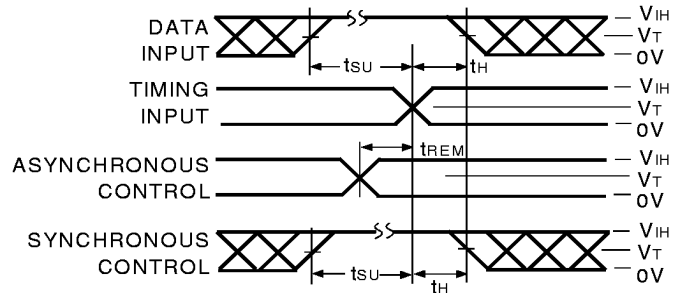


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NOTE:

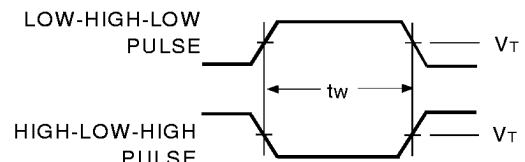
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
						524	18-Bit Registered Bus Transceiver with 3-State Outputs
						16	Double-Density with Resistors, $\pm 24\text{mA}$
						H	Bus-Hold
						74	-40 °C to +85 °C



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

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