



3.3V CMOS 10-BIT FLIP-FLOP WITH DUAL OUTPUTS, 3-STATE OUTPUTS, AND BUS-HOLD

IDT74ALVCH16820

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16820:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

DESCRIPTION:

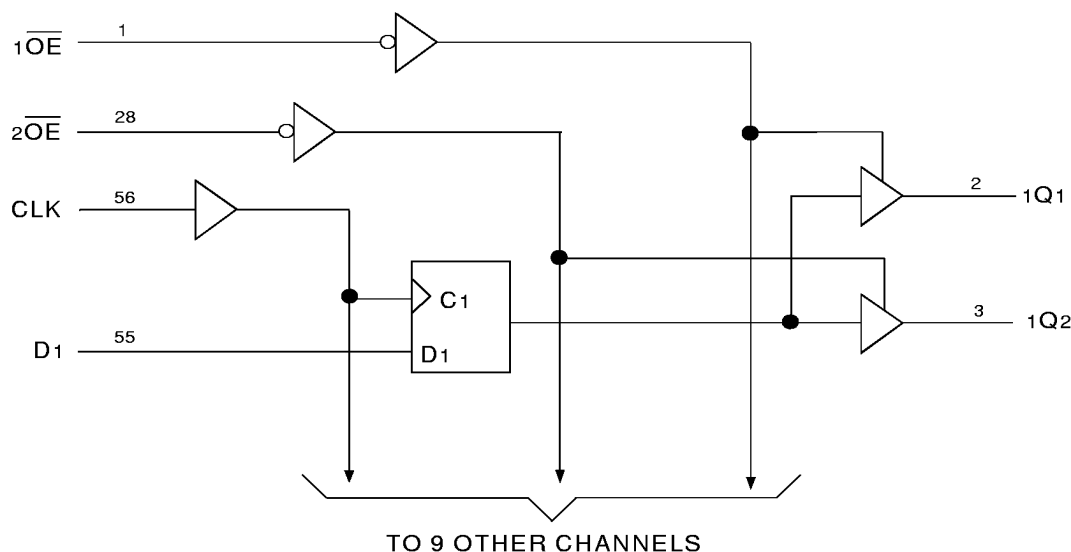
This 10-bit flip-flop is built using advanced dual metal CMOS technology. The flip-flops of the ALVCH16820 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs.

A buffered output-enable ($\overline{\text{OE}}$) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface or pullup components. $\overline{\text{OE}}$ input does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The ALVCH16820 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16820 has “bus-hold” which retains the inputs’ last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

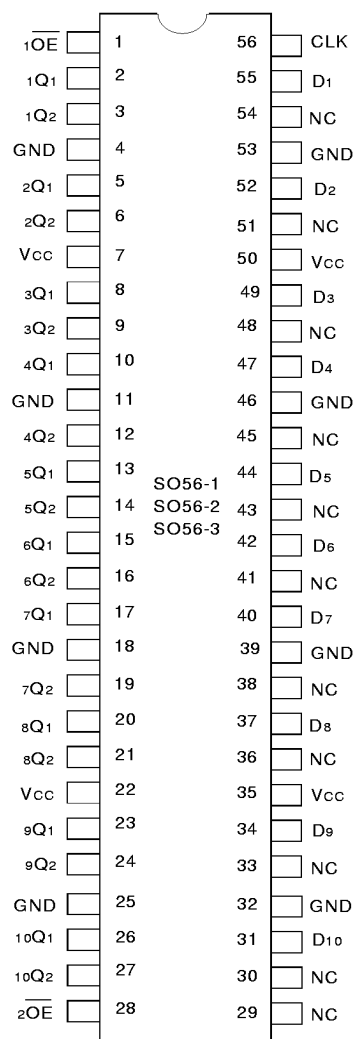
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

APRIL 1999

PIN CONFIGURATION

SSOP/TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
Dx	Data Inputs ⁽¹⁾
CLK	Clock Input
xQx	3-State Outputs
$\overline{xOE}$	3-State Output Enable Inputs
NC	No Internal Connection

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (each flip-flop) (1)

Inputs			Output
$\overline{xOE}$	CLK	Dx	xQx
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
Q₀ = Indicates the previous state

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
I_{OLZ}			$V_O = \text{GND}$	—	—	± 10	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

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NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	$V_{CC} = 3.0\text{V}$	$V_I = 2.0\text{V}$	-75	—	—	μA
I_{BHL}			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	μA
I_{BHL}			$V_I = 0.7\text{V}$	45	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = - 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

NOTE:

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1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per flip-flop Outputs enabled	CL = 0pF, f = 10Mhz	60	63	pF
CPD	Power Dissipation Capacitance per flip-flop Outputs disabled		38	46	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fMAX		150	—	150	—	150	—	MHz
tPLH tPHL	Propagation Delay, CLK to xQx	1	5.9	—	5.5	1	4.8	ns
tPZH tPZL	Output Enable Time, xOE to xQx	1	6.4	—	6.1	1	5	ns
tPHZ tPLZ	Output Disable Time, xOE to xQx	1	5.7	—	5	1	4.5	ns
tw	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tsu	Set-up Time, HIGH or LOW, data before CLK↑	1.7	—	1.8	—	1.4	—	ns
tH	Hold Time, HIGH or LOW, data after CLK↑	1.1	—	1.1	—	1	—	ns
tsk(O)	Output Skew ⁽²⁾	—	500	—	500	—	500	ps

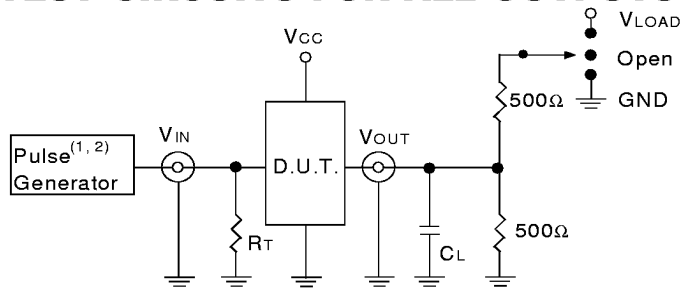
NOTES:

1. See test circuits and waveforms. TA = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS:**TEST CONDITIONS**

Symbol	Vcc(1) = 3.3V±0.3V	Vcc(1) = 2.7V	Vcc(2) = 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{cc}	V
V _{IH}	2.7	2.7	V _{cc}	V
V _T	1.5	1.5	V _{cc} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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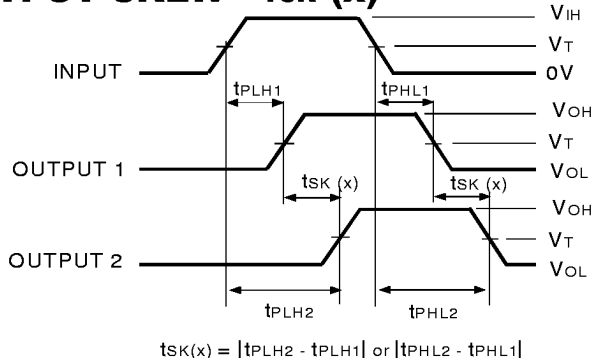
TEST CIRCUITS FOR ALL OUTPUTS**DEFINITIONS:**C_L = Load capacitance: includes jig and probe capacitance.R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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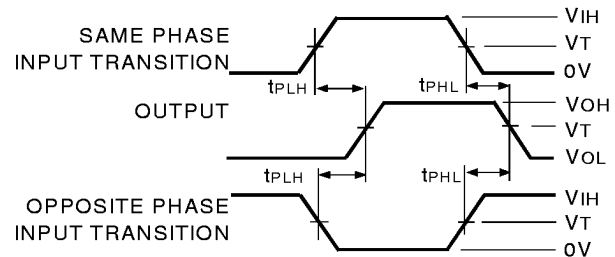
OUTPUT SKEW - t_{SK} (x)

$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

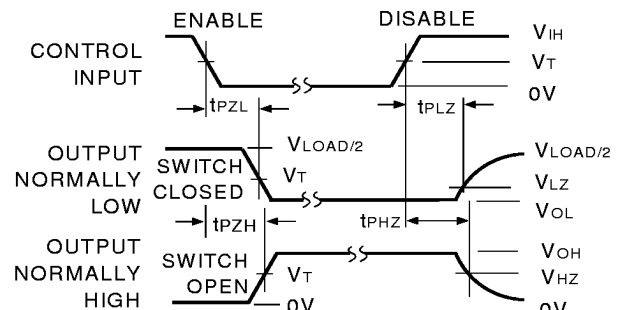
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NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY

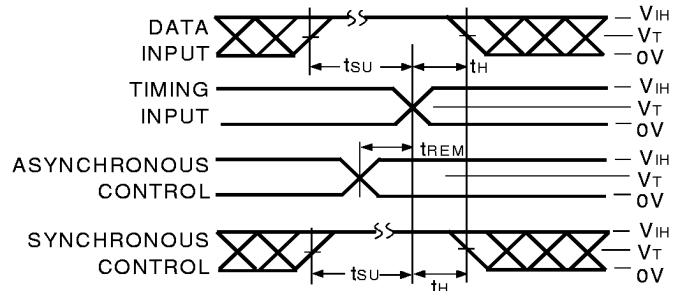
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ENABLE AND DISABLE TIMES

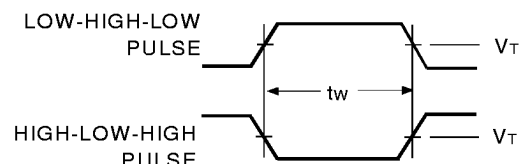
ALVC Link

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES

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PULSE WIDTH

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ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
Temp. Range	Bus-Hold	Family	Device Type	Package			
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
				820			10-Bit Flip Flop with Dual Outputs, 3-State Outputs
			16				Double-Density with Resistors, $\pm 24\text{mA}$
		H					Bus-Hold
					74		-40°C to $+85^{\circ}\text{C}$



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