



FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT162501AT/CT/ET

FEATURES:

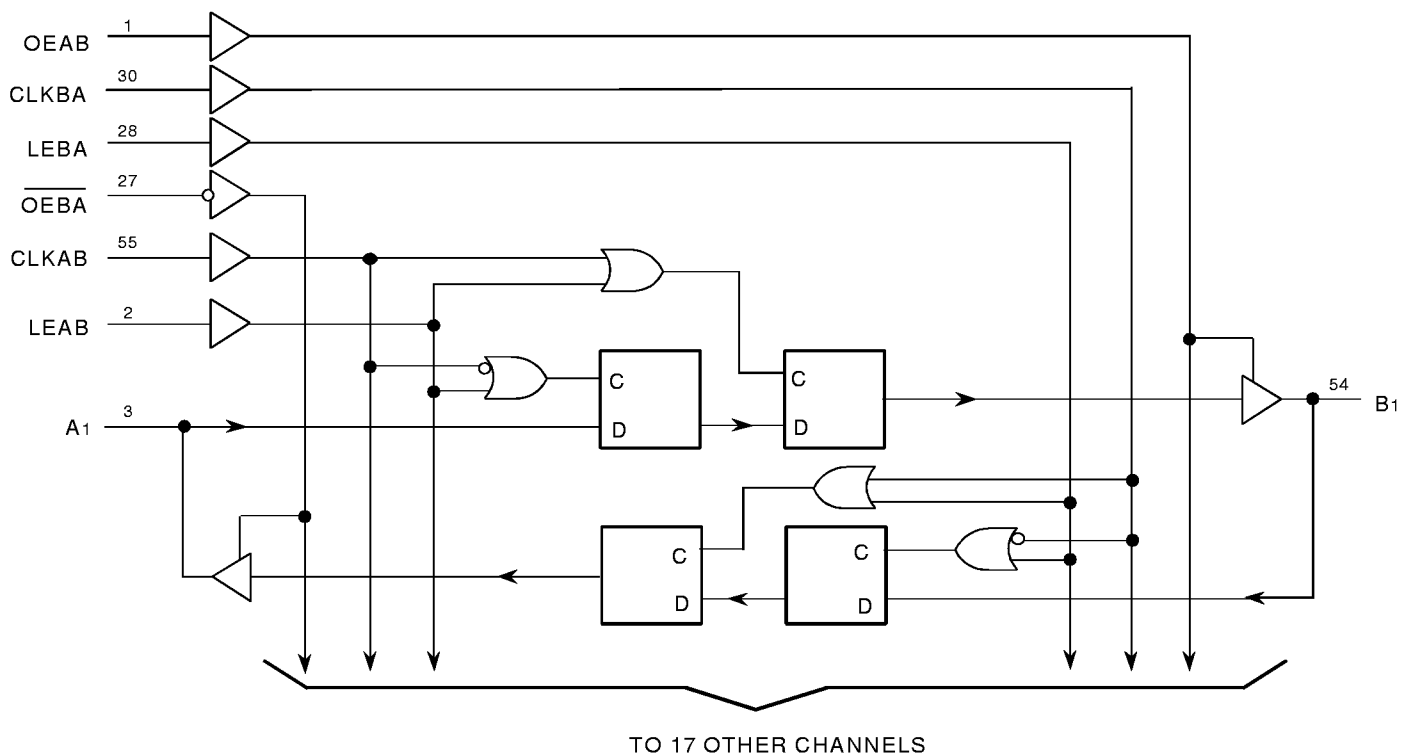
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical tsk(o) (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch CERPACK packages
- Extended commercial range of -40°C to +85°C
- Balanced Output Drivers:
 - $\pm 24\text{mA}$ (commercial)
 - $\pm 16\text{mA}$ (military)
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) < 0.6V at VCC = 5V, TA = 25°C

DESCRIPTION:

The FCT162501AT/CT/ET 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. OEAB is the output enable for the B port. Data flow from the B port to the A port is similar but requires using OEBA, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT162501AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162501AT/CT/ET are plug-in replacements for the FCT16501AT/CT/ET and ABT16501 for on-board bus interface applications.

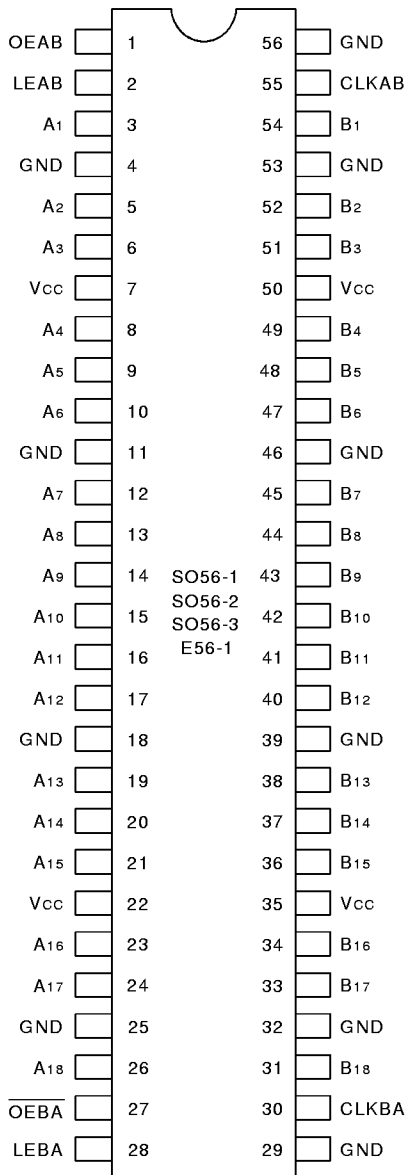
Functional Block Diagram



MILITARY AND COMMERCIAL TEMPERATURE RANGES

AUGUST 1999

PIN CONFIGURATION



SSOP/TSSOP/TVSOP/CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
$V_{\text{TERM}}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{\text{TERM}}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{\text{CC}}+0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

5v16-link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXT.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	$V_{\text{IN}} = 0\text{V}$	3.5	6	pF
COUT	Output Capacitance	$V_{\text{OUT}} = 0\text{V}$	3.5	8	pF

5v16-link

NOTE:

- This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,4)

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B ⁽²⁾
H	L	H	X	B ⁽³⁾

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State Output pins) ⁽⁵⁾		$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{OCL} I_{OCH} I_{OZZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

5v16-link

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -16\text{mA MIL.}$ $I_{OH} = -24\text{mA COM'L.}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 16\text{mA MIL.}$ $I_{OL} = 24\text{mA COM'L.}$	—	0.3	0.55	V

5v16-link

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $OEAB = \overline{OEBA} = V_{CC}$ or GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	75	120	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ (CLKAB) 50% Duty Cycle $OEAB = \overline{OEBA} = V_{CC}$ $LEAB = \text{GND}$ Eighteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.5	20.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

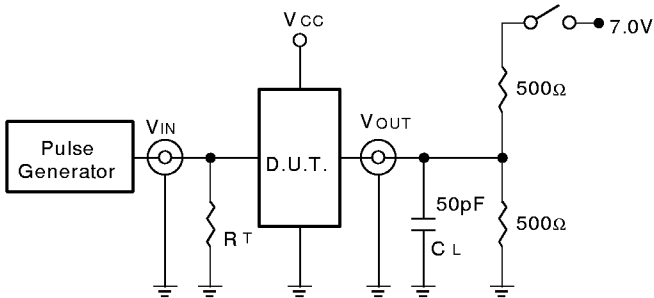
Symbol	Parameter	Condition ⁽¹⁾	FCT162501AT				FCT162501CT				FCT162501ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
fMAX	CLKAB or CLKBA frequency ⁽⁴⁾	CL = 50pF	—	150	—	150	—	150	—	150	—	150	—	—	MHz
tPLH	Propagation Delay	RL = 500Ω	1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	1.5	3.8	—	—	ns
tPHL	Ax to Bx or Bx to Ax														
tPLH	Propagation Delay		1.5	5.6	1.5	6	1.5	5.3	1.5	5.6	1.5	4.2	—	—	ns
tPHL	LEBA to Ax, LEAB to Bx														
tPLH	Propagation Delay		1.5	5.6	1.5	6	1.5	5.3	1.5	5.4	1.5	4.2	—	—	ns
tPHL	CLKBA to Ax, CLKAB to Bx														
tPZH	Output Enable Time		1.5	6	1.5	6.4	1.5	5.6	1.5	6	1.5	4.8	—	—	ns
tPZL	$\overline{\text{OEBA}}$ to Ax, OEAB to Bx														
tPHZ	Output Disable Time		1.5	5.6	1.5	6	1.5	5.2	1.5	5.6	1.5	5.2	—	—	ns
tPLZ	$\overline{\text{OEBA}}$ to Ax, OEAB to Bx														
tsu	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA		3	—	3	—	3	—	3	—	2.4	—	—	—	ns
th	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	0	—	0	—	—	—	ns
tsu	Set-up Time HIGH or LOW	Clock LOW	3	—	3	—	3	—	3	—	2	—	—	—	ns
	Ax to LEAB, Bx to LEBA	Clock HIGH	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
th	Hold Time, HIGH or LOW Ax to LEAB, Bx to LEBA	1.5	—	1.5	—	1.5	—	1.5	—	0.5	—	—	—	ns	
tw	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾	3	—	3	—	3	—	3	—	3	—	—	—	ns	
tw	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾	3	—	3	—	3	—	3	—	3	—	—	—	ns	
tsk(o)	Output Skew ⁽³⁾	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns	

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

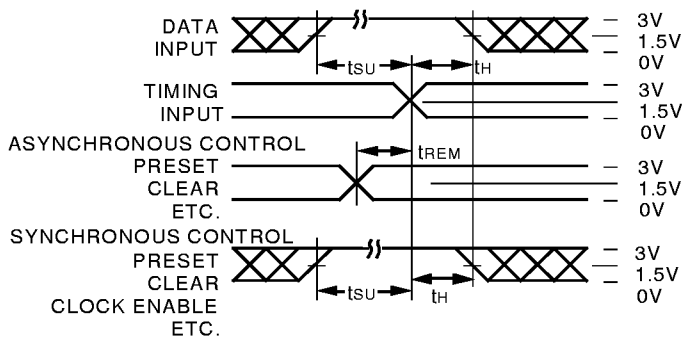
5v16-link

DEFINITIONS:

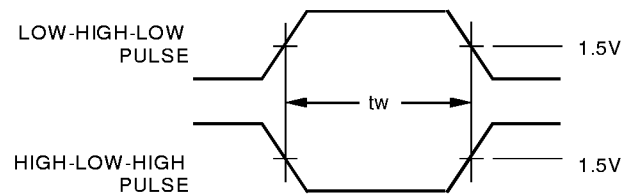
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

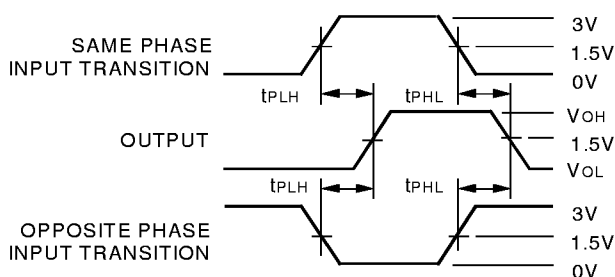
SET-UP, HOLD, AND RELEASE TIMES



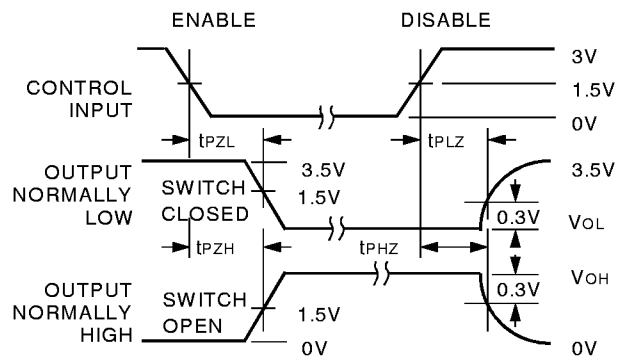
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.

ORDERING INFORMATION

<u>IDT</u> <u>X</u>	<u>FCT</u> <u>XXX</u>	<u>X</u>	<u>XXXX</u>	<u>X</u>	<u>X</u>		
Temperature Range	Family	Bus Hold	Device Type	Package	Process		
						Blank B	Commercial MIL-STD-883, Class B
						PV PA PF E	Shrink Small Outline Package (SO56-1) Thin Shrink Small Outline Package (SO56-2) Thin Very Small Outline Package (SO56-3) CERPACK (E56-1)
						501AT 501CT 501ET	18-Bit Registered Transceiver
						Blank	No Bus-Hold
						162	Double-Density 5 Volt Balanced Drive
						54 74	- 55°C to +125°C - 40°C to +85°C



CORPORATE HEADQUARTERS

2975 Stender Way
 Santa Clara, CA 95054

for SALES:

800-345-7015 or 408-727-6116
 fax: 408-492-8674
www.idt.com*

*To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.
 The IDT logo is a registered trademark of Integrated Device Technology, Inc.