



3.3V CMOS OCTAL D REGISTER (3-STATE)

IDT74FCT3574/A

FEATURES:

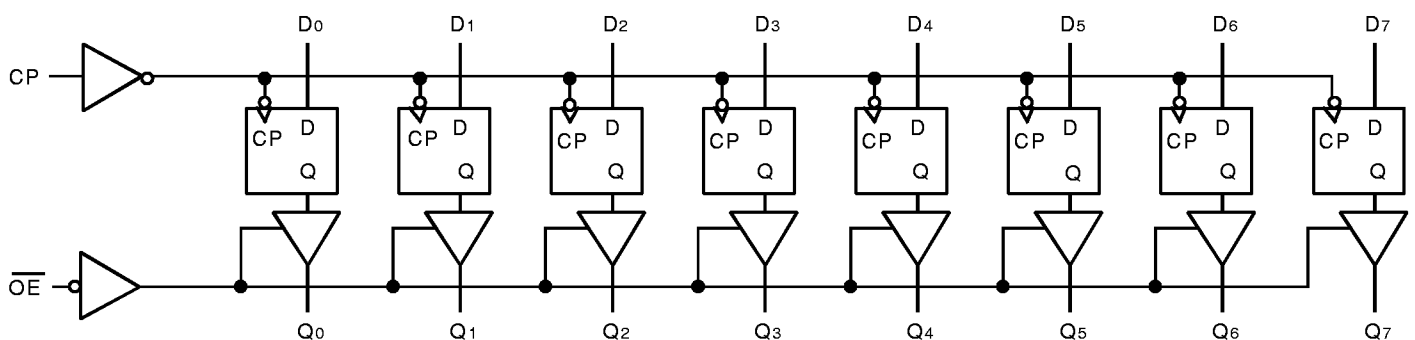
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range or $V_{CC} = 2.7V$ to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

DESCRIPTION:

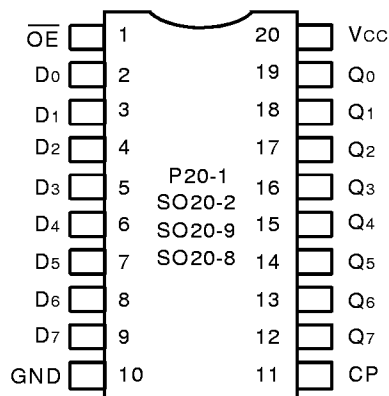
The FCT3574/A are 8-bit registers built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the $\overline{OE}$ input is low, the eight outputs are enabled. When the $\overline{OE}$ input is high, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the low-to-high transition of the clock input.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/ SOIC/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to +7	V
V _{TERM} ⁽⁴⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +60	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	4	8	pF

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NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
Dx	D Flip-Flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
Qx	3-State outputs
$\overline{OE}$	Active LOW 3-State Output Enable input

FUNCTION TABLE (1)

Function	Inputs			Outputs
	$\overline{OE}$	CP	Dx	Qx
HI-Z	H	L	X	Z
	H	H	X	Z
LOAD REGISTER	L	↑	L	L
	L	↑	H	H
	H	↑	L	Z
	H	↑	H	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
NC = No Change
↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	—	5.5	V
	Input HIGH Level (I/O pins)			2	—	$V_{CC}+0.5$	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	$V_{CC} = \text{Max.}$	$V_I = 5.5\text{V}$	—	—	± 1	μA
	Input HIGH Current (I/O pins)		$V_I = V_{CC}$	—	—	± 1	
I_{IL}	Input LOW Current (Input pins)		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins)		$V_I = \text{GND}$	—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins)	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	± 1	μA
I_{OZL}			$V_O = \text{GND}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		-36	-60	-110	mA
I_{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_O = 1.5\text{V}^{(3)}$		50	90	200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -0.1\text{mA}$	$V_{CC}-0.2$	—	—	V
			$I_{OH} = -3\text{mA}$	2.4	3	—	
		$V_{CC} = 3\text{V}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4 ⁽⁵⁾	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 0.1\text{mA}$	—	—	0.2	V
			$I_{OL} = 16\text{mA}$	—	0.2	0.4	
			$I_{OL} = 24\text{mA}$	—	0.3	0.55	
		$V_{CC} = 3\text{V}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 24\text{mA}$		0.3	0.5	
I_{OS}	Short Circuit Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-135	-240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	0.1	10	μA

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- $V_{OH} = V_{CC} - 0.6\text{V}$ at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ 50% Duty Cycle One Input Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	85	$\mu A/\text{MHz/Bit}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	0.9	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.6	0.9	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $f_i = 2.5\text{MHz}$ 50% Duty Cycle Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	2.2 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	1.5	2.3 ⁽⁵⁾	

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽³⁾

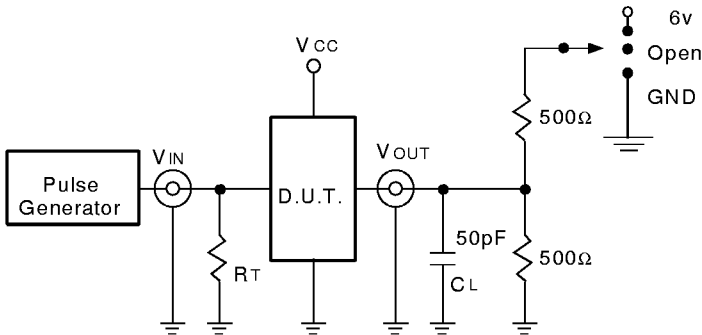
Symbol	Parameter	Conditions ⁽¹⁾	FCT3574		FCT3574A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Q _X ⁽³⁾	CL = 50pF RL = 500Ω	2	10	2	6.5	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	12.5	1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	8	1.5	5.5	ns
t _{SU}	Set-up Time HIGH or LOW, Dx to CP		2	—	2	—	ns
t _H	Hold Time HIGH or LOW, Dx to CP		1.5	—	1.5	—	ns
t _w	CP Pulse Width HIGH or LOW		7	—	5	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other Tests	Open

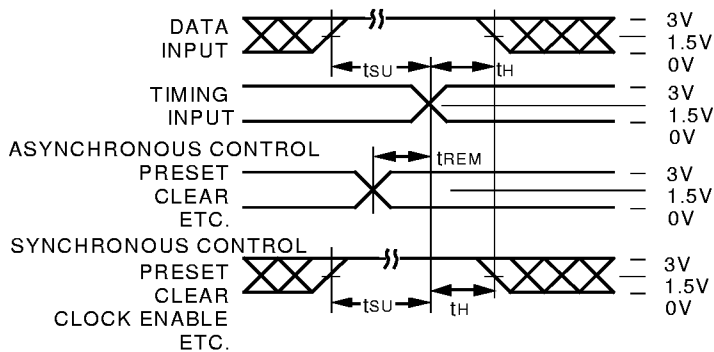
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DEFINITIONS:

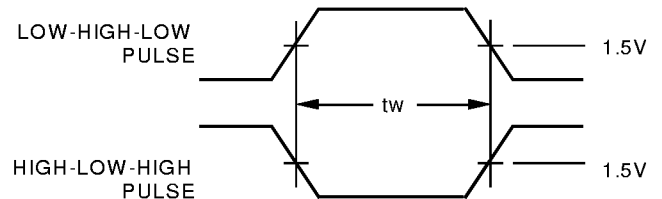
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

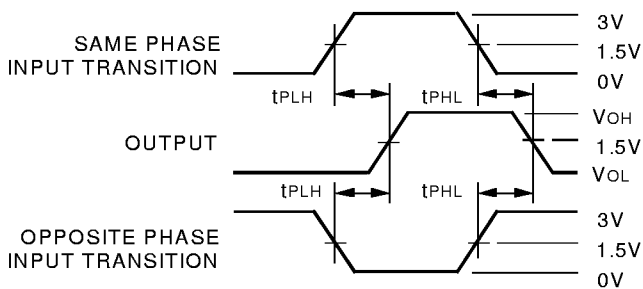
SET-UP, HOLD, AND RELEASE TIMES



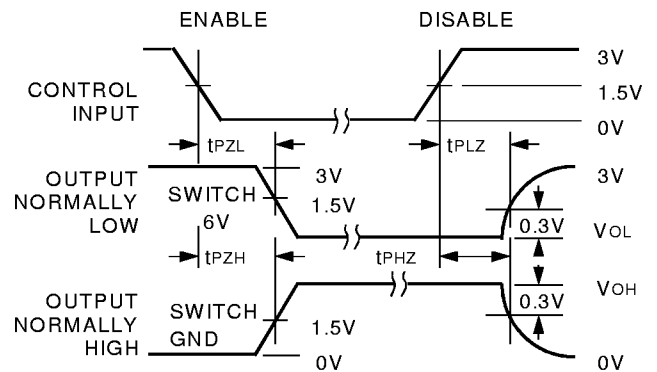
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION

IDT	XX	FCT	X	XX	X	
Temp. Range			Family	Device Type	Package	
					P	Plastic DIP (P20-1)
					SO	Small Outline IC (SO20-2)
					PG	Thin Shrink Small Outline Package (SO20-9)
					Q	Quarter-size Small Outline Package (SO20-8)
				574		Non-Inverting Octal D Register
				574A		
				3		3.3 Volt
				74		- 40°C to +85°C



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