



Integrated Device Technology, Inc.

FAST CMOS 10-BIT BUFFERS

IDT54/74FCT827/2827AT/BT/CT/DT
IDT54/74FCT828/2828AT/BT/CT/DT

FEATURES:

- **Common features:**
 - A, B, C and D speed grades
 - Low input and output leakage $\leq 1\mu\text{A}$ (max.)
 - CMOS power levels
 - True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
 - Meets or exceeds JEDEC standard 18 specifications
 - Product available in Radiation Tolerant and Radiation Enhanced versions
 - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
 - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT827/828AT/BT/CT/DT:**
 - High drive outputs (-15mA I_{OH} , 48mA I_{OL})
- **Features for FCT2827/2828AT/BT/CT/DT:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise

DESCRIPTION:

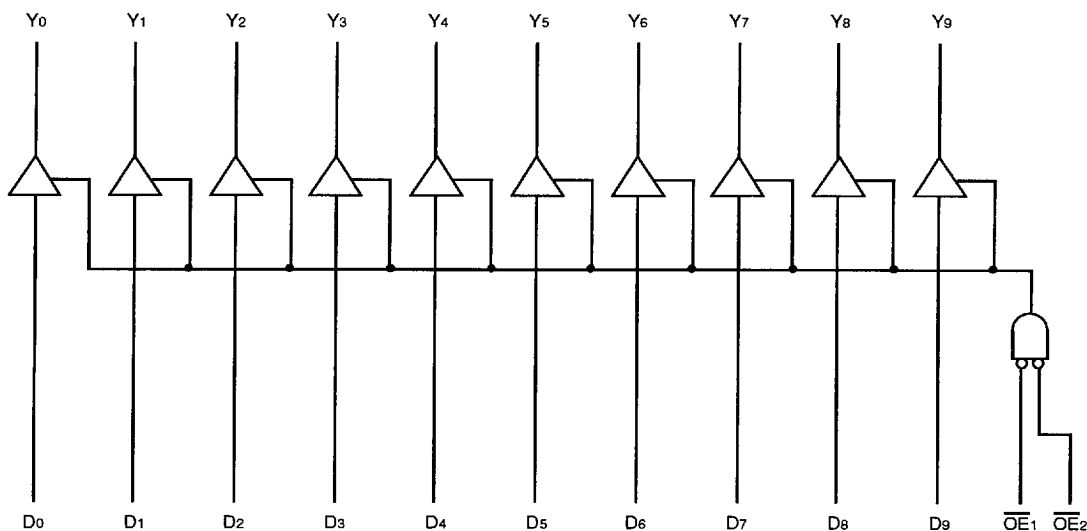
The IDT54/74FCT8xx series is built using an advanced dual metal CMOS technology.

The IDT54/74FCT827/2827AT/BT/CT/DT and IDT54/74FCT828/2828AT/BT/CT/DT 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT8xx high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

The IDT54/74FCT2827AT/BT/CT/DT and IDT54/74FCT2828AT/BT/CT/DT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. IDT54/74FCT2xxxT parts are plug-in replacements for IDT54/74FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM



2573 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

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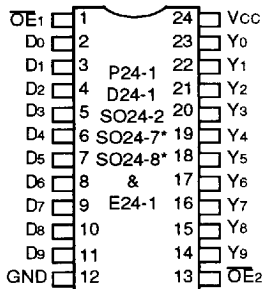
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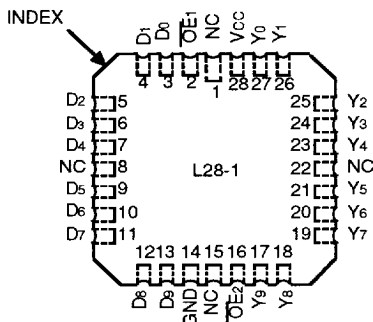
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PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

2573 drw 02



LCC
TOP VIEW

2573 drw 03

* FCT827/2827AT/BT/CT/DT only.

PIN DESCRIPTION

Names	I/O	Description
OE _i	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D _i	I	10-bit data input.
Y _i	O	10-bit data output.

2573 tbl 01

FUNCTION TABLES

827 (NON-INVERTING)⁽¹⁾

Inputs			Output	Function
OE ₁	OE ₂	D _i	Y _i	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

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828 (INVERTING)⁽¹⁾

Inputs			Output	Function
OE ₁	OE ₂	D _i	Y _i	
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

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- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	V _{CC} = Max.	V _I = 2.7V	—	—	±1	μA
I _{IL}	Input LOW Current ⁽⁴⁾		V _I = 0.5V	—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
I _I	Input HIGH Current ⁽⁴⁾	V _{CC} = Max., V _I = V _{CC} (Max.)		—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-60	-120	-225	mA
V _H	Input Hysteresis	—		—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT827/828T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL.	2.4	3.3	—	V
			I _{OH} = -8mA COM'L.	—	—	—	—
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.5	V

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OUTPUT DRIVE CHARACTERISTICS FOR FCT2827/2828T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL. I _{OH} = -24mA COM'L.	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16mA MIL. I _{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is ±5μA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾			Min.	Typ. ⁽²⁾	Max.	Unit
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾			—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open OE ₁ = OE ₂ = GND One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	FCTxxxT FCT2xxxT	—	0.15 0.06	0.25 0.12	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _i = 10MHz 50% Duty Cycle OE ₁ = OE ₂ = GND One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND V _{IN} = 3.4V V _{IN} = GND	FCTxxxT FCT2xxxT FCTxxxT FCT2xxxT	—	1.5 0.6 1.8 0.9	3.5 2.2 4.5 3.2	mA
		V _{CC} = Max. Outputs Open f _i = 2.5MHz 50% Duty Cycle OE ₁ = OE ₂ = GND Eight Bits Toggling	V _{IN} = V _{CC} V _{IN} = GND V _{IN} = 3.4V V _{IN} = GND	FCTxxxT FCT2xxxT FCTxxxT FCT2xxxT	—	3.0 1.2 5.0 3.2	6.0 ⁽⁵⁾ 3.4 ⁽⁵⁾ 14.0 ⁽⁵⁾ 11.4 ⁽⁵⁾	

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC} D_{HN}T + I_{CCD} (f_{CP}/2 + f_iN_i)
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT827AT/828AT FCT2827AT/2828AT				FCT827BT/828BT FCT2827BT/2828BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay 827 Di to Yi	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPLH tPHL	Propagation Delay 828 Di to Yi	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	5.5	1.5	6.5	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	14.0	1.5	16.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time OEi to Yi	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time OEi to Yi	CL = 5pF ⁽³⁾ RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

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Symbol	Parameter	Condition ⁽¹⁾	FCT827CT/828CT FCT2827CT/2828CT				FCT827DT/828DT FCT2827DT/2828DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay 827 Di to Yi	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	1.5	3.8	—	—	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	10.0	1.5	11.0	1.5	7.5	—	—	
tPLH tPHL	Propagation Delay 828 Di to Yi	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	—	3.8	—	—	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	10.0	1.5	11.0	—	7.5	—	—	
tPZH tPZL	Output Enable Time OEi to Yi	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.0	—	—	ns
		CL = 300pF ⁽³⁾ RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time OEi to Yi	CL = 5pF ⁽³⁾ RL = 500Ω	1.5	5.7	1.5	6.7	1.5	4.3	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.3	—	—	

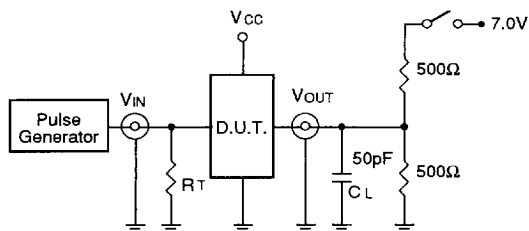
NOTES:

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- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- These conditions are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2573 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

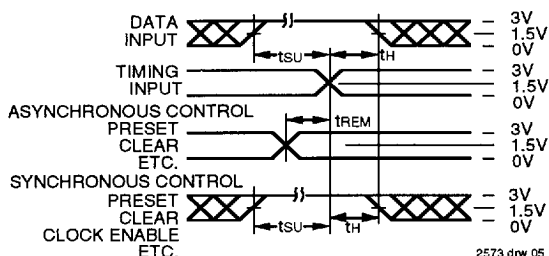
DEFINITIONS:

C_L = Load capacitance; includes jig and probe capacitance.

R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

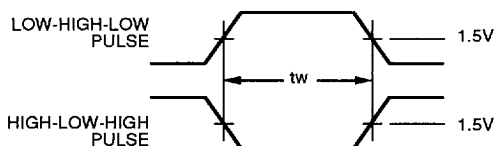
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SET-UP, HOLD AND RELEASE TIMES



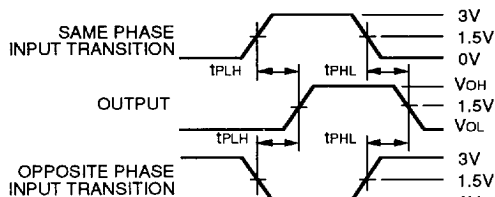
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PULSE WIDTH



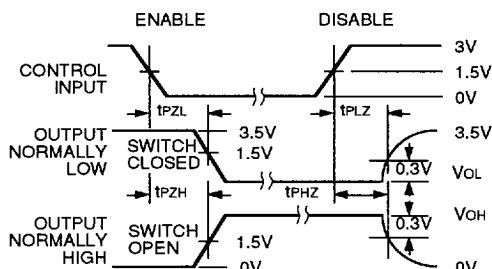
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PROPAGATION DELAY



2573 drw 07

ENABLE AND DISABLE TIMES



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NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION

IDT	XX	FCT	X	XX	X	X											
Temp. Range			Family	Device Type	Package	Process											
						Blank B	Commercial MIL-STD-883, Class B										
						P	Plastic DIP										
						D	CERDIP										
						E	CERPACK										
						L	Leadless Chip Carrier										
						SO	Small Outline IC										
						PY	Shrink Small Outline Package										
						Q	Quarter-size Small Outline Package										
												827AT	Non-Inverting 10-Bit Buffer				
						828AT	Inverting 10-Bit Buffer										
						827BT											
						828BT											
						827CT											
						828CT											
						827DT											
						828DT											
							Blank					High Drive					
							2					Balanced Drive					
							54					-55°C to +125°C					
							74	0°C to +70°C									

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