



3.3V CMOS OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O

IDT74LVC373A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.65mm pitch SSOP,
0.635mm pitch QSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.3\text{V}$ to 3.6V , Extended Range
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC373A:

- High Output Drivers: $\pm 24\text{mA}$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

The LVC373A Octal transparent D-type latch is built using advanced dual metal CMOS technology.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

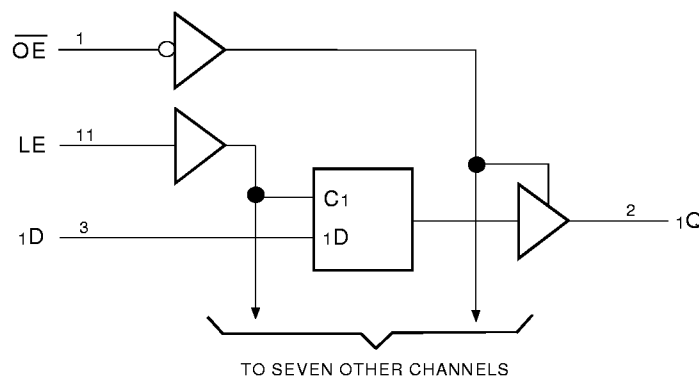
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

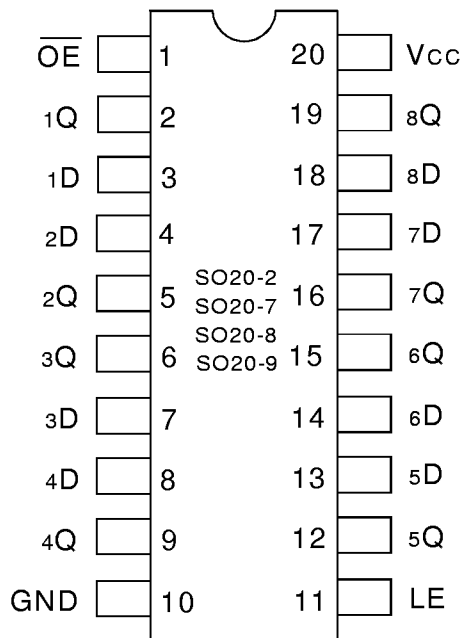
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T _{STG}	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output-enable Input (Active LOW)
LE	Latch-enable Input
x _D	Data Inputs
x _Q	3-State Data Outputs

FUNCTION TABLE (each latch) ⁽¹⁾

Inputs			Outputs
$\overline{OE}$	LE	x _D	x _Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
Q₀ = Indicates previous state before the indicated steady-state input conditions

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = - 40°C To +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IIH IIL	Input Leakage Current	VCC = 3.6V	VI = 0 to 5.5V	—	—	±5	μA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = 0 to 5.5V	—	—	±10	μA
IOFF	Input/Output Power Off Leakage	VCC = 0V, VIN or VO ≤ 5.5V		—	—	±50	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = - 18mA		—	- 0.7	- 1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = 3.6V	VIN = GND or VCC	—	—	10	μA
			3.6 ≤ VIN ≤ 5.5V ⁽²⁾	—	—	10	
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V, other inputs at VCC or GND		—	—	500	μA

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NOTES:

1. Typical values are at VCC = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = - 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to +85°C.

OPERATING CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per latch Outputs enabled	$C_L = 0pF$, $f = 10MHz$	46	pF
CPD	Power Dissipation Capacitance per latch Outputs disabled		3	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 2.7V$		$V_{CC} = 3.3V \pm 0.3V$		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay xD to xQ	—	—	—	7.8	1.5	6.8	ns
t _{PLH} t _{PHL}	Propagation Delay LE to xQ	—	—	—	8.2	2	7.6	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OE}$ to xQ	—	—	—	8.7	1.5	7.7	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OE}$ to xQ	—	—	—	7.6	1.5	7	ns
tw	Pulse Duration, LE HIGH	—	—	3.3	—	3.3	—	ns
tsu	Set up Time, data before LE $\downarrow$	—	—	2	—	2	—	ns
th	Hold Time, data after LE $\downarrow$	—	—	1.5	—	1.5	—	ns
tsk(0)	Output Skew ⁽²⁾	—	—	—	—	—	1	ns

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ C$ to $+85^\circ C$.
2. Skew between any two outputs of the same package and switching in the same direction.

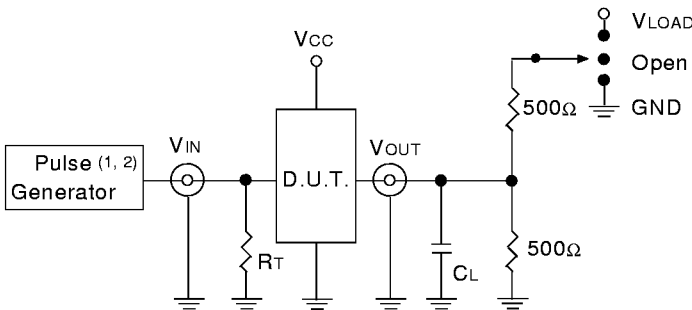
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1) = 3.3V ± 0.3V	V _{CC} (1) = 2.7V	V _{CC} (2) = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

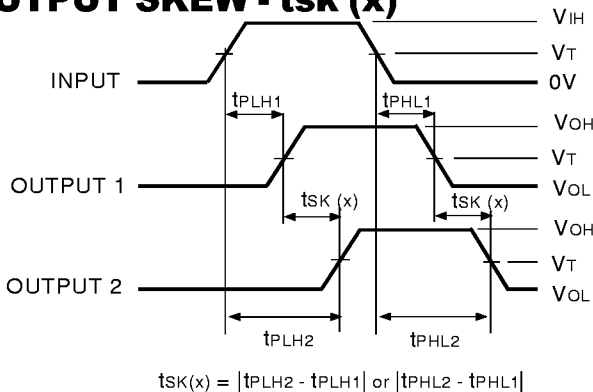
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK}(x)



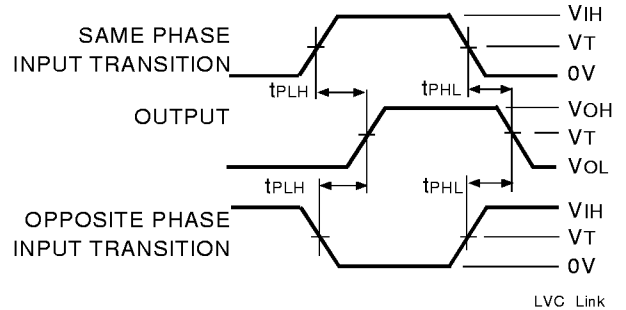
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

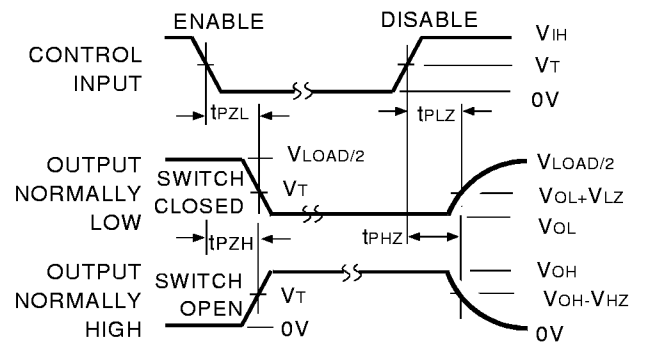
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PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

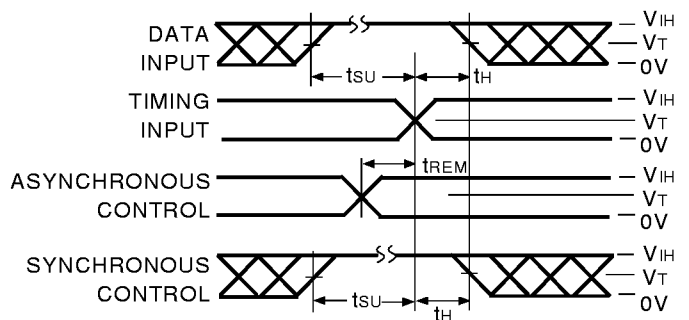


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NOTE:

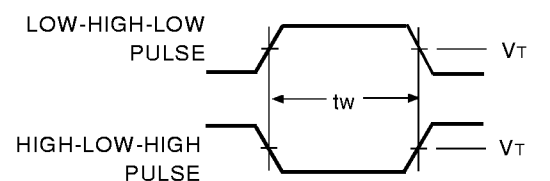
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	X	XXXX	XX	
Temp. Range			Bus-Hold	Device Type	Package	
					SO	Small Outline IC (gull wing) (SO20-2)
					PY	Shrink Small Outline Package (SO20-7)
					Q	Quarter Size Small Outline Package (SO20-8)
					PG	Thin Shrink Small Outline Package (SO20-9)
				373A		Octal Transparent D-Type Latch with 3-State Outputs, $\pm 24\text{mA}$
				Blank		No Bus-hold
				74		-40°C to $+85^{\circ}\text{C}$



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