



Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUS TRANSCIEVER/REGISTER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

IDT74LVCH16646A

FEATURES:

- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVCH16646A

- High Output Drivers: $\pm 24mA$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems.
- Data communication and telecommunication systems

DESCRIPTION:

The LVCH16646A 16-bit bus transceiver and register is built using advanced dual metal CMOS technology. This high-speed, low power device is organized as two independent 8-bit D-type

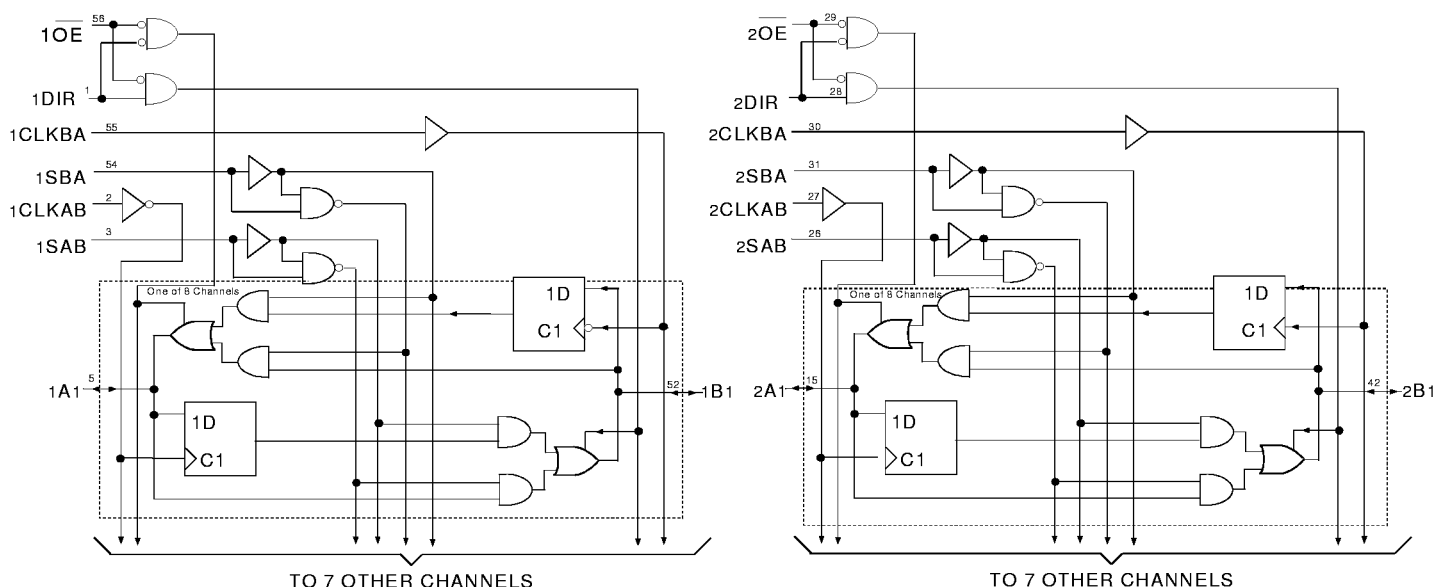
transceivers with 3-state D-type registers. The controls circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (DIR), over-riding Output Enable control ($\overline{OE}$) and Select lines (SAB and SBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVCH16646A has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16646A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

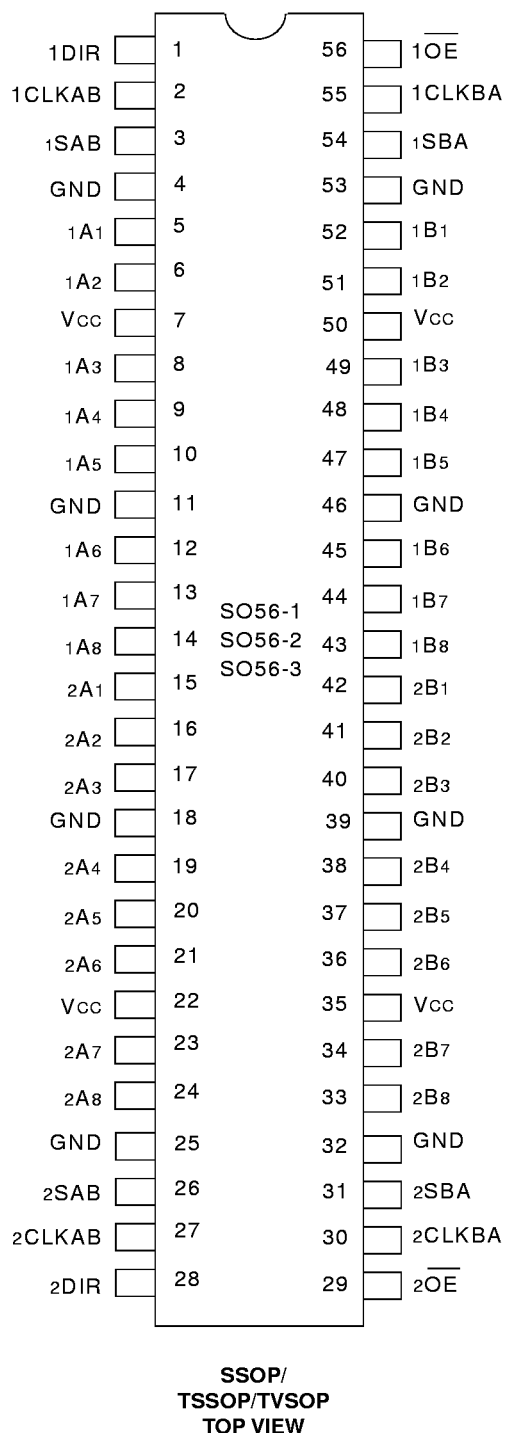


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EXTENDED COMMERCIAL TEMPERATURE RANGE

SEPTEMBER 1998

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	− 0.5 to +6.5	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	− 0.5 to +6.5	V
T _{STG}	Storage Temperature	− 65 to +150	°C
I _{OUT}	DC Output Current	− 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	− 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs ⁽¹⁾ Data Register B Outputs
xBx	Data Register B Inputs ⁽¹⁾ Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xsAB, xsBA	Output Data Source Select Inputs
xOE	Output Enable Inputs
xDIR	Direction Control Inputs

NOTE:

- These pins have "Bus-hold".
All other pins are standard inputs, outputs or I/O's.

FUNCTION TABLE (2)

Inputs						Data I/O ⁽¹⁾		Operation or Function
$\overline{xOE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	A1-A8	B1-B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified ⁽¹⁾
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified ⁽¹⁾
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

NOTES:

- The data-output functions may be enabled or disabled by various signals at $\overline{OE}$ or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = Low-to-High Transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCCL} I _{CCCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V other inputs at V _{CC} or GND		—	—	500	μA

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NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies in the disabled state only.

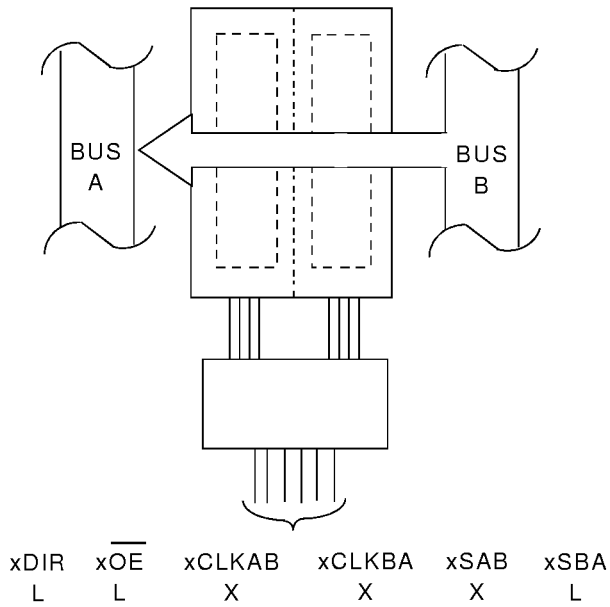
BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

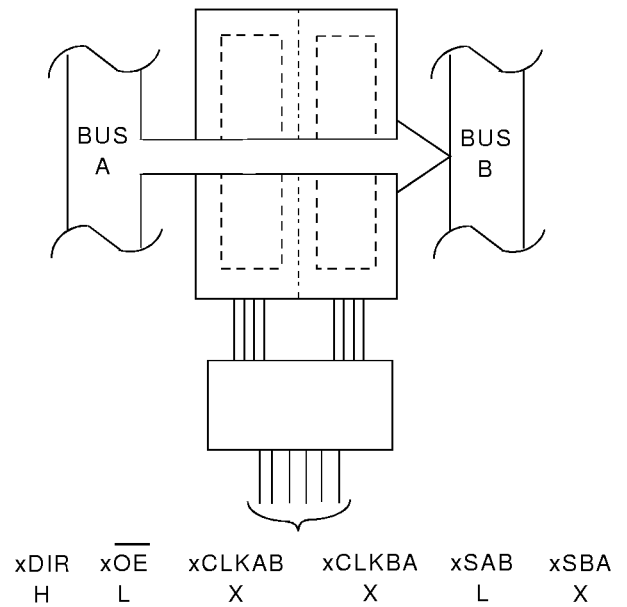
LVC Link

NOTES:

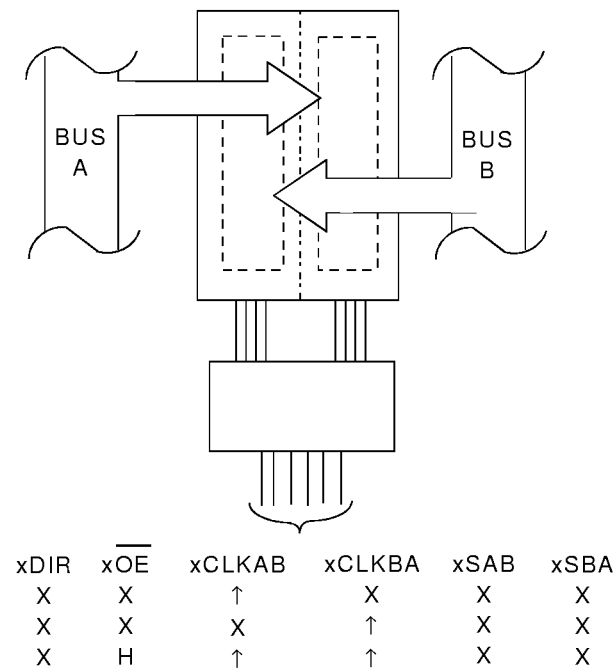
- Pins with Bus-hold are identified in the pin description.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.



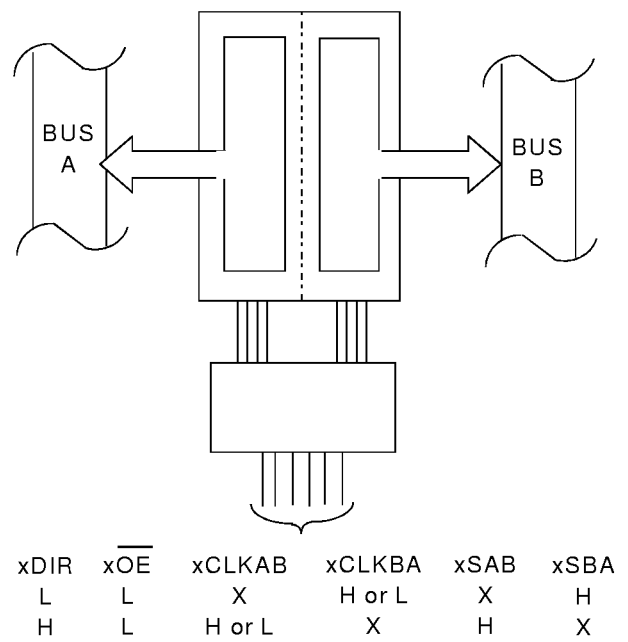
**REAL-TIME TRANSFER
BUS B TO A**



**REAL-TIME TRANSFER
BUS A TO B**



**STORAGE FROM
A, B, OR A AND B**



**TRANSFER STORED
DATA TO A AND/OR B**

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = – 0.1mA	VCC – 0.2	—	V
		VCC = 2.3V	IOH = – 6mA	2	—	
		VCC = 2.3V	IOH = – 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3.0V		2.4	—	
		VCC = 3.0V	IOH = – 24mA	2.2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3.0V	IOL = 24mA	—	0.55	

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NOTE:

1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = – 40°C to +85°C.

OPERATING CHARACTERISTICS, VCC = 3.3V ± 0.3V, TA = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	CL = 0pF, f = 10Mhz	60	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		12	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	VCC = 2.7V		VCC = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
fMAX		150	—	150	—	MHz
tPLH	Propagation Delay	—	6.8	1.3	5.7	ns
tPHL	xAx to xBx or xBx to xAx					
tPLH	Propagation Delay	—	7.9	1.8	6.7	ns
tPHL	xCLKAB or xCLKBA to xAx or xBx					
tPLH	Propagation Delay	—	9.2	1.7	7.7	ns
tPHL	xSBA or xSAB to xAx or xBx					
tPZH	Output Enable Time	—	8.5	1.3	6.9	ns
tPZL	xOE to xAx or xBx					
tPZH	Output Enable Time	—	8.5	1.4	7.2	ns
tPZL	xDIR to xAx or xBx					
tPHZ	Output Disable Time	—	7.7	2.1	6.9	ns
tPLZ	xOE to xAx or xBx					
tPHZ	Output Disable Time	—	7.8	2	7	ns
tPLZ	xDIR to xAx or xBx					
tSU	Set-up Time, xAx or xBx before xCLKAB↑ or xCLKBA↑	3.2	—	2.9	—	ns
tH	Hold Time, xAx or xBx after xCLKAB↑ or xCLKBA↑	0	—	0.3	—	ns
tW	Pulse duration, CLK HIGH or LOW	3.3	—	3.3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. TA = – 40°C to + 85°C.
 2. Skew between any two outputs of the same package and switching in the same direction.

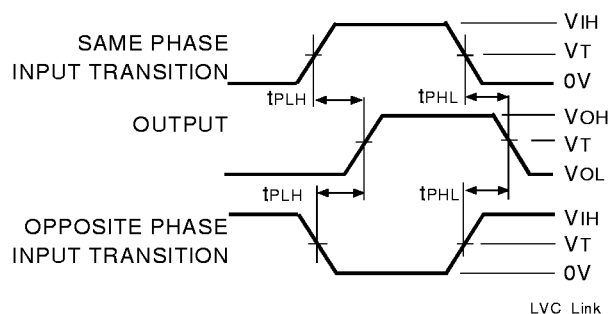
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(1)} = 2.7V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC} / 2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

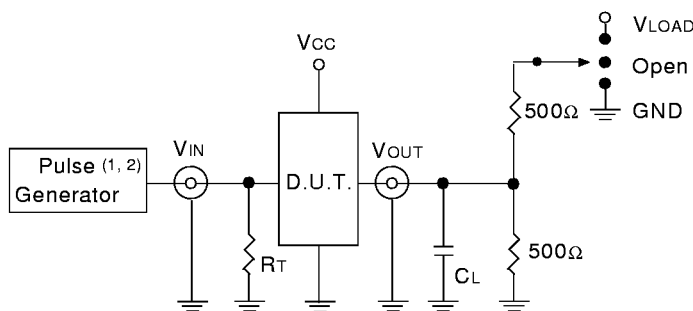
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PROPAGATION DELAY



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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

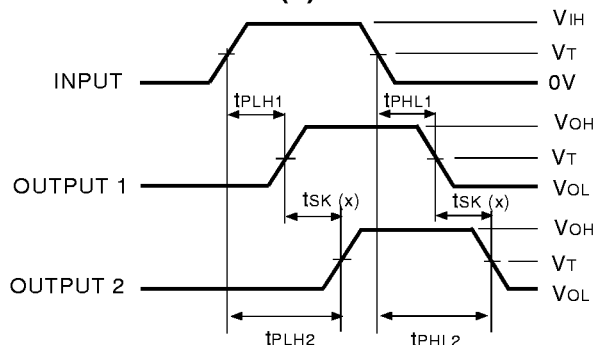
1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.
2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_F \leq 2\text{ns}$; $t_R \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - $t_{SK}(x)$



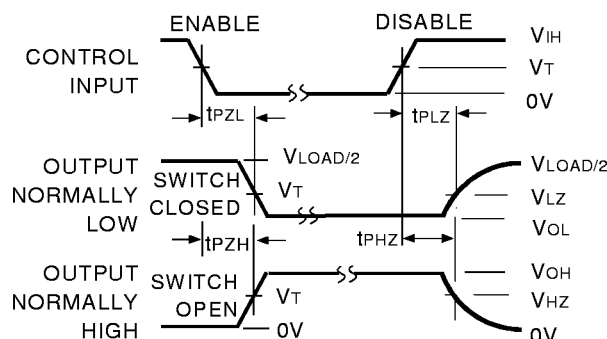
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

ENABLE AND DISABLE TIMES

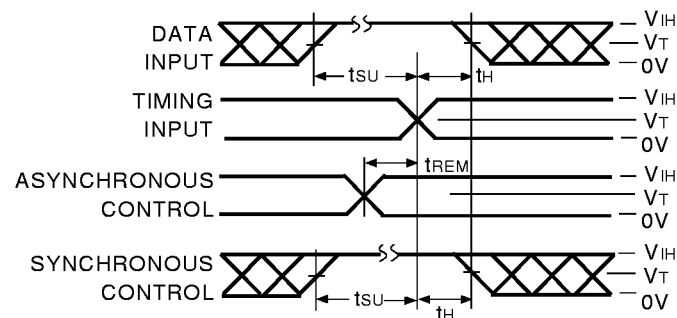


LVC Link

NOTE:

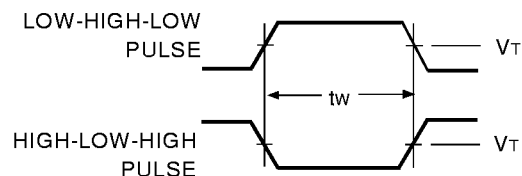
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD AND RELEASE TIMES



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PULSE WIDTH



LVC Link

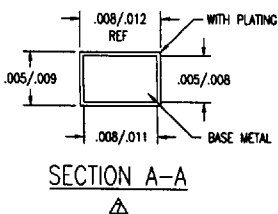
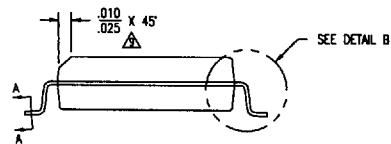
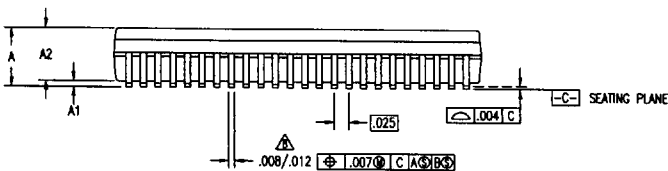
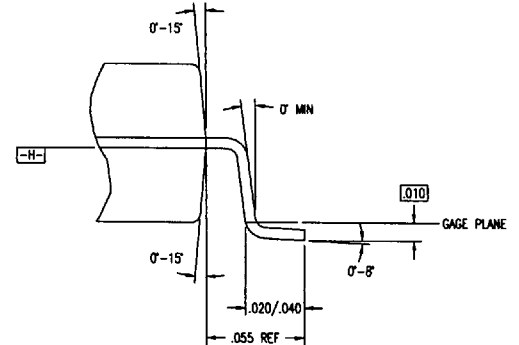
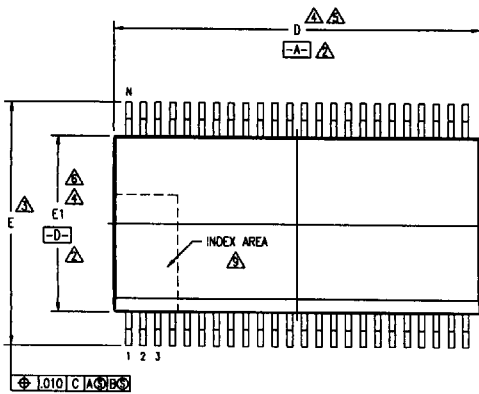
ORDERING INFORMATION

IDT	<u>XX</u>	<u>LVC</u>	<u>X</u>	<u>XX</u>	<u>XXXX</u>	<u>XX</u>	
Temp. Range		Bus-Hold		Family	Device Type	Package	
						646A	PV Shrink Small Outline Package (SO56-1)
							PA Thin Shrink Small Outline Package (SO56-2)
							PF Thin Very Small Outline Package (SO56-3)
						16	16-Bit Bus Transceiver/Register with 3-State Outputs and 5 Volt Tolerant I/O
Double-Density w/Resistors, ±24mA							
							H Bus-hold
							74 -40°C to +85°C

PACKAGE DIAGRAM OUTLINES

SSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	



TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Slender Way, Santa Clara, CA 95054	
XXXS	±	PHONE: (408) 727-8118	
XXXX		FAX: (408) 482-8874	
XXXXS		TWC: 910-338-2070	
APPROVALS	DATE	TITLE	REV
DRAWN AA	08/15/90	PV PACKAGE OUTLINE	02
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE C	
		DRAWING No. PSC-4029	
		DO NOT SCALE DRAWING	

PACKAGE DIAGRAM OUTLINES SSOP (Continued)

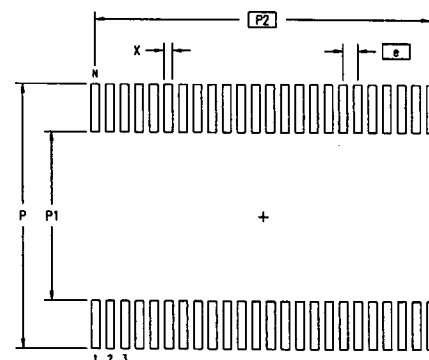
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WJ
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1				DWG #		S056-1			
SYMBOL	JEDEC VARIATION				NOTE	JEDEC VARIATION				NOTE	
	AA			AB							
	MIN	NOM	MAX	MIN		NOM	MAX				
A	.095	.102	.110		.095	.102	.110				
A1	.008	.012	.016		.008	.012	.016				
A2	.088	.090	.092		.088	.090	.092				
D	.620	.625	.630	4,5	.720	.725	.730	4,5			
E	.395	.405	.420	3	.395	.405	.420	3			
E1	.291	.295	.299	4,6	.291	.295	.299	4,6			
N	48				56						

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

LAND PATTERN DIMENSIONS



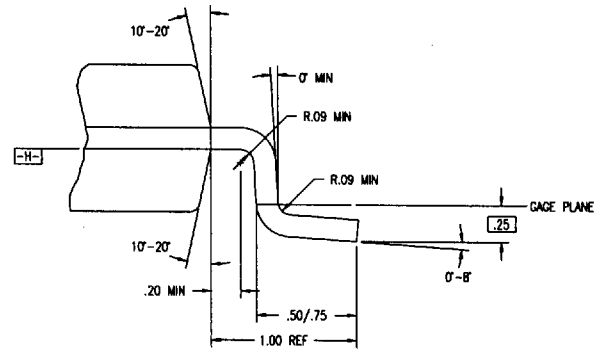
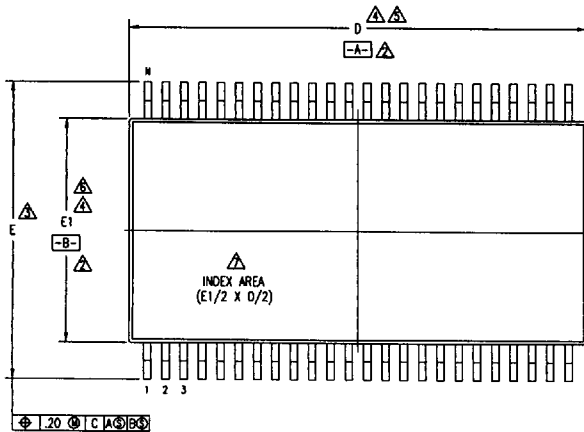
	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC.	
DECIMAL	ANGULAR	2075 Stoner Way, Santa Clara, CA 95054	
XXX.X	±	PHONE: (408) 727-8116	
XXXX.X		FAX: (408) 482-8874	
XXXX.X		TW: 810-338-2070	
APPROVALS	DATE	TITLE	REV
DRN	06/15/90	PV PACKAGE OUTLINE	
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE	REV
		C	02
		DRAWING No.	
		PSC-4029	
		DO NOT SCALE DRAWING	

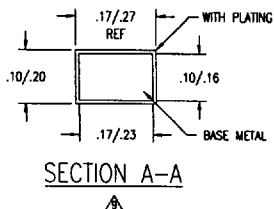
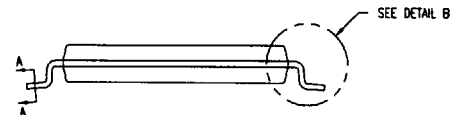
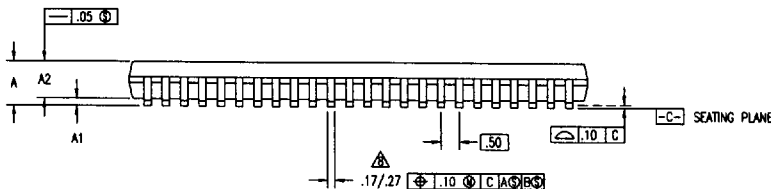
PACKAGE DIAGRAM OUTLINES

TSSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	



DETAIL B



SECTION A-A

TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
XXX.X	±	PHONE: (408) 727-8118	
XXXX.X		FAX: (408) 492-8674	
XXXXX.X		TW: 910-336-2070	
APPROVALS	DATE	TITLE	REV
DRAWN	01/15/93	PA PACKAGE OUTLINE	
CHECKED		6.10 mm BODY WIDTH TSSOP	
		.50 mm PITCH	
		SIZE C	DRAWING No. PSC-4039
			REV 03
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES TSSOP (Continued)

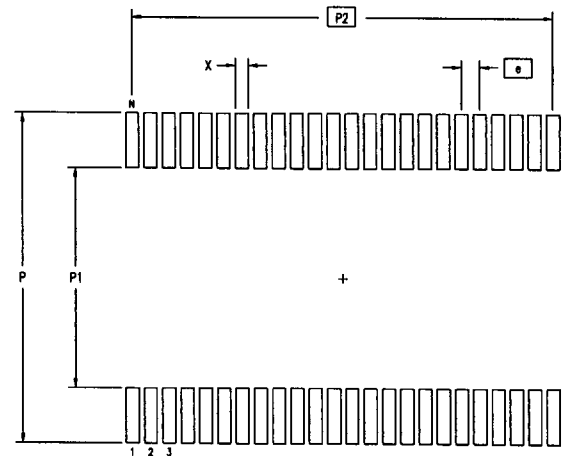
DWG #				S048-2		DWG #				S056-2	
SYMBOL	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE			
	ED				EE						
	MIN	NOM	MAX		MIN	NOM	MAX				
	MIN	NOM	MAX		MIN	NOM	MAX				
A	—	—	1.10		—	—	1.10				
A1	.05	—	.15		.05	—	.15				
A2	.85	1.00	1.05		.85	1.00	1.05				
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5			
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3			
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6			
N	48				56						

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A- and $\square$ -B- TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE $\square$ -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

LAND PATTERN DIMENSIONS



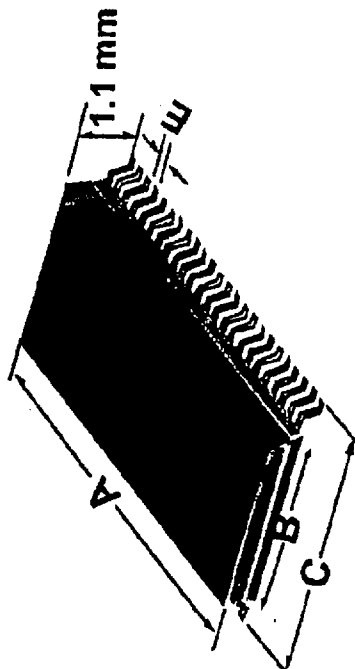
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50	BSC	13.50	BSC
X	.30	.40	.30	.40
e	.50	BSC	.50	BSC
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Slender Way, Santa Clara, CA 95054	
XXX.X	±	PHONE: (408) 727-8118	
XXXX.XX		FAX: (408) 482-8874	
XXXX.XXX		TWC: 910-338-2070	
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE
DRAWN	01/19/93	6.10 mm BODY WIDTH TSSOP	
CHECKED		.50 mm PITCH	
		SIZE	C
		DRAWING No.	PSC-4039
		REV	03
DO NOT SCALE DRAWING			



TVSOP

The Most Compact Double Density Package

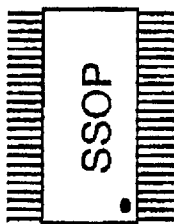


TVSOP Package	Typical Dimensions (in mm)				Area (mm ²)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50



Double Density Packaging

48-Pin



16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

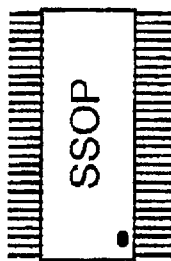


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²



9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin



18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²



14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²



11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm ²)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0