Integrated Device Technology, Inc.

CMOS TRIPLE 8-BIT PALETTEDAC™

IDT 75C458

FEATURES:

- 165/135/125/110/80MHz operating speed
- Fixed pipeline delay: 9 clock cycles
- 50ns read access time
- Integral and differential linearity < 1/2LSB
- Triple 8-bit DACs
- 256 x 24 Dual-Ported Color Palette RAM
- 4 x 24 Dual-Ported Overlay Palette RAM
- Multiplexed TTL pixel and overlay inputs
- RS-343A compatible RGB outputs
- CEMOS™ monolithic construction
- Single 5V power supply
- 84-pin PGA and PLCC packages
- Typical power dissipation: 1000mW
- Pin- and function-compatible with Brooktree BT458
- Military product is compliant to MIL-STD-883, Class B

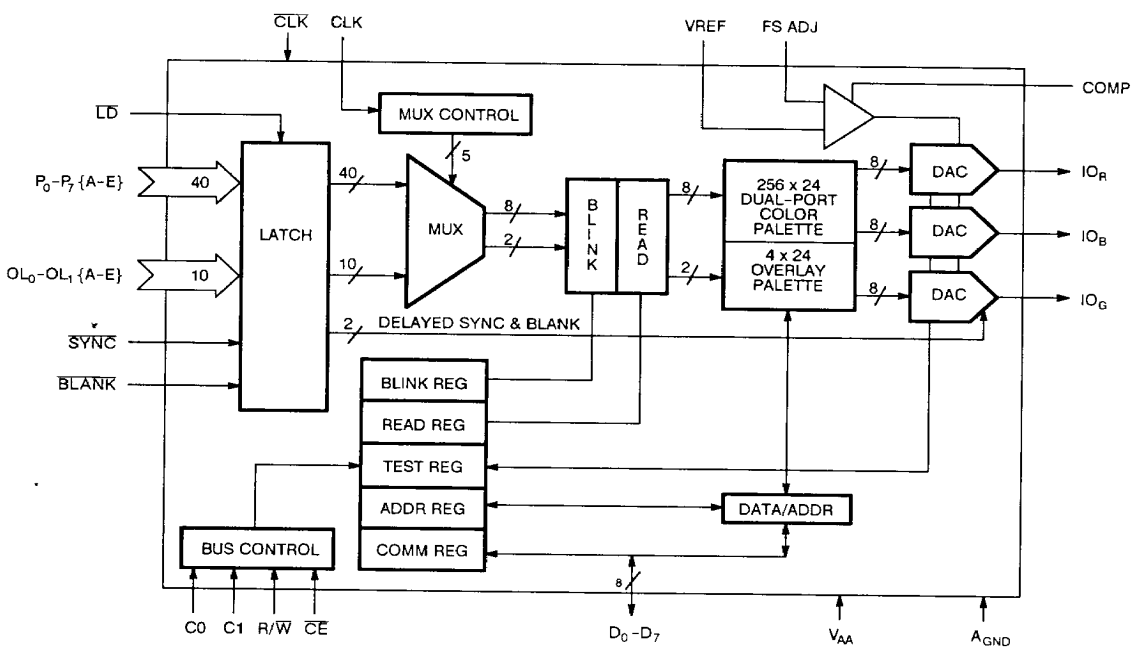
DESCRIPTION:

The IDT75C458 is a triple 8-bit video DAC with on-chip, dual-ported color palette memory. This chip is specifically designed for the display of high resolution color graphics. The architecture eliminates the ECL pixel interface by providing multiple TTL-compatible pixel ports and by multiplexing the pixel data on-chip.

The IDT75C458 supports up to 259 simultaneous colors from a palette of 16.8 million. Other features included on-chip are programmable blink rates, bit plane masking and blinking as well as a color overlay capability. The IDT75C458 generates RS-343A compatible red, green, and blue video outputs which are capable of directly driving a doubly terminated 75Ω coaxial cable.

The IDT75C458 military DACs are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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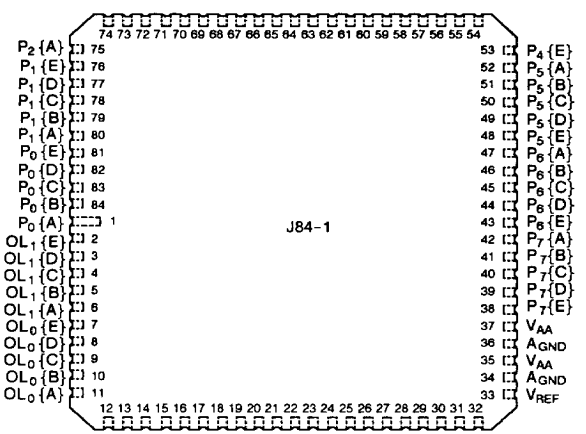
PIN CONFIGURATIONS

	A	B	C	D	E	F	G	H	J	K	L	M
12	COMP	A_{GND}	V_{AA}	$P_7\{D\}$	$P_7\{B\}$	$P_6\{E\}$	$P_6\{C\}$	$P_6\{B\}$	$P_5\{E\}$	$P_5\{C\}$	$P_5\{B\}$	$P_4\{E\}$
11	IO_B	A_{GND}	V_{AA}	$P_7\{E\}$	$P_7\{C\}$	$P_7\{A\}$	$P_6\{D\}$	$P_6\{A\}$	$P_5\{D\}$	$P_5\{A\}$	$P_4\{C\}$	$P_4\{A\}$
10	IO_G	FSADJ	V_{REF}							$P_4\{D\}$	$P_4\{B\}$	$\overline{SYNC}$
9	V_{AA}	IO_R									$\overline{BLANK}$	$\overline{LD}$
8	C1	R/$\overline{W}$									$\overline{CLK}$	CLK
7	V_{AA}	C0									V_{AA}	V_{AA}
6	A_{GND}	A_{GND}					G84-2				$P_3\{E\}$	A_{GND}
5	$\overline{CE}$	D_7									$P_3\{C\}$	$P_3\{D\}$
4	D_6	D_5									$P_3\{A\}$	$P_3\{B\}$
3	D_4	D_2	D_0	△ ALIGNMENT MARK						$P_2\{A\}$	$P_2\{C\}$	$P_2\{E\}$
2	D_3	D_1	$OL_0\{B\}$	$OL_0\{E\}$	$OL_1\{B\}$	$OL_1\{E\}$	$P_0\{B\}$	$P_0\{D\}$	$P_1\{A\}$	$P_1\{D\}$	$P_1\{E\}$	$P_2\{D\}$
1	$OL_0\{A\}$	$OL_0\{C\}$	$OL_0\{D\}$	$OL_1\{A\}$	$OL_1\{C\}$	$OL_1\{D\}$	$P_0\{A\}$	$P_0\{C\}$	$P_0\{E\}$	$P_1\{B\}$	$P_1\{C\}$	$P_2\{B\}$

PGA
TOP VIEW



PLCC
TOP VIEW

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GENERAL INFORMATION:

The IDT75C458 triple 8-bit PaletteDAC is a highly integrated building block which interfaces a relatively low bandwidth frame buffer memory to an analog RS-343A, high bandwidth output. To decrease the frame buffer memory requirements, the IDT75C458 has a color lookup table (dual-port RAM) included on-chip. The basic functional blocks are the microprocessor bus interface, the frame buffer memory interface and multiplexer, a dual-port RAM with one R/W port and one high-speed R/O port and three 8-bit video speed DACs.

MICROPROCESSOR BUS INTERFACE

The IDT75C458 supports a standard microprocessor bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay registers allow color updating without contention with the display refresh process.

The bus interface consists of eight bidirectional data pins, D_0 - D_7, with two control inputs, C0 and C1, a read/write direction input, R/$\overline{W}$, and a clock input, $\overline{CE}$. All data and control information are latched on the falling edge of $\overline{CE}$, as shown in Figure 3. All accesses to the chip are controlled by the data in the address register combined with the control inputs C0, C1 and R/$\overline{W}$, depicted in the Truth Table (Table 1).

An access to a control register requires writing a 4 through 7 into the address register (C0 = C1 = 0) and then writing or reading data to the selected register (C0 = 0, C1 = 1). When accessing the control registers, the address register is not changed, facilitating read-modify-write operations. If an invalid address is loaded into the address register, data written is ignored or invalid data is read out.

It is also possible to access the color palette information. The palette is organized as 256 addresses with 8 bits of red, blue and green information. Additionally, there are four extra addresses assigned to overlay information, yielding a total memory size of 260 x 24.

Access to the palette entries is, again, through the address register. The desired palette address is loaded into the address register, C0 and C1 are modified to point to the color palette or overlay and the information is read or written. In this case, however, an internal counter is used to access the red, green or blue color information. The first color palette or overlay access reads or writes red. The next access is for green, while the third access is for blue. After the third access, the address register is incremented, allowing the reading or writing of the red information of the next palette address. When writing, red and green information is temporarily stored in registers and, during the blue cycle, all 24 bits are written.

The internal counter is reset by an access to the address or any of the control registers. After setting the address register, it is possible to read or write the entire palette without accessing the address register again. Some care is needed; only continuous reads or writes are allowed and it is not possible to switch between the color palette and overlay.

The color palette RAM and overlay registers are dual-ported which allows simultaneous access from the MPU port (D_0 - D_7) and the pixel port (P_0 - P_7 {A-E}). If the pixel port is reading the same palette entry as the MPU is writing, it is possible that the DAC output may be invalid. It is recommended that the palette and overlay entries be updated during the blanking time.

ADDRESS REGISTER DATA	C1	C0	ACCESS
X	0	0	Address Register
$00-$FF	0	1	Color Palette
$00	1	1	Overlay Color 0
$01	1	1	Overlay Color 1
$02	1	1	Overlay Color 2
$03	1	1	Overlay Color 3
$04	1	0	Read Mask Register
$05	1	0	Blink Mask Register
$06	1	0	Command Register
$07	1	0	Test Register

NOTE:

Control input C0 = 1 enables the internal counter which accesses the red, green and blue colors individually and increments the address counter after the blue access. C0 = 0 disables auto-increment of the address register allowing read-modify-write operations.

Table 1. Truth Table for MPU Operations

FRAME BUFFER INTERFACE

The frame buffer interface consists of five 8-bit input ports which correspond to five consecutive pixels. In addition, there are two extra bits per port which may be used for overlay information. To reduce the bandwidth requirements for the pixel data, the IDT75C458 latches 4 or 5 pixels (the multiplex factor is programmable to 4 or 5 by bit 7 of the command register) on each rising edge of $\overline{LD}$. The color and overlay information is internally multiplexed at the pixel clock frequency, CLK, and sequentially output. This arrangement allows pixel data to be transferred at a rate 4 or 5 times slower than the pixel clock. Typically, $\overline{LD}$ is the pixel clock divided by 4 or 5 and is used to clock data out of the frame buffer memory.

As shown in Figure 2, sync, blank, color and overlay information are latched on the rising edge of $\overline{LD}$. Up to 40 bits of color information are input through P_0 - P_7 {A-E} and up to 10 bits of overlay information are input through OL_0 - OL_1 {A-E}. Both sync and blank have separate inputs, $\overline{SYNC}$ and $\overline{BLANK}$, respectively. The IDT75C458 outputs color information on each clock cycle. Four or five pixels are output sequentially, beginning with the {A} information, then the {B} information, until the cycle is completed with the {D} or {E} information. In this configuration, sync and blank times are limited to multiples of four or five clock cycles.

The multiplexing factor, 4:1 or 5:1, is programmable from the command register, bit 7. In the 4:1 mode, the {E} color and overlay inputs are not used and the $\overline{LD}$ clock should be CLOCK divided by 4. The {E} color and overlay inputs must be connected to a valid logic level.

The overlay inputs (OL_0 - OL_1) have the same timing as the pixel inputs (P_0 - P_7). It is possible to use additional bit planes or external logic to control the overlay selection for cursor generation.

INTERNAL MULTIPLEXING

$\overline{LD}$ is typically CLK divided by four or five and it latches color and overlay information on every rising edge, independent of CLK. A digital PLL allows $\overline{LD}$ to be phase independent of CLK. The only restriction is that only one rising edge of $\overline{LD}$ is allowed to occur per four (4:1 multiplexing) or five (5:1 multiplexing) CLK cycles.

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Color Palette

On the rising edge of each CLK cycle, eight bits of color information (P_0 - P_7) and two bits of overlay information (OL_0 - OL_1) for each pixel are processed by the read mask, blink mask and command registers. This information provides the address to the dual-port color palette RAM. Note that P_0 is the LSB when addressing the color palette RAM. The value stored at a selected address determines the displayed color. In this way, 8 bits of information can select from a palette of over 16 million with 256 simultaneous displayed colors (plus 3 overlay colors). Through the use of the control register, individual bit planes may be enabled or disabled for display and/or blinked at one of four blink rates and duty cycles.

The blink timing is based on vertical retrace intervals which are defined by at least 256 $\overline{LD}$ cycles since the last falling edge of $\overline{BLANK}$. The color changes during this normally blanked time.

The processed pixel data is then used to select which color palette entry or overlay register is used to provide color information. Table 2 illustrates the truth table used for color selection.

CR6	OL_1	OL_0	$P_7 - P_0$	PALETTE ENTRY
1	0	0	$00	Color palette entry $00
1	0	0	$01	Color palette entry $01
	.			.
	.			.
	.			.
1	0	0	$FF	Color palette entry $FF
0	0	0	$xx	Overlay color 0
x	0	1	$xx	Overlay color 1
x	1	0	$xx	Overlay color 2
x	1	1	$xx	Overlay color 3

NOTE:
CR6 is bit 6 of the Command Register.

Table 2. Palette and Overlay Select

Video Generation, DACs

On every CLK cycle, the selected 24 bits of color information (8 bits each of red, green and blue) from the Color Palette RAM are presented to the three 8-bit D/A converters. The IDT75C458 uses a 5 x 3 segmented approach where the five MSBs of the input data are decoded into a parallel "Thermometer" code which produces thirty two "course" output levels. The remaining three LSBs of input data drive three binary weighted current switches with a total contribution of one-thirty second of full scale. The MSB and LSB currents are summed at the output to produce 256 levels.

The $\overline{SYNC}$ and $\overline{BLANK}$ inputs are pipelined to maintained synchronization with the pixel data. Both inputs drive appropriately weighted current switches which are summed at the output of the DACs to produce the specific output levels required by RS-343, as shown in Figure 3. Note that the sync information is only available at the IO_G (green) output and that the input data to the DAC sums with the sync current. Table 3 details the output levels associated with $\overline{SYNC}$, $\overline{BLANK}$ and data.

Monitor Interface

The analog outputs of the IDT75C458 are high-impedance current sources which are capable of directly driving a doubly terminated 75Ω coaxial cable to standard video levels. A typical output circuit is shown in Figure 4.

Description	S	B	DAC data	IO_G(mA)	IO_R, IO_B (mA)
WHITE	1	1	$FF	26.67	19.05
DATA	1	1	data	data + 9.05	data + 1.44
DATA & SYNC	0	1	data	data + 1.44	data + 1.44
BLACK	1	1	$0	9.05	1.44
BLACK & SYNC	0	1	$0	1.44	1.44
BLANK	1	0	X	7.62	0
SYNC	0	0	X	0	0

NOTE:
Typical values with full scale IOG = 26.67mA. RSET = 523Ω, VREF = 1.235V. S is $\overline{SYNC}$, B is $\overline{BLANK}$.

Table 3. Video Output Truth Table

IO_R, IO_B		IO_G	
mA	V	mA	V
19.05	0.714	26.67	1.000
•	•	•	•
•	•	•	•
•	•	•	•
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

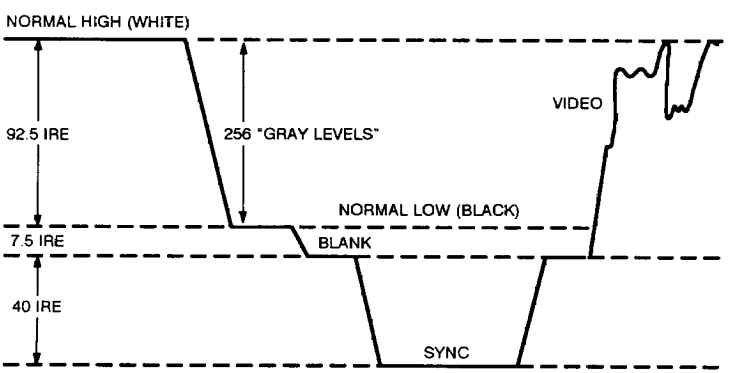

Figure 1. Composite Video Output Waveform

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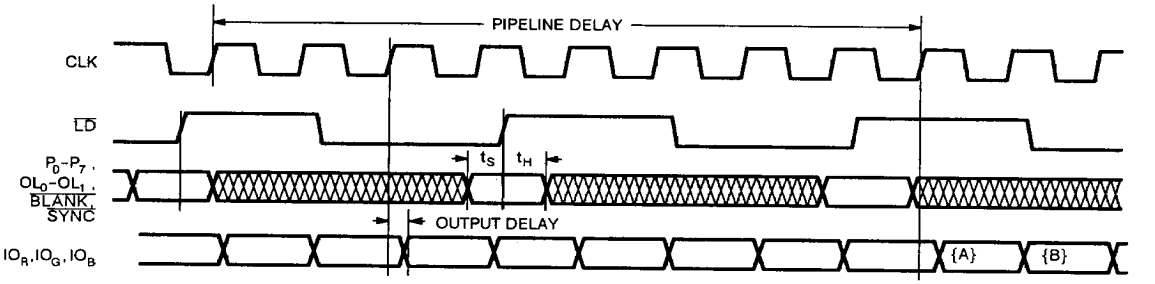

Figure 2. Pixel Timing

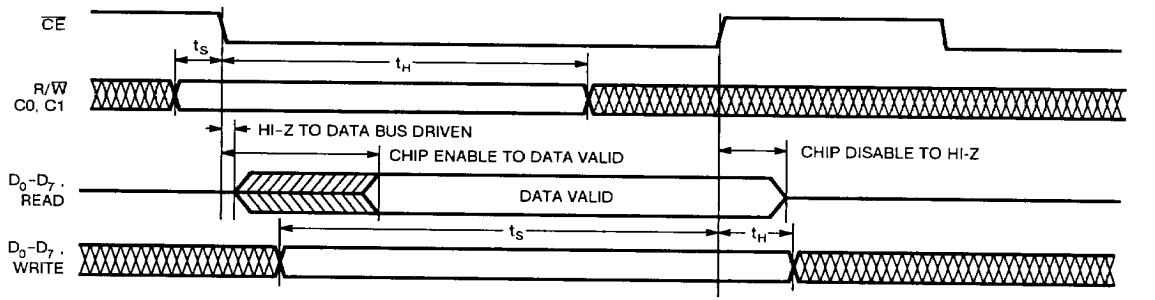

Figure 3. Data Bus Timing

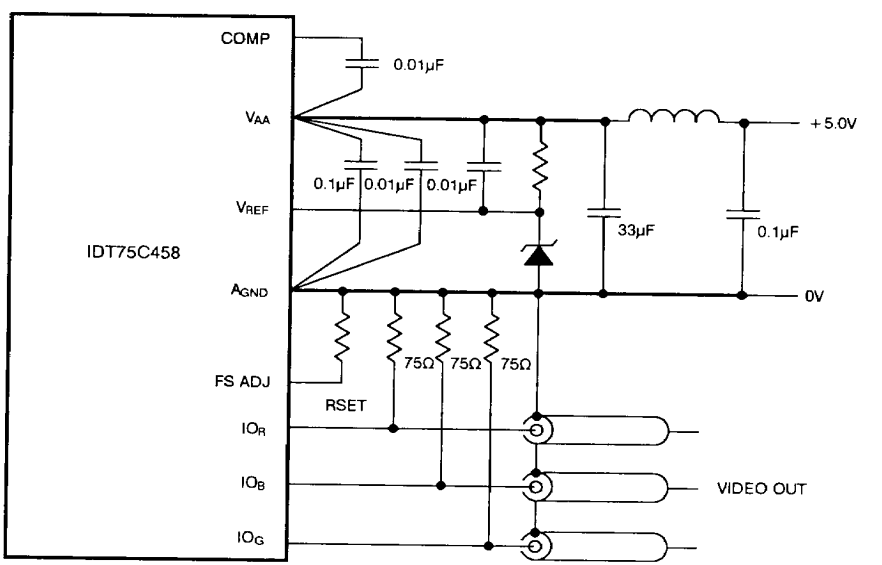

Figure 4. Typical Application

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PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
DATA BUS	
D_0 - D_7	8-bit, bidirectional data bus. Data is input and output over this bus and the flow is controlled by R/$\overline{W}$ and $\overline{CE}$. D_7 is the most significant bit.
$\overline{CE}$	Chip Enable input. The chip is enabled when this control pin is LOW. During a write cycle (R/$\overline{W}$ LOW), the data present on D_0 - D_7 is internally latched on the LOW-to-HIGH transition of this pin.
R/$\overline{W}$	Read/Write Control input. The Read/Write input is latched on the HIGH-to-LOW transition of $\overline{CE}$ and determines the direction of the bidirectional data bus D_0 - D_7. If R/$\overline{W}$ is HIGH during the falling edge of $\overline{CE}$, a read cycle occurs. If R/$\overline{W}$ is LOW during the falling edge of $\overline{CE}$, a write cycle occurs and, additionally, D_0 - D_7 are latched on the rising edge of $\overline{CE}$.
C0, C1	Register Control inputs. C0 and C1 determine which register or palette entry is accessed during a read or write cycle. These inputs are latched on the HIGH-to-LOW transition of $\overline{CE}$.
PIXEL	
CLK, $\overline{CLK}$	Pixel Clock inputs. These inputs are differential and may be driven by ECL operating from a +5V supply. The clock frequency is normally the system pixel clock rate.
$\overline{LD}$	Load Clock input. The Load Clock is normally CLK divided by 4 or 5 (determined by the Control Register, bit 7). The pixel data, P_0 - P_7 {A-E} and OL_0 - OL_1{A-E}, $\overline{BLANK}$ and $\overline{SYNC}$ are internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
P_0 - P_7 {A-E}	Pixel Input Data. These inputs provide the address input to the color palette RAM. The data stored at a particular address is the color output by the DAC. Four or five consecutive pixels, as determined by bit 7 in the Command Register, are internally latched on the LOW-to-HIGH transition of $\overline{LD}$. The pixels are output sequentially, first {A} then {B}. After all four or five pixels have been output, the cycle repeats. Unused inputs must be connected to a valid logic level.
OL_0 - OL_1{A-E}	Pixel Overlay Inputs. The Overlay inputs have the same timing as P_0 - P_7 and select between either the color palette or the overlay palette. When the overlay palette is selected, the pixel information P_0 - P_7 {A-E} is ignored. Bit 6 of the command register determines if Overlay = 0 displays overlay color 0 or the color palette entry. See Table 2 for details.
$\overline{BLANK}$	Composite Blank Input. A LOW on this input forces the analog outputs (IO_R, IO_G, IO_B) to the blanking level. The $\overline{BLANK}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$. This input overrides all other pixel information.
$\overline{SYNC}$	Composite Sync Input. A LOW on this input subtracts approximately 7mA from the IO_G analog output and overrides no other pixel information. For the correct SYNC level, this input should be LOW only when $\overline{BLANK}$ is also LOW. The $\overline{SYNC}$ input is internally latched on the LOW-to-HIGH transition of $\overline{LD}$.
ANALOG	
A_{GND}	Analog Ground Power Supply, 0V.
V_{AA}	Analog Power Supply, 5V.
V_{REF}	Voltage Reference Input, 1.235V. This input supplies a reference voltage for the DAC circuitry. Care must be taken to correctly decouple this voltage because noise on this pin will couple directly to the DAC outputs.
FS ADJ	Full-Scale Adjust Input. The current flowing from this pin to A_{GND} is directly proportional to the full-scale analog output current. Normally, a resistor is connected between this pin and A_{GND}. The voltage on this pin is approximately equal to V_{REF}. The relationship between the full-scale output current and RSET is: IO_G (mA) = 11.294 x V_{REF} (V)/RSET (KΩ) IO_R, IO_B (mA) = 8.067 x V_{REF} (V)/RSET (KΩ)
IO_G, IO_R, IO_B	Green, Red and Blue DAC current outputs.
COMP	Compensation Input. This pin provides the ability to compensate the internal reference operational amplifier.

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INTERNAL REGISTERS

Command Register

The Command Register is accessed by reading or writing with the Address Register = $06, C0 = 0 and C1 = 1 (see Table 1). It provides control over multiplexing and blink rate selection. The Command Register may be read or written at any time. CR7 (Command Register bit 7) corresponds to D7 (Data Bus bit 7).

CR0 — OL_0 display enable. This bit is ANDed internally with the data from OL_0 prior to the palette selection. If CR0 is LOW, the internal OL_0 bits are set LOW allowing only overlay colors 0 and 2 to be selected.

CR1 — OL_1 display enable. This bit is ANDed internally with the data from OL_1 prior to the palette selection. If CR1 is LOW, the internal OL_1 bits are set LOW allowing only overlay colors 0 and 1 to be selected.

CR2 — OL_0 blink enable. If this bit is set HIGH, the OL_0 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR0 must be set HIGH for this function.

CR3 — OL_1 blink enable. If this bit is set HIGH, the OL_1 bit is internally switched between the value input and 0 at the rate specified by the CR4 and CR5 bits. CR1 must be set HIGH for this function.

CR4, CR5 — Blink Rate Select. These bits select blink rates based on Vertical Sync cycles, defined as more than 256 $\overline{LD}$ cycles during BLANK.

CR6 — Color Palette RAM enable. This bit specifies whether to use the Color Palette or the Overlay Palette when $OL_0 = OL_1 =$ LOW.

CR7 — Multiplex Select. This bit selects between 4:1 (CR7 = 0) or 5:1 (CR7 = 1) multiplexing. When using 4:1 multiplexing, the {E} inputs are never used and must be connected to a valid logic level.

Read Mask Register

The Read Mask Register is accessed by reading or writing with the Address Register = $04, C0 = 0 and C1 = 1 (see Table 1). It internally ANDs the pixel information with a bit from the register before the color palette selection, effectively enabling (HIGH) or disabling (LOW) the entire pixel plane. The Read Mask Register may be read or written at any time. RMR7 (Read Mask Register bit 7) corresponds to D7 (Data Bus bit 7).

Blink Mask Register

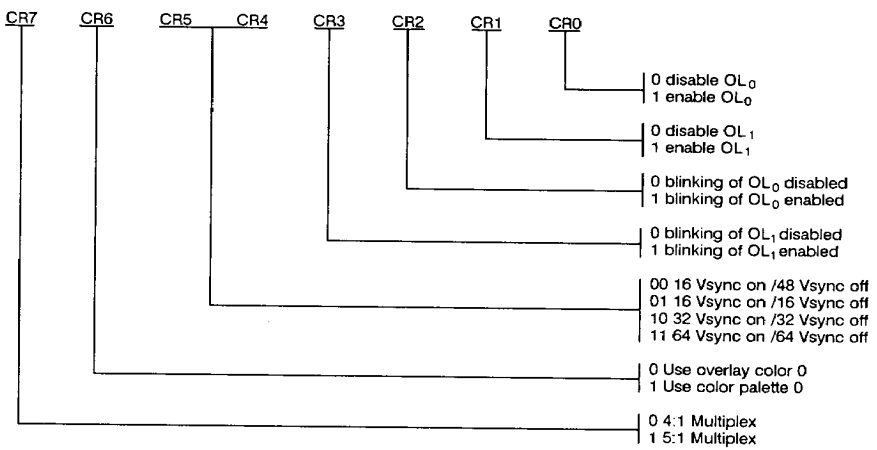
The Blink Mask Register is accessed by reading or writing with the Address Register = $05, C0 = 0 and C1 = 1 (see Table 1). Each register bit causes the corresponding pixel bit (P_0 - P_7) to internally switch between the input value and 0 at the blink rate specified in the Command Register. For this function to work, the corresponding enable bit in the Read Mask Register must be set HIGH. The Blink Mask Register may be read or written at any time. BMR7 (Blink Mask Register bit 7) corresponds to D_7 (Data Bus bit 7).

Test Register

The Test Register is accessed by reading or writing with the Address Register = $07, C0 = 0 and C1 = 1 (see Table 1). This register allows the MPU to read the 24 input bits of the DACs. The register bits are defined below.

TR7-TR4	Read data (one nibble of red, blue or green)
TR3	Upper (LOW) or Lower (HIGH) nibble select
TR2	Blue enable
TR1	Green enable
TR0	Red enable

The desired DAC is selected by setting only one color enable bit (D_0 - D_2) HIGH and the upper or lower nibble is selected with D_3. After this write operation, a subsequent read yields the DAC data on D_7 - D_4 and the previously written enable data on D_0 - D_3. For a correct read, pixel and overlay data must remain constant for the entire MPU read cycle. When $\overline{BLANK}$ is asserted, the Test Register information D_7 - D_4 will be forced to zero. TR7 (Test Register bit 7) corresponds to D_7 (Data Bus bit 7).



COMMAND REGISTER DESIGNATIONS

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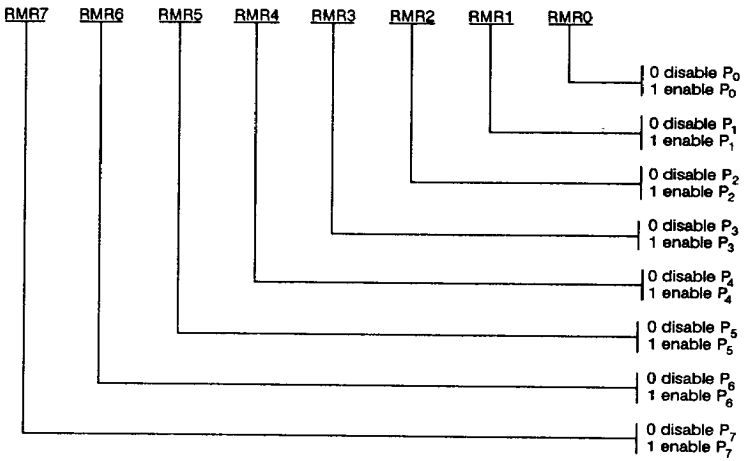
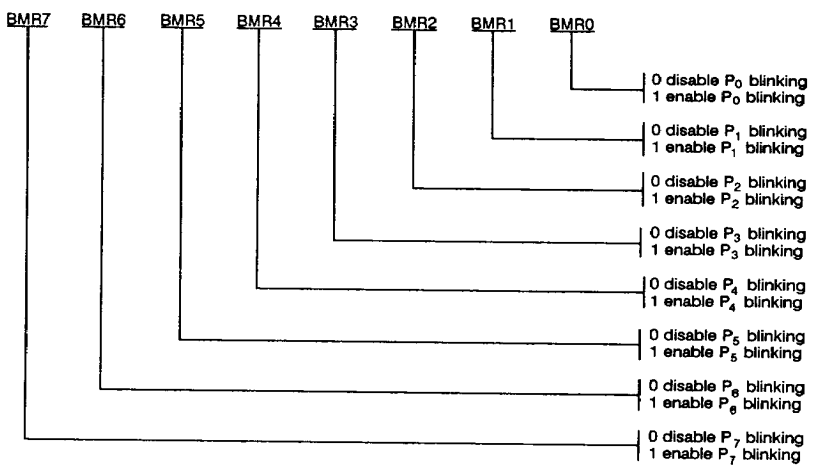


READ MASK REGISTER DESIGNATIONS



BLINK MASK REGISTER DESIGNATIONS

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{AA}	Measured to A_{GND}	-0.5 to +7.0	V
INPUT VOLTAGE			
Applied Voltage(2)	Measured to A_{GND}	-0.5V to V_{AA} + 0.5	V
OUTPUT			
Applied Voltage(2)	Measured to A_{GND}	-0.5V to V_{AA} + 0.5	V
Applied Current(2,3,4)	Externally forced	-1.0 to +6.0	mA
Short Circuit Duration	Single output High to A_{GND}	Indefinite	–
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{AA}	Power Supply	Measured to A_{GND}	4.75	5.0	5.25	V
I_{AA}	Power Supply Current	V_{AA} = Typ., Static	–	200	–	mA
V_{IH} (1)	Input Voltage HIGH		2.0	–	V_{AA} +0.5	V
V_{IL} (1)	Input Voltage LOW		A_{GND} -0.5	–	0.8	V
V_{CIH}	Clock Input Voltage HIGH		V_{AA} -1.0	–	V_{AA} +0.5	V
V_{CIL}	Clock Input Voltage LOW		A_{GND} -0.5	–	V_{AA} -1.6	V
I_{IH}	Input Current HIGH	V_{IN} = 2.4V	–	–	1	µA
I_{IL}	Input Current LOW	V_{IN} = 0.4V	–	–	-1	µA
V_{OH}	Output Voltage HIGH	V_{AA} = Min., I_{OH} = -800µA	2.4	–	–	V
V_{OL}	Output Voltage LOW	V_{AA} = Min., I_{OL} = 6.4mA	–	–	0.4	V
I_{OZ}	Output 3-State Current		–	–	10	µA

NOTE:
1. All digital inputs except CLK and $\overline{CLK}$.

AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0V, V_{IH} = 3.0V, rise/fall time < 5ns
CLK Inputs, V_{IH} = V_{AA} -1.0V, V_{IL} = V_{AA} -1.6V, rise/fall time < 2ns
Timing reference points at 50% of signal swing
Analog Output Load ≤ 10pF
D_0 – D_7 Output Load ≤ 50pF

		IDT75C458-165(1)		IDT75C458-135(1)		IDT75C458-125		IDT75C458-110		IDT75C458-80		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	165	–	135	–	125	–	110	–	80	MHz
F_{LD}	$\overline{LD}$ Clock Frequency	–	41	–	34	–	32	–	28	–	20	MHz
t_{CS}	Control Set-up Time; C0, C1, R/$\overline{W}$	0	–	0	–	0	–	0	–	0	–	ns
t_{CH}	Control Hold Time; C0, C1, R/$\overline{W}$	15	–	15	–	15	–	15	–	15	–	ns
t_{CEH}	$\overline{CE}$ HIGH Time	20	–	20	–	25	–	25	–	25	–	ns
t_{CEL}	$\overline{CE}$ LOW Time	30	–	30	–	50	–	50	–	50	–	ns
t_{CEZO}	$\overline{CE}$ to Data Bus Driven	10	–	10	–	10	–	10	–	10	–	ns
t_{CED}	$\overline{CE}$ to Data Valid	–	30	–	30	–	50	–	50	–	75	ns
t_{CEOZ}	$\overline{CE}$ to Data Bus HI-Z	–	15	–	15	–	15	–	15	–	15	ns
t_{WDS}	Write Data Set-up Time	30	–	30	–	35	–	35	–	50	–	ns
t_{WDH}	Write Data Hold Time	0	–	0	–	0	–	0	–	0	–	ns
t_{CLKCY}	Clock Cycle Time	6	–	7.4	–	8	–	9	–	12	–	ns
t_{CLKPL}	Clock Pulse Width LOW	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{CLKPH}	Clock Pulse Width HIGH	2.8	–	3.0	–	3.2	–	4	–	5	–	ns
t_{LDCY}	$\overline{LD}$ Cycle Time	24	–	29	–	31	–	35	–	50	–	ns
t_{LDPH}	$\overline{LD}$ Pulse Width HIGH	10	–	12	–	13	–	15	–	20	–	ns
t_{LDPL}	$\overline{LD}$ Pulse Width LOW	10	–	12	–	13	–	15	–	20	–	ns
t_{PS}	Pixel Data Set-up Time	2	–	3	–	3	–	3	–	4	–	ns
t_{PH}	Pixel Data Hold Time	1	–	2	–	2	–	2	–	2	–	ns
t_{AAD}	Dynamic Supply Current Commercial Temp.	–	450	–	425	–	400	–	380	–	360	mA
t_{AAD}	Dynamic Supply Current Military Temp.	–	–	–	–	–	450	–	430	–	410	mA

NOTE:
1. 165 and 135 MHz specified over commercial temperature only.

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ANALOG OUTPUT DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Res	Resolution			–	8	–	bits
I_{LSB}	LSB Current Size			–	69.1	–	µA
L_I			1 LSB VERSION	–	1/2	±1	LSB
			1/2 LSB VERSION	–	1/4	±1/2	LSB
L_D			1 LSB VERSION	–	1/2	±1	LSB
			1/2 LSB VERSION	–	1/4	±1/2	LSB
V_{OC}	Output Compliance Voltage			-1.0	–	1.2	V
R_{AOUT}(2)	Output Impedance				50		kΩ
C_{AOUT}(2)	Output Capacitance	f = 1MHz, I_{OUT} = 0mA			8	12	pF
I_{REF}	V_{REF} Input Current				10		µA
E_M	Matching Error (DAC to DAC)			–	2	5	%
PSRR	Power Supply Rejection Ratio			–	50	–	dB
I_W(1)	White Current	Measured to Blank		17.69	19.05	20.40	mA
I_W(1)	White Current	Measured to Black		16.74	17.62	18.50	mA
I_B(1)	Black Current	Measured to Blank		0.95	1.44	1.90	mA
I_{BLANK}	Blank Current IO_R, IO_B			0	5	50	µA
I_{BLANK}(1)	Blank Current IO_G			6.29	7.62	8.96	mA
I_{SYNC}	Sync Current IO_G			0	5	50	µA

NOTE:
1. R_{SET} = 523Ω, V_{REF} = 1.235V
2. This parameter is guaranteed but not tested in production.

ANALOG OUTPUT AC ELECTRICAL CHARACTERISTICS

Following conditions apply unless otherwise specified:
T_A = 0°C to +70°C (Commercial Temperature Range)
T_A = -55°C to +125°C (Military Temperature Range)
V_{AA} = 5.0V ±5%
TTL Inputs, V_{IL} = 0.8V, V_{IH} = 2.0V, rise/fall time < 5ns
CLK Inputs, V_{IH} = V_{AA} -1.0V, V_{IL} = V_{AA} -1.6V, rise/fall time < 2ns
Timing reference points at 50% of signal swing

		IDT75C458-165(3)			IDT75C458-135(3)			IDT75C458-125			IDT75C458-110			IDT75C458-80			
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
F_{CLK}	Clock Frequency	–	–	165	–	–	135	–	–	125	–	–	110	–	–	80	MHz
t_{VD}	Video Output Delay Time	–	15	–	–	15	–	–	15	–	–	15	–	–	15	–	ns
t_{VT}	Video Output Transition Time	–	1.5	–	–	1.7	–	–	1.8	–	–	2	–	–	2	–	ns
t_S	Video Output Skew(1)	–	0	<2	–	0	<2	–	0	<2	–	0	<2	–	0	<2	ns
t_{SI}(2)	Video Output Settling Time	–	6	–	–	7	–	–	8	–	–	8	–	–	12	–	ns
FT(2)	Clock and Data Feedthrough	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
G_E(2)	Glitch Energy	–	50	–	–	50	–	–	50	–	–	50	–	–	50	–	pV-s
CT(2)	Crosstalk, DAC to DAC	–	100	–	–	100	–	–	100	–	–	100	–	–	100	–	pV-s
t_{VP}	Pipeline Delay	9	–	9	9	–	9	9	–	9	9	–	9	9	–	9	clock

NOTES:
1. C_L = 10pF, 10%-90% points
2. This parameter is guaranteed but not tested in production.
3. 165 and 135 MHz specified over commercial temperature range only.

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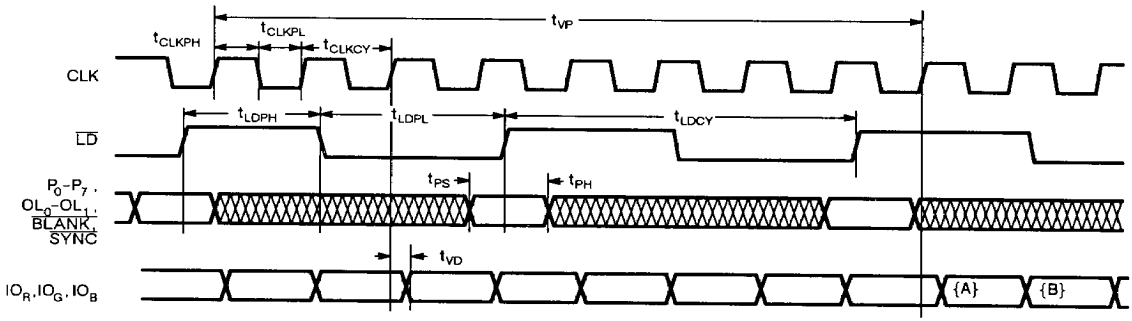

Figure 5. Video I/O Timing Diagram

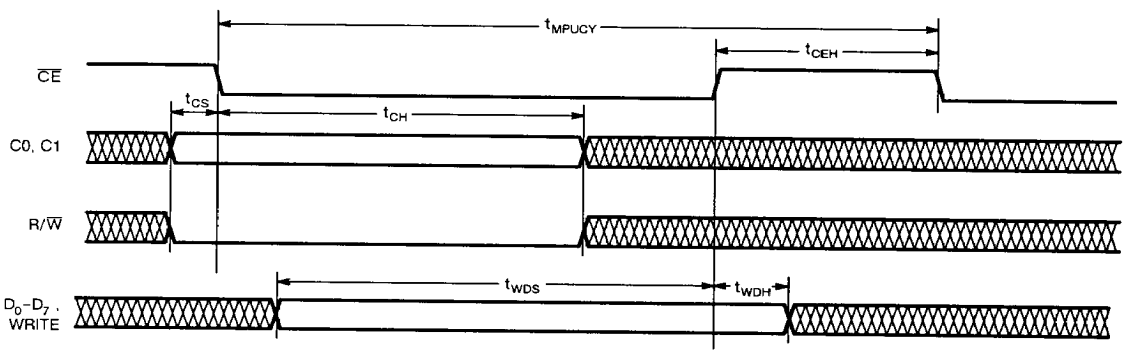

Figure 6. MPU WRITE Timing Diagram

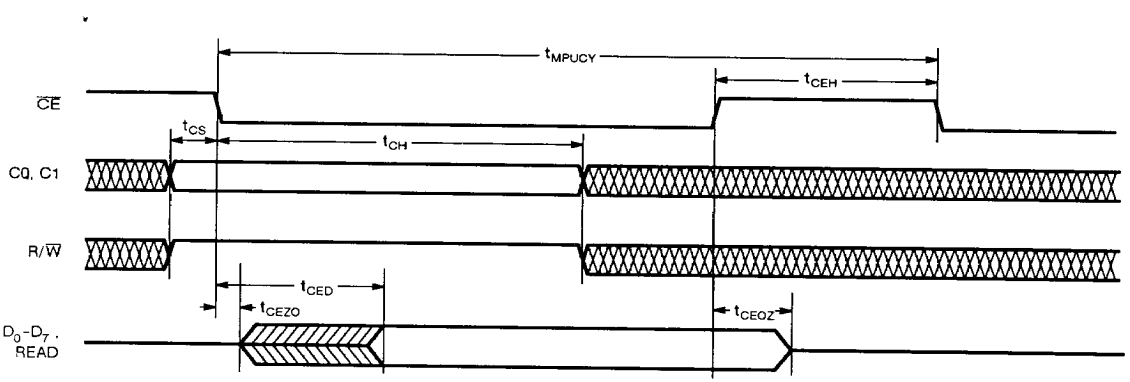

Figure 7. MPU READ Timing Diagram

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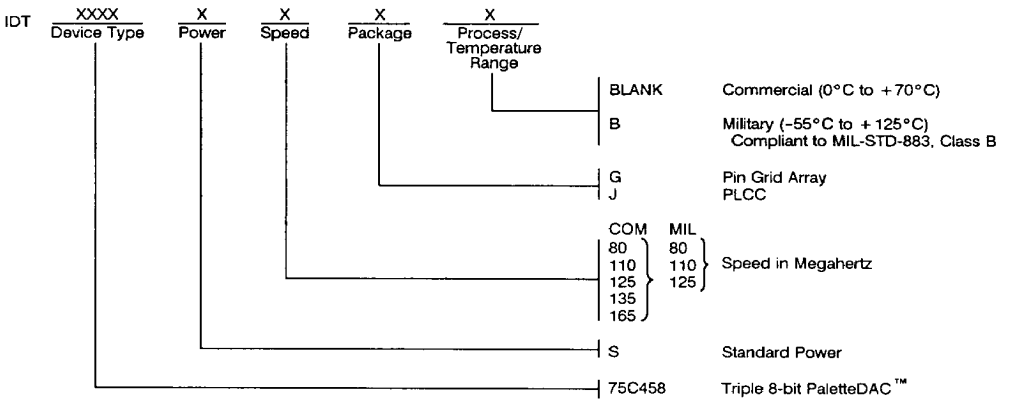

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