Integrated Device Technology, Inc.

PHY-TC for 25.6 Mbps ATM Networks

PRELIMINARY
IDT77101

FEATURES

- Performs the PHY-Transmission Convergence (TC) Sublayer functions for 25.6 Mpbs ATM Networks
- Interfaces to Industry-Standard Physical Media Dependent (PMD) devices
- UTOPIA Level 1 Interface
- LED Interface for Status Signalling
- Supports UTP Category 3 (CAT 3) Physical Media
- Low-Power CMOS
- 2-Cell Transmit & Receive FIFOs
- 64-pin TQFP and STQFP Package (10 x 10mm)

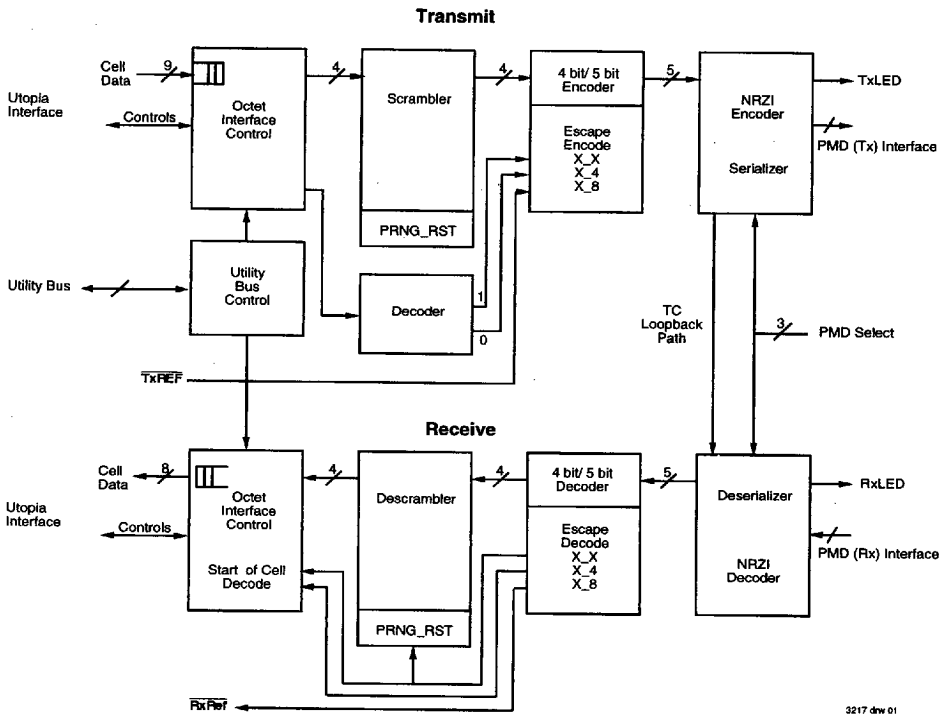
DESCRIPTION

The IDT77101 is a member of IDT's family of products developed to support Asynchronous Transfer Mode (ATM) data communications and networking. The IDT77101 provides the Transmission Convergence (TC) sublayer portion of a 25.6 Mbps ATM PHY suitable for ATM networks using Unshielded Twisted Pair (UTP) Category 3 (or better) wiring. The UTOPIA interface provides standardized control and communications to other components, such as Segmentation and Reassembly (SAR) controilers and ATM switches.

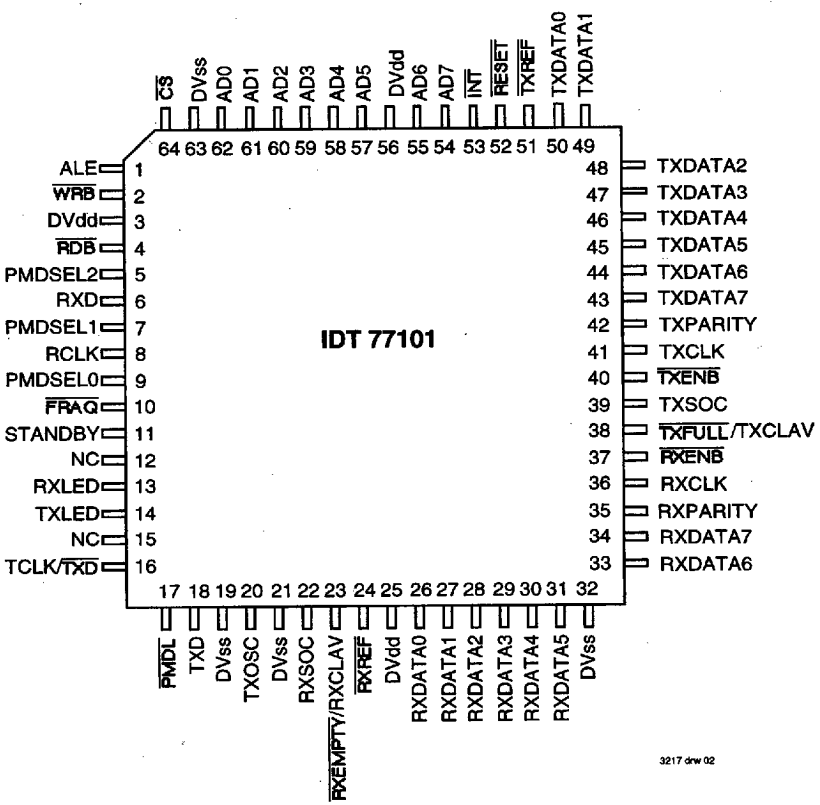
The IDT77101 supports glue-less interfaces to several PMD devices, such as those from IBM™, Seeq™ and Texas Instruments™.

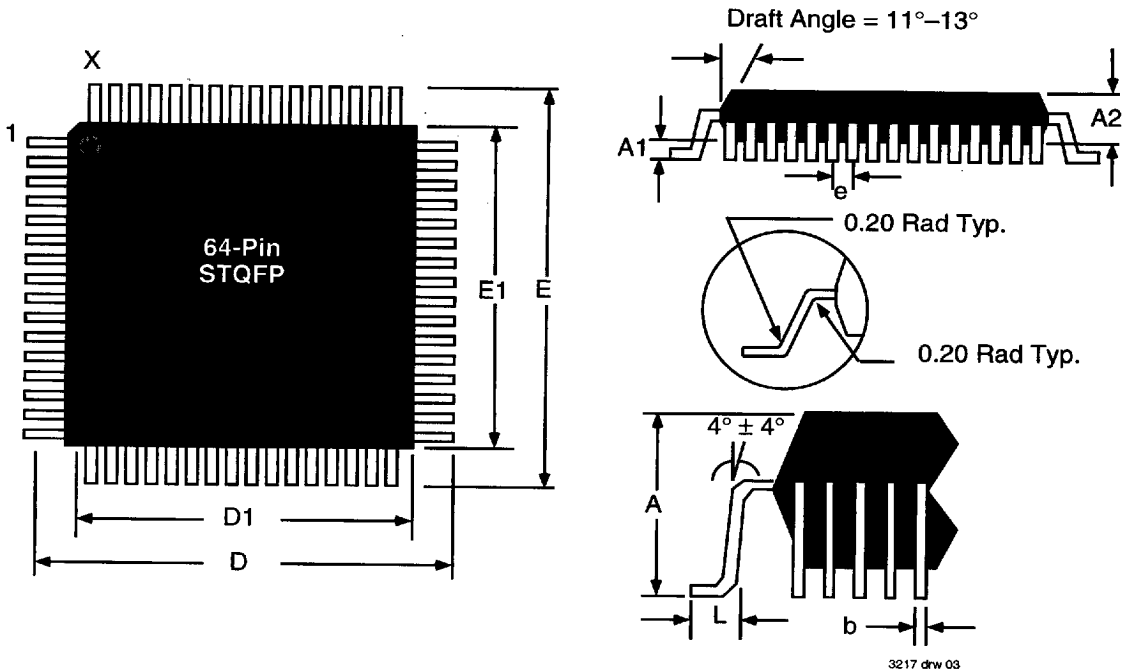
The IDT77101 is fabricated using IDT's state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





DIMENSIONS

64-PIN STQFP WITH 10MM BODY

DImension Letter	Tolerance (mm)	Dimension (mm)
A	Max.	1.60
A1	±.05	0.10
A2	±.05	1.45
D	±.10	12.00
D1	±.10	10.00
E	±.10	12.00
E1	±.10	10.00
L	±15	0.60
e	Basic	0.50
b	.05	0.22

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to DVss	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 3139 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
DVdd	Supply Voltage	4.5	5.0	5.5	V
DVss	Ground Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial: DVdd = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Min.	Typ.	Max	Unit
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	V
I_{DD1}(3)	Active Power Supply Current	—	—	140	mA
I_{DD2}(4)	Average Standby Current	—	—	10	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ DVdd.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ DVdd.
3. Tested at f = 32MHz with outputs unloaded.
4. All inputs are CMOS level.

CAPACITANCE (T_A = +25°C, f = 32MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(1)	Input Capacitance	VIN = 0V	10	pF
C_{OUT}(1)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 3139 tbl 05

1. Characterized values, not currently tested.

PIN DESCRIPTION

Pin	Name	I/O	Interfaces to	Description
1	ALE	I	Utility bus	Address Latch Enable signal. The falling edge of ALE is used to latch the address on AD[7:0].
2	$\overline{WRB}$	I	Utility bus	Write Byte Enable (active low).
3	DVdd	-	Digital power plane	
4	$\overline{RDB}$	I	Utility bus	Read Byte Enable (active low).
5	PMDSEL2	I	Hardwired to board	High order bit of PMDSelect[2:0]. Used to select which PMD is being used in conjunction with 77101. See "PMD Interfacing" section within Functional Description.
6	RxD	I	PMD	Receive serial data stream.
7	PMDSEL1	I	Hardwired to board	Mid order bit of PMDSelect[2:0]. Used to select which PMD is being used in conjunction with 77101. See "PMD Interfacing" section within Functional Description.
8	RCLK	I	PMD	Receive clock derived from received data stream.
9	PMDSEL0	I	Hardwired to board	Low order bit of PMDSelect[2:0]. Used to select which PMD is being used in conjunction with 77101. See "PMD Interfacing" section within Functional Description.
10	$\overline{FrAq}$	O	PMD	Frequency Acquisition signal (active low). If equal to 1, Normal Operation; if equal to 0, Frequency Acquisition mode.
11	Standby	O	PMD	Standby signal used to place PMD in standby mode.
12	NC	-		
13	Rx LED	O	LED	LED driver output for indicating receive status.
14	Tx LED	O	LED	LED driver output for indicating transmit status.
15	NC	-		
16	TCLK/$\overline{TxD}$	O	PMD	Transmit data clock or inverse transmit data; selection is determined via PMD SEL[2:0].
17	$\overline{PMDL}$	O	PMD	PMD Loopback control signal (active low).
18	TxD	O	PMD	Transmit serial data stream.
19	DVss	-	Digital ground plane	
20	TxOsc	I	OSC/PMD	32MHz input from either an external clock oscillator or derived clock from receive data (RCLK).
21	DVss	-	Digital ground plane	
22	RxSOC	O	UTOPIA bus	Receive Start of Cell signal.
23	$\overline{RxEmpty}$/RxClav	O	UTOPIA bus	Receive Empty (active low; byte mode) or Receive Cell Available (active high; cell mode).
24	$\overline{RxRef}$	O	UTOPIA bus	Receive Reference signal (active low). This pin is driven in response to a received X_8 command nibble. Assertion duration is programmable to 1,2,4 or 8 clocks, as set via register 0x03, bits 3, 4.
25	DVdd	-	Digital power plane	
26	RxData0	O	UTOPIA bus	Receive data bit 0.
27	RxData1	O	UTOPIA bus	Receive data bit 1.
28	RxData2	O	UTOPIA bus	Receive data bit 2.
29	RxData3	O	UTOPIA bus	Receive data bit 3.
30	RxData4	O	UTOPIA bus	Receive data bit 4.
31	RxData5	O	UTOPIA bus	Receive data bit 5.
32	DVss	-	Digital ground plane	

PIN DISCRIPTION (Continued)

Pin	Name	I/O	Interfaces to	Description
33	RxData6	O	UTOPIA bus	Receive data bit 6.
34	RxData7	O	UTOPIA bus	Receive data bit 7.
35	RxParity	O	UTOPIA bus	Parity bit for RxData[7:0].
36	RxClk	I	UTOPIA bus	Receive data path synchronization clock.
37	$\overline{\text{RxEnb}}$	I	UTOPIA bus	Receive Enable signal (active low).
38	$\overline{\text{TxFull}}$/TxCLAV	O	UTOPIA bus	Transmit Full (active low; byte mode) or Transmit Cell Available (active high; cell mode).
39	TxSOC	I	UTOPIA bus	Transmit Start of Cell signal.
40	$\overline{\text{TxEnb}}$	I	UTOPIA bus	Transmit Enable signal (active low).
41	TxClk	I	UTOPIA bus	Transmit data path synchronization clock.
42	TxParity	I	UTOPIA bus	Parity bit for TxData[7:0].
43	TxData7	I	UTOPIA bus	Transmit data bit 7.
44	TxData6	I	UTOPIA bus	Transmit data bit 6.
45	TxData5	I	UTOPIA bus	Transmit data bit 5.
46	TxData4	I	UTOPIA bus	Transmit data bit 4.
47	TxData3	I	UTOPIA bus	Transmit data bit 3.
48	TxData2	I	UTOPIA bus	Transmit data bit 2.
49	TxData1	I	UTOPIA bus	Transmit data bit 1.
50	TxData0	I	UTOPIA bus	Transmit data bit 0.
51	$\overline{\text{TxRef}}$	I	UTOPIA bus	Transmit Reference signal input (active low). Assertion of this pin stimulates insertion of command byte X_8 into transmit data stream to PMD.
				See UTOPIA description elsewhere in this datasheet.
52	$\overline{\text{Reset}}$	I	control	77101 reset signal (active low).
53	$\overline{\text{INT}}$	O	control	Interrupt signal (active low).
54	AD7	I/O	Utility bus	Address/Data bit 7.
55	AD6	I/O	Utility bus	Address/Data bit 6.
56	DVdd	-	Digital power plane	
57	AD5	I/O	Utility Bus	Address/Data bit 5.
58	AD4	I/O	Utility Bus	Address/Data bit 4.
59	AD3	I/O	Utility Bus	Address/Data bit 3.
60	AD2	I/O	Utility Bus	Address/Data bit 2.
61	AD1	I/O	Utility Bus	Address/Data bit 1.
62	AD0	I/O	Utility Bus	Address/Data bit 0.
63	DVss	-	Digital ground plane	
64	$\overline{\text{CS}}$	I	control	Utility Buss Chip select (active low).

FUNCTIONAL DESCRIPTION

25MB/S ATM COMMUNICATIONS STANDARD

The IDT77101 implements the Transmission Convergence Sublayer for 25.6Mbps ATM network communications. A complete 25.6Mbps ATM PHY is implemented using the IDT77101 and a "PMD" (Physical Medium Dependent Sublayer) device.

The physical layer is divided into a Physical Media Dependent sub layer (PMD) and Transmission Convergence (TC) sub layer. The PMD sub layer defines the specifications for the transmitter, receiver, timing recovery, and channel that allow connection to transmission media conforming to TIA/EIA 568 (UTP Category 3). The TC sub layer defines the line coding, scrambling, data framing and synchronization, and is described below.

• TRANSMISSION CONVERGENCE (TC) SUB LAYER

Introduction

Under control of a Segmentation and Reassembly (SAR) system or other, the 25.6Mbps ATM PHY accepts a 53-byte ATM cell, scrambles the data, appends a command byte to the beginning of the cell, and encodes the entire 53 bytes before transmission. These data transformations ensure that the signal is evenly distributed across the frequency spectrum. In addition, the serialized bit stream is NRZI coded. An 8kHz timing sync pulse may be used for isochronous communications.

Data Structure and Framing

Each 53-byte ATM cell is preceded with a command byte. This byte is distinguished by an escape symbol followed by one of 17 encoded symbols. Together, this byte forms one of seventeen possible command bytes. Three command bytes are defined:

1. **X_X** (read: 'escape' symbol followed by another 'escape'): Start-of-cell with scrambler/descrambler reset.
2. **X_4** ('escape' followed by '4'): Start-of-cell without scrambler/descrambler reset.
3. **X_8** ('escape' followed by '8'): 8kHz timing marker. This command byte is generated when the 8kHz sync pulse is detected, and has priority over all line activity (data or command bytes). It is transmitted immediately when the sync pulse is detected. When this occurs during a cell transmission, the data transfer is temporarily interrupted on an octet boundary, and the X_8 command byte is inserted. This condition is the only allowed interrupt in an otherwise contiguous transfer.

FUNCTIONAL BLOCK DIAGRAM (Continued)

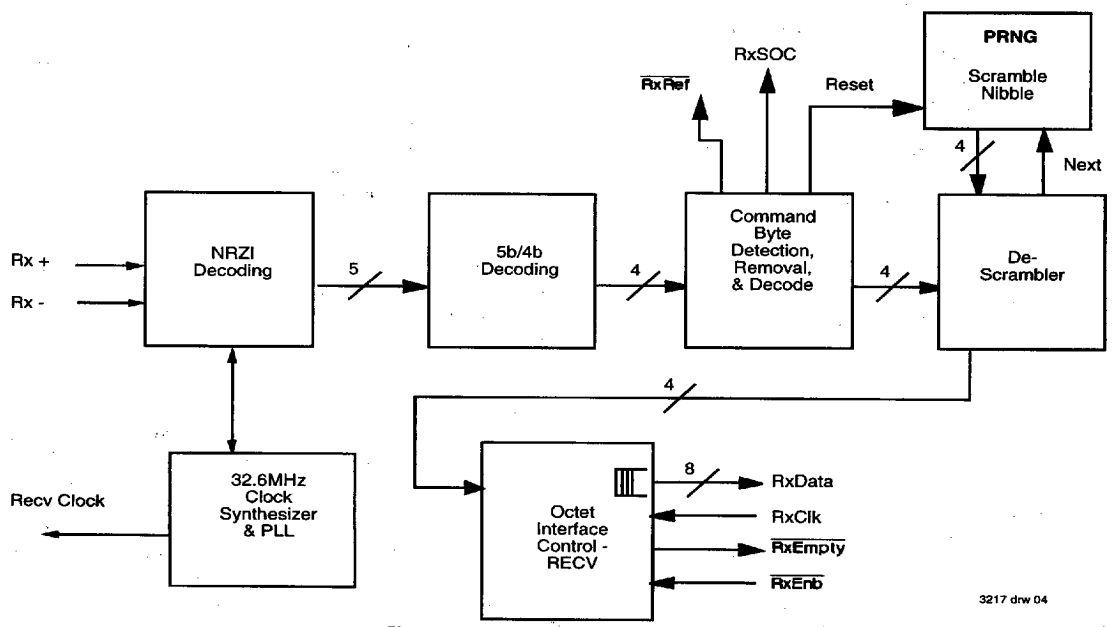


Figure 1. 25 Mbps TC Transmit Block Diagram

Below is an illustration of the cell structure and command byte usage:

{X_X} {53-byte ATM cell} {X_4} {53-byte ATM {X_8} cell} ...

In the above example, the first ATM cell is preceded by the X_X start-of-cell command byte which resets both the transmitter-scrambler and receiver-descrambler pseudo-random nibble generators (PRNG) to their initial states. The following cell illustrates the insertion of a start-of-cell command without scrambler/descrambler reset. During this cell's transmission, an 8kHz timing sync pulse triggers insertion of the X_8 8kHz timing marker command byte.

Transmission Description

Refer to the "25Mbps PHY transmit Block Diagram" on the previous page. Cell transmission begins with the Octet Interface Control:

- The SAR (or other upstream system) confirms that the PHY may accept transmit data by polling the $\overline{\text{TxFull}}$ flag. If this signal is 'high' (PHY xmit buffer not full), the SAR then asserts $\overline{\text{TxEnb}}$.
- The SAR then asserts TxSOC, puts the first byte on the TxData bus, and toggles TxClk. TxSOC is then deasserted.
- Following bytes are transmitted by putting them onto the TxData bus, and toggling TxClk.
- 4-bit data (MSB first) is asynchronously (to TxClk) sent to the 'Scrambler'.

The 'Scrambler' takes each nibble of data and exclusive-ORs them against the 4 high order bits (X(t), X(t-1), X(t-2), X(t-3)) of a 10 bit pseudo-random nibble generator (PRNG). Its function is to provide the appropriate frequency distribution for the signal across the line.

The PRNG is clocked every time a nibble is processed, regardless of whether the processed nibble is part of a data or command byte. Note however that only data nibbles are scrambled. The entire command byte (X_C) is NOT scrambled before it's encoded (see diagram for illustration). The PRNG is based upon the following polynomial:

$$X^{10} + X^7 + 1$$

With this polynomial, the four output data bits (D3, D2, D1, D0) will be generated from the following equations:

D3 = d3 xor X(t-3)
D2 = d2 xor X(t-2)
D1 = d1 xor X(t-1)
D0 = d0 xor X(t)

The following nibble is scrambled with X(t+4), X(t+3), X(t+2), and X(t+1).

A scrambler lock between the transmitter and receiver occurs each time an X_X command is sent. An X_X command is initiated only at the beginning of a cell transfer after the PRNG has cycled through all of its states (210 - 1 = 1023 states). The first valid ATM data cell transmitted after power on will also be accompanied with an X_X command byte. Each time an X_X command byte is sent, the first nibble after the last escape (X) nibble is XOR'd with 1111b (PRNG = 3FFx).

Because a timing marker command (X_8) may occur at any time, the possibility of a reset PRNG start-of-cell command and a timing marker command occurring consecutively does exist (eg. X_X_X_8). In this case, the detection of the last two consecutive escape (X) nibbles will cause the PRNG to reset to its initial 3FFx state. Therefore, the PRNG is clocked only after the first nibble of the second consecutive escape pair.

Once the data nibbles have been scrambled using the PRNG, the nibbles are further encoded using a 4b/5b process. The 4b/5b scheme ensures that an appropriate number of signal transitions occur on the line. A total of 17 5-bit symbols are used to represent the 16 4-bit data nibbles and the one escape (X) nibble. The table below lists the 4-bit data with their corresponding 5-bit symbols:

Data	Symbol
0000	10101
0100	00111
1000	10010
1100	10111

Data	Symbol
0001	01001
0101	01101
1001	11001
1101	11101

Data	Symbol
0010	01010
0110	01110
1010	11010
1110	11110

Data	Symbol
0011	01011
0111	01111
1011	11011
1111	11111

ESC(X) = 00010

3217 drw 05

This encode/decode implementation has several very desirable properties. Among them is the fact that the output symbol bits can be represented by a set of relatively simple logic equations. The other main advantage is that it contains transmission properties that are desirable, which include:

- Transition averages over 3 per 5 signal elements;
- Encode/Decode is not affected by the incorporation of the scrambler;
- Run length is limited to <= 5;
- Disparity never exceeds +/- 1.

On the receiver, the decoder determines from the received symbols whether a timing marker command (X_8) or a start-of-cell command was sent (X_X or X_4). If a start-of-cell command is detected, the next 53 bytes received are decoded and forwarded to the descrambler. (See Recv Block Diagram, Figure 2).

The output of the 4b/5b encoder provides serial data to the NRZI encoder. The NRZI code transitions the wire voltage each time a '1' bit is sent. This, together with the previous encoding schemes guarantees that long run lengths of either '0' or '1's are prevented. Each symbol is shifted out with its most significant bit sent first.

Receiver Description

On the receiving end, the inverse occurs. The data is NRZI decoded before each symbol is reassembled. The symbols are then sent to the 5b/4b decoder, followed by the Command Byte Interpreter, De-Scrambler, and finally the UTOPIA interface to the outside world.

UTOPIA INTERFACE

The 'UTOPIA' (Universal Test & Operations PHY Interface for ATM) interface is used as the data path interface between the IDT77101 PHY and other system elements such as the Segmentation and Reassembly (SAR) device, or switching systems.

Overview

Cell data is transferred via separate Transmit and Receive synchronizing clocks which are controlled by the SAR or other system components. Transfer of data is synchronized at the cell level through the use of a Start of Cell signal. This signal is asserted when the data transfer path contains the first byte of a cell.

Since the PHY layer uses external clocks for data transfer synchronization, flow control signals are provided to allow both the external device and the PHY to throttle the data transfer rate.

Receive data is transferred when the $\overline{\text{RxEnb}}$ signal is asserted by an external device. The PHY also provides an $\overline{\text{RxEmpty}}$ signal to indicate that no valid data is ready for transfer out of the PHY. This signal is active if another read would cause a PHY buffer underflow. Along with $\overline{\text{RxEmpty}}$, RxClav (Receive Cell Available) indicates that a complete cell has been received and is ready for transfer. Likewise, Transmit data is also transferred using similar controls and handshake signals.

The Status and Control interface for the IDT77101 PHY is provided to allow control of several functions such as Header Error Control (HEC) processing, diagnostics, and error notification/management.

FUNCTIONAL BLOCK DIAGRAM (Continued)

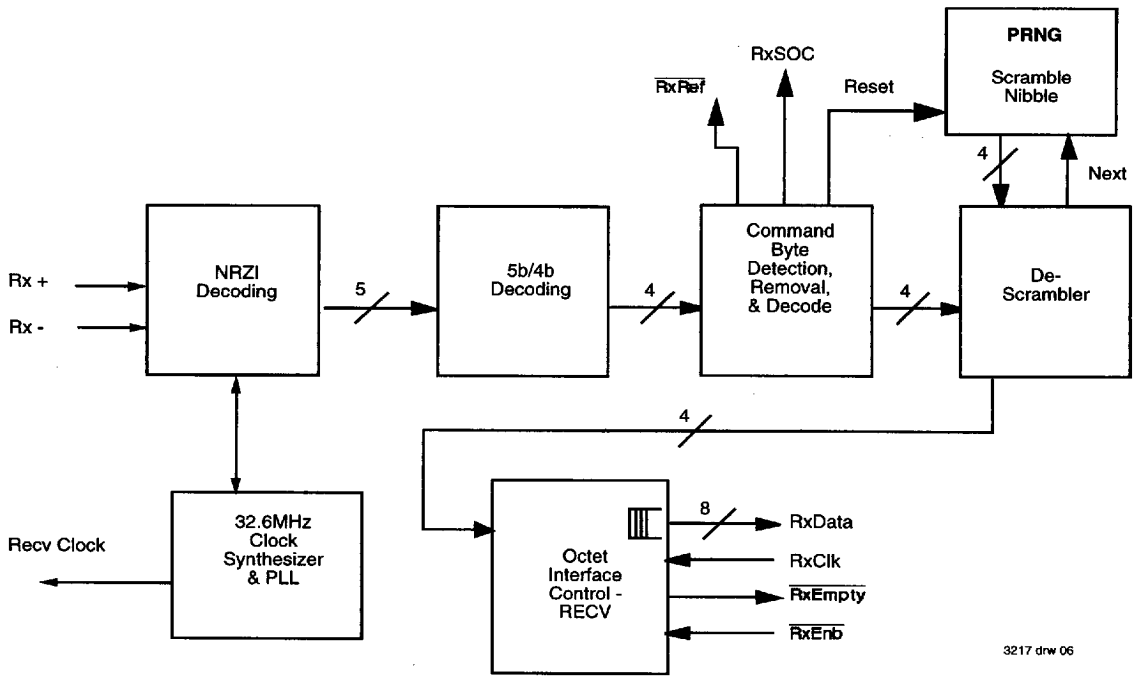


Figure 2. 25 Mbps TC Receive Block Diagram

• TRANSMIT INTERFACE

Signals

TxData[7..0]—Transmit Data. TxData[7] is the MSB.
TxSOC—Start Of Cell. Active high signal to be asserted when TxData contains the first byte of the cell.
$\overline{\text{TxENB}}$—Enable. Active low signal to be asserted when TxData contains valid data.
$\overline{\text{TxFull}}$/TxClav—Full/Cell Available. For octet (byte)-level handshake control, $\overline{\text{TxFull}}$ is an active low signal asserted by PHY at least 4 cycles before it is no longer able to accept transmit data. For cell-level flow control, the assertion of TxClav indicates that the PHY is capable of receiving an entire 53-byte cell.
TxClk—Transmit Clock. Data transfer clock to synchronize data transfers on TxData to PHY.
$\overline{\text{TxRef}}$—Transmit Reference. 8kHz input for synchroniztion.

Operation and Timing

Cell transmission is controlled by the external system and is synchronized to TxClk. All signals are sampled on the rising edge of TxClk. Data is transferred to the PHY using one of two handshake methods: Octet (byte)-Level Handshake, Cell-Level Handshake. Handshake method is selected via setting of the Register 0x00 Bit 1.

Octet (byte)-level handshake operates as follows:

- The PHY indicates it can accept data by deasserting $\overline{\text{TxFull}}$. (The PHY may assert $\overline{\text{TxFull}}$ at any time which will indicate that no more than 4 write cycles (bytes) will be accepted.)
- If $\overline{\text{TxEnb}}$ is asserted by the external system, data is clocked into the PHY on the rising edge of TxClk. Note that $\overline{\text{TxEnb}}$ *must be deasserted within 4 cycles of* $\overline{\textit{TxFull}}$ *assertion, and must not be reasserted until after* $\overline{\textit{TxFull}}$ *deassertion is detected.*

The "cell-level" handshake is the same as the byte-level except that TxClav is only asserted when the PHY can accept transfer of an entire 53-byte cell. $\overline{\text{TxEnb}}$ must remain asserted until at least the last byte of the cell. If TxClav remains asserted at the end of the cell, $\overline{\text{TxEnb}}$ may also remain asserted, which allows uninterrupted cell transfer from the external system to the PHY.

• RECEIVE INTERFACE

Signals

RxData[7..0]—Receive Data. RxData[7] is the MSB.
RxSOC—Start Of Cell. Active high signal asserted by PHY when RxData contains first byte of a cell.
$\overline{\text{RxEnb}}$—Enable. Active low signal asserted externally to indicate that RxData and RxSOC will be sampled at the start of the next cycle.
$\overline{\text{RxEmpty}}$/RxClav—Empty/Cell Available. For octet (byte)-level flow control, $\overline{\text{RxEmpty}}$ is an active low signal asserted by the PHY to indicate that in the *current* cycle there is no valid data available for delivery over RxData[7:0]. For cell-level flow control, RxClav indicates that an entire cell is available for immediate transfer over RxData. In both cases, this signal indicates cycles where there is valid data on RxData/RxSOC.
RxClk—Receive Clock. Transfer clock provided externally to synchronize transfers on RxData.
$\overline{\text{RxRef}}$—Receive Reference. 8kHz output derived from incoming data stream.

Operation and Timing

Received-cell transfer from the PHY is controlled externally and is synchronized to RxClk Since data transfer is dependent upon an external system, a 4-cell FIFO is provided to buffer the receive data path. As with the transmit path, the receive data and controls are sampled on the rising edge of RxClk.

Octet (byte)-level handshake operates as follows:

- The PHY indicates it can accept data by deasserting $\overline{\text{TxFull}}$. (The PHY may assert $\overline{\text{TxFull}}$ at any time which will indicate that no more than 4 write cycles (bytes) will be accepted.)
- If $\overline{\text{TxEnb}}$ is asserted by the external system, data is clocked into the PHY on the rising edge of TxClk. Note that $\overline{\text{TxEnb}}$ *must be deasserted within 4 cycles of* $\overline{\textit{TxFull}}$ *assertion, and must not be reasserted until after* $\overline{\textit{TxFull}}$

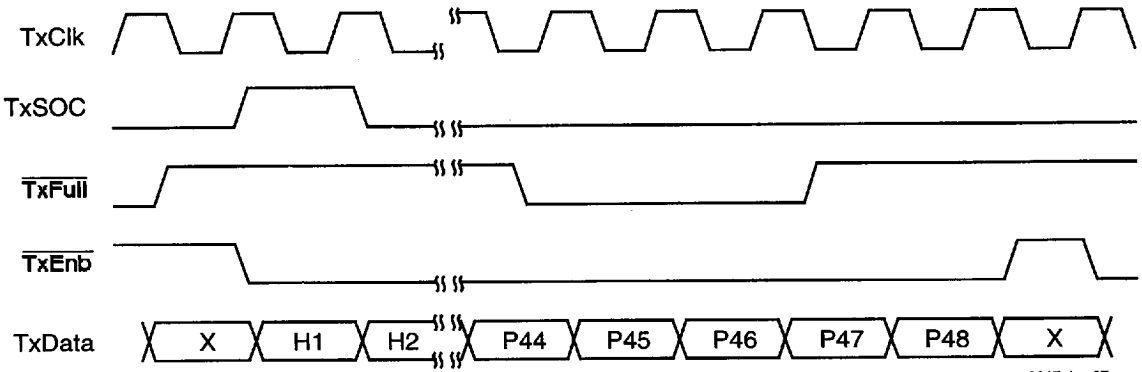


Figure 3. Transmit Waveform for Octet (byte)-Level Handshake

3217 drw 07

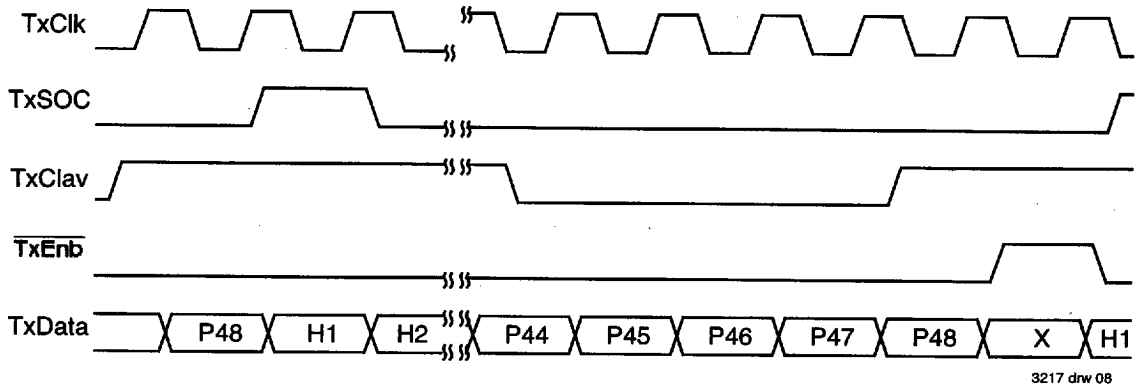
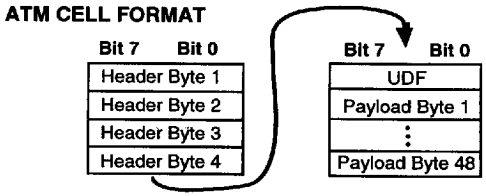


Figure 4. Transmit Waveform for Cell-Level Handshake

TRANSMIT HEC BYTE CALCULATION AND INSERTION

Byte #5 of each ATM cell, the HEC (Header Error Control) is calculated automatically across the first 4 bytes of the cell header. Depending upon the setting of bit field 5 of register, 0x03, Bit 5 this byte is then either inserted as a replacement of the fifth byte transferred to the PHY by the external system, or the cell is transmitted as received. A second operating mode provides for insertion of "Bad" HEC codes which may aid in communication diagnostics.



UDF = User Defined Field (or HEC)

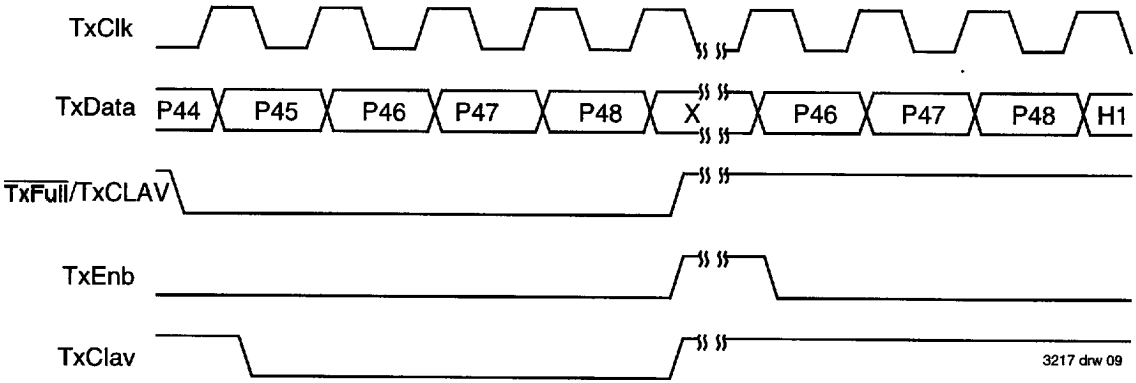


Figure 5. TxFull/TxClav Waveform

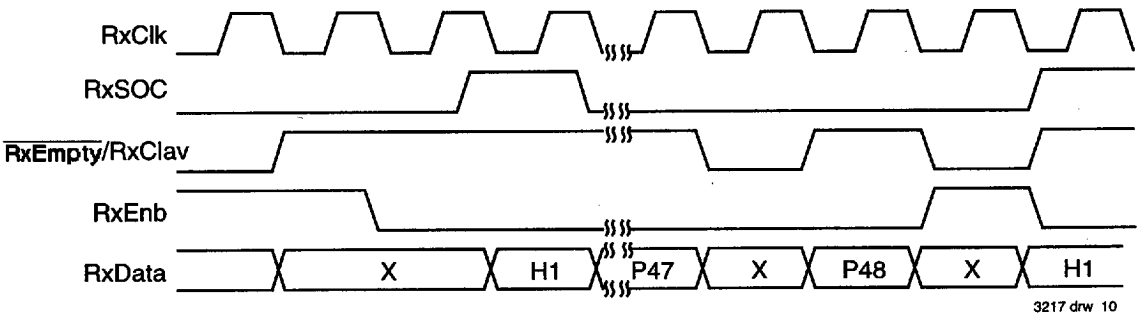


Figure 6. Receive Waveform for Cell or Octet-Level Handshake

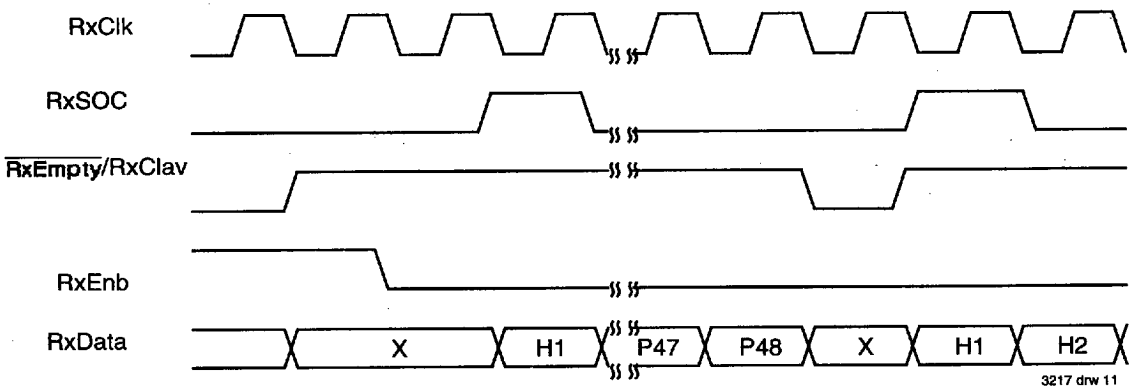


Figure 7. RxEmpty/RxClav Waveform

FUNCTIONAL DESCRIPTION (Continued)

UTILITY BUS

The Utility Bus is a byte-wide interface that provides access to the registers within the IDT77101. These registers are used to select desired operating characteristics and functions, and to communicate status to external systems.

The Utility Bus is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the Address Latch Enable (ALE) signal.

The Utility Bus interface is comprised of the following pins:

AD[7:0]
ALE
$\overline{CS}$
$\overline{RDB}$
$\overline{WRB}$

NOTE: Register 0x01 is an interrupt status register which should always be read prior to any other register reads: Register 0x01 is always cleared during any register read operation.

Read Operation

Refer to the Utility Bus waveforms on Pages 19, 20. A register read is performed as follows:

1. Initial condition:
   - $\overline{RDB}$, $\overline{WRB}$, $\overline{CS}$ not asserted (logic 1)
   - ALE set at logic 0
2. Set up register address:
   - set ALE to logic 1;
   - assert $\overline{CS}$ by setting to logic 0;
   - place desired register address on AD[7:0]
   - latch this address by setting ALE to logic 0.
3. Read register data:
   - Remove register address data from AD[7:0]
   - assert $\overline{RDB}$ by setting to logic 0
   - wait minimum pulse width time (see AC specifications)

Write Operation

A register write is performed as described below:

1. Initial condition:
   - $\overline{RDB}$, $\overline{WRB}$, $\overline{CS}$ not asserted (logic 1)
   - ALE set at logic 0
2. Set up register address:
   - set ALE to logic 1;
   - assert $\overline{CS}$ by setting to logic 0;
   - place desired register address on AD[7:0]
   - latch this address by setting ALE to logic 0.
3. Write data:
   - place data on AD[7:0]
   - Assert $\overline{WRB}$ (logic 0) for minimum time (according to timing specification); reset $\overline{WRB}$ to logic 1 to complete register write cycle.

INTERRUPT OPERATIONS

The IDT77101 provides a variety of selectable interrupt and signalling conditions which are useful both during 'normal' operation, and as diagnostic aids. Refer to the Status and Control Register List on Page 15.

Overall interrupt control is provided via register 0x00, bit 0. When this bit is cleared (set to 0), interrupt signalling is prevented. Additional interrupt signal control is provided by register 0x00, bit 5. When this bit is set (=1), receive cell errors will be flagged via interrupt signalling and all other interrupt conditions are masked. These errors include:

- Bad receive HEC
- Short (fewer than 53 bytes) cells
- Received cell symbol error

Normal interrupt operations are performed by setting register 0x00 bit-0 = 1, and bit-5 = 0. $\overline{INT}$ (pin 53) will go to a low state when an interrupt condition is detected. The external system should then interrogate the 77101 to determine which one (or more) conditions caused this flag, and reset the interrupt for further occurrences. This is accomplished by reading register 0x01. Decoding the bits in this byte will tell which error condition caused the interrupt. Reading register 0x01 also:

- clears all interrupt status bits
- resets $\overline{INT}$

This leaves the interrupt system ready to signal an alarm for further problems.

PMD INTERFACING

The IDT77101 directly supports seamless connection to PMD components manufactured by IBM™, Texas Instruments™, and Seeq Technology™. Since there are some differences in control signals from between these manufacturers products, 3 PMD Select pins are provided as inputs to the 77101 to make the appropriate selection. These have been provided as discrete pins (rather than as a register-selection) to support hardwire selection in individual applications. (See Page 21).

PMD Select[2:0]	2	1	0	
	0	0	0	IBM™
	0	0	1	TI™
	0	1	0	Seeq™
	0	1	1	Reserved
	1	X	X	Reserved

LED CONTROL AND SIGNALLING

The LED outputs, pins 13 and 14 provide bi-directional LED drive capability of 10mA. As an example, the RxLED pin's output is described in the truth table:

State	Pin Voltage
Cells being received	Low
Cells not being received	High

As illustrated in the following drawing (Figure 8), this could be connected to provide for a two-LED condition indicator. These could also be different colors to provide simple status indication at a glance.

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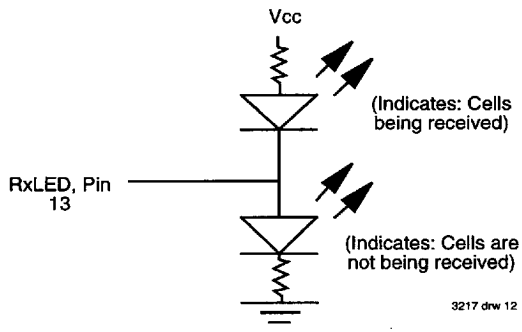

Figure 8.

TxLED Truth Table (Pin 14)

STATE	PIN VOLTAGE
CELLS BEING TRANSMITTED	LOW
CELLS NOT BEING TRANSMITTED	HIGH

DIAGNOSTIC FUNCTIONS

1. LOOPBACK

There are three loopback modes supported by the 77101. Two are implemented directly within the device; one operates a control signal, used by a PMD (which supports loopback). The loopback mode is controlled via Register 0x02, bits 1 and 0:

0x02	Bit 1	Bit 0	
	0	0	Normal operating mode
	0	1	PMD Loopback
	1	0	TC Loopback
	1	1	Line Loopback

Normal Mode

This mode, Figure 9, supports normal operating conditions: data to be transmitted is transferred to the TC, where it is queued and formatted for transmission by the PMD. Receive data from the PMD is decoded along with its clock for transfer to the receiving "upstream system".

TC Loopback

As Figure 10 illustrates below, this loopback mode provides a connection within the TC between transmit and receive data. Note that while this mode is operating, no data is forwarded to or received from the PMD.

Line Loopback

Figure 11 might also be called "remote loopback" since it provides for a means to test the overall system, including the line. Since this mode will probably be entered under direction from another system (at a remote location), receive data is also decoded and transferred to the upstream system to allow it to listen for commands. A common example would be a command asking the upstream system to direct the TC to leave this loopback state, and resume normal operations.

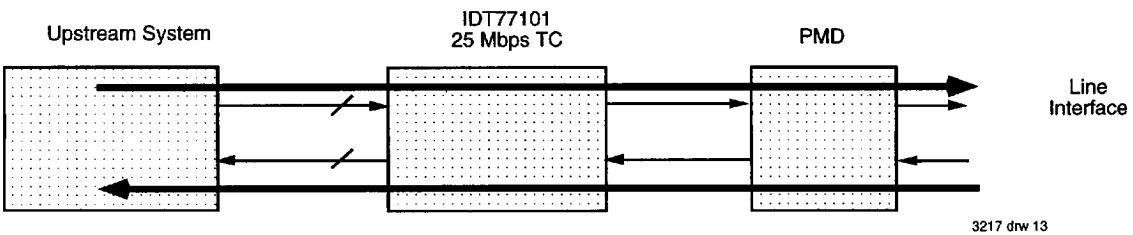

Figure 9. Normal Mode

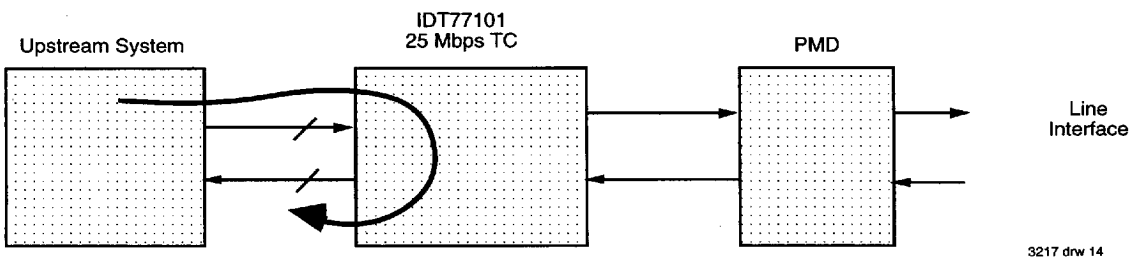

Figure 10. TC Loopback

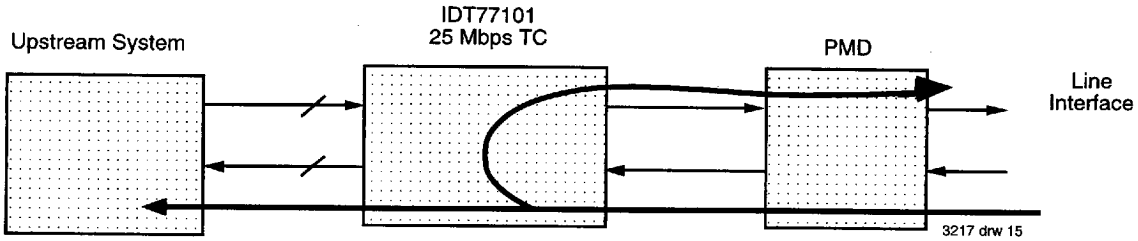

Figure 11. Line Loopback

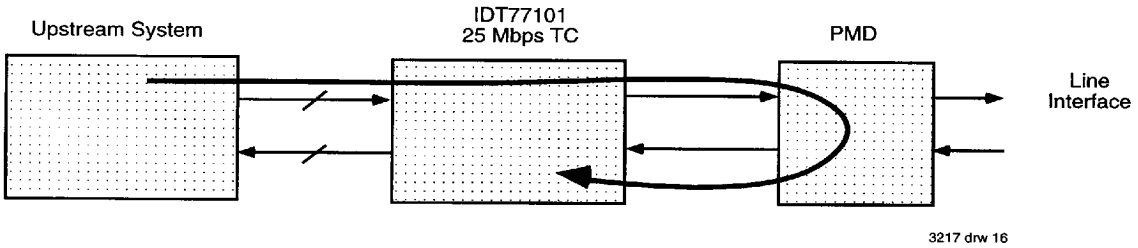

Figure 12. PMD Loopback

PMD Loopback

In Figure 12, the mode is supported only if loopback is a supported feature of the particular PMD. Entering this mode via register 0x02 causes $\overline{\text{PMDL}}$ (pin 17) to go to its logic low state which is used to signal the PMD to enter this mode.

To enter a loopback mode, it may be preferable to allow the internal transmit and/or receive FIFOs to empty themselves of valid data, and then enter loopback mode. The way to accommodate this depends upon which UTOPIA mode is in use, either cell or byte mode. Below is a suggested series of operations for entering and exiting loopback modes:

Entering Loopback (Byte Mode)

In byte mode, the 77101 counts 53 bytes after each TxSOC, and after receiving a complete cell, the cell is transmitted.

1. Assert TxFull, via register 0x02, Bit 7. This stops the 77101 from receiving more data, and prevents the complete assembly of a cell for transmission.
2. Enter desired loopback mode.
3. De-assert TxFull using 0x02, Bit 7. The previously 'interrupted' cell will continue to be assembled in the transmit FIFO; on completion, it will be transmitted, as selected via the loopback mode. If this partial cell should be discarded, assertion of TxSOC will clear this 'short' cell from the internal FIFO, and normal operation will resume.

Exiting Loopback (Cell Mode)

Under UTOPIA specification, cell mode is operated via the TxCLAV control, which indicates that the transmission device can receive an entire 53 byte cell for transmission. Therefore, a complete cell will automatically be received and transmitted by the 77101, even after TxCLAV assertion is inhibited:

1. De-assert TxCLAV, using 0x02, Bit 7. As described above, under normal UTOPIA operation it is assumed that the remainder of the cell will continue to be shipped to the 77101.
2. After waiting for complete cell to be transmitted, enable desired loopback mode. If loopback is entered prior to complete cell receipt, the cell will be looped back.
3. Re-assert TxCLAV using 0x02, Bit 7.

Exiting Loopback (Byte and Cell Modes)

The same conditions and concerns exist for exiting loopback, as for entering these modes. Therefore, follow the above instructions, except replace step #2 with 'disable loopback mode'.

2. COUNTERS

Several condition counters are provided to assist external systems (e.g. software drivers) in evaluating communications conditions. It is anticipated that these counters will be polled from time-to-time (user selectable) to evaluate performance.

- Symbol Error Counter
  - 8 bit counter
  - counts all undefined 5 bit symbols in received data stream
- TxCell Counter
  - 16 bit
  - counts all transmitted cells
- RxCell Counter
  - 16 bit counter
  - counts all received cells
- Receive HEC Error Counter
  - 5 bit counter
  - counts all received HEC errors

8

The TxCell and RxCell counters are sized (16 bits) to provide a full cell count (without roll over) if the counter is read once/second. The Symbol Error counter and HEC Error counter were given sufficient size indicate exact counts for low error-rate conditions. If these counters overflow, a gross condition is occurring, where additional counter resolution does not provide additional diagnostic benefit.

Reading Counters

1. Decide which counter value is desired. Write to register 0x06 to the bit location corresponding to the desired counter. This loads the Counter Read register with the selected counter's value, and resets this counter to zero.

NOTE: Only one counter (Selected bit in 0x06) may be enabled at any time.

2. Read registers 0x04 (low byte) and 0x05 (high byte) to get the value.

Further reads may be accomplished in the same manner by writing to register 0x06.

MULTI-PHY OPERATION

Multiple physical interfaces may be connected to common busses to amortize the use of common "upstream" hardware. Device selection is controlled via the UTOPIA "enable" control signals: $\overline{\text{TxEnb}}$ and $\overline{\text{RxEnb}}$. In transmit, $\overline{\text{TxEnb}}$ tells the selected device that the data and control signals it sees are to be used for ATM cell transmission. In receive, when $\overline{\text{RxEnb}}$ is not asserted (active low), RxData[7:0], RxParity, and RxSOC are all tri-stated, allowing them to share a common bus. When $\overline{\text{RxEnb}}$ is asserted, the selected device drives these outputs, transferring the data to the upstream hardware.

Note that while multiple transmit devices may be selected (e.g. for multicast) by asserting more than one $\overline{\text{TxEnb}}$, multiple receive devices should not be enabled. Also, the output of $\overline{\text{RxRef}}$ is not affected by $\overline{\text{RxEnb}}$; the same is also true for $\overline{\text{TxRef}}$ and $\overline{\text{TxEnb}}$. These must routed and/or multiplexed separately.

Figure 13 is an example of connecting multiple PHYs in the transmit direction. A separate TxEnb signal is provided to each 77101 for device select.

Multi-Phy Receive is constructed in the same manner as transmit, in that each device is selected with a dedicated $\overline{\text{RxEnb}}$ signal. (See Figure 14).

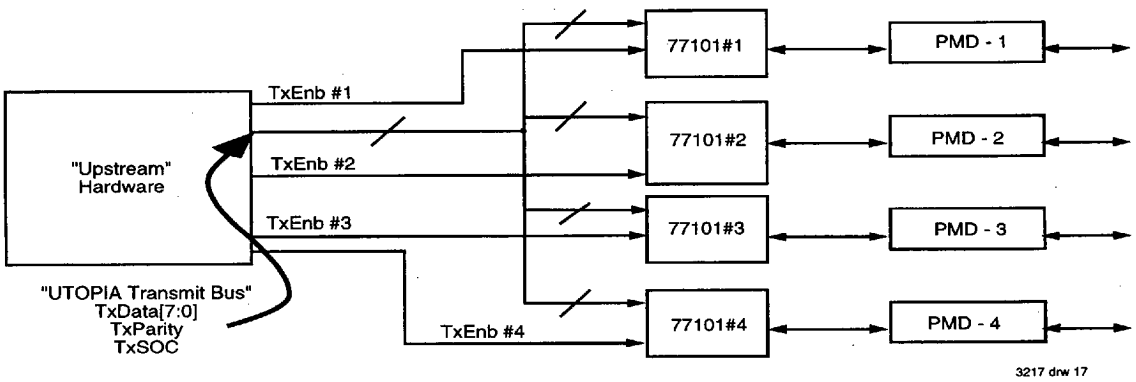

Figure 13 Multi-PHY: Transmit Example

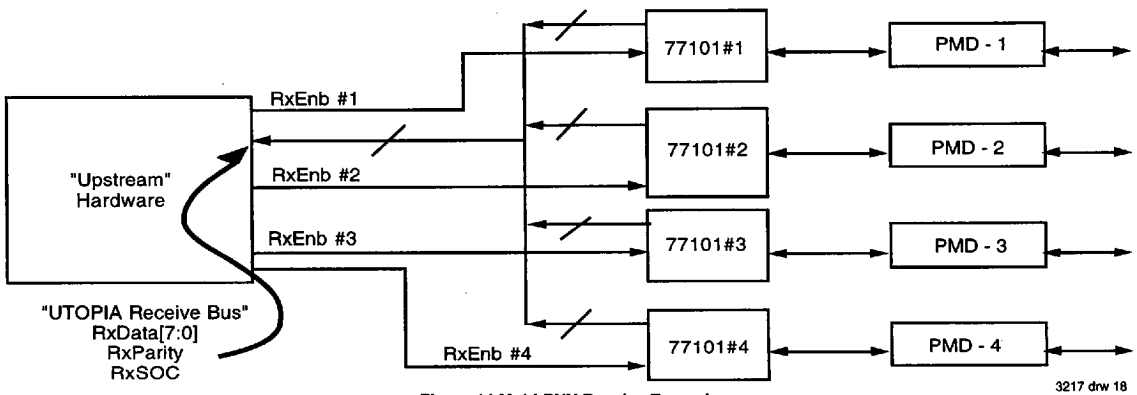

Figure 14 Multi-PHY Receive Example

STATUS AND CONTROL REGISTER LIST

Nomenclature
R/W = register may be read via the management interface and written from the management interface;
R-only or W-only = register may be read-only or write-only from management interface;
sticky = register bit is reset back to default state after read.
"0" = 'cleared' or 'not set'
"1" = 'set'

MASTER CONTROL REGISTER

Address: 0x00

Master	Type	Default	Function
Bit 7	R/W	0 = disabled	**Standby** Controls pin 11, "Standby" used to select standby mode of PMD component.
Bit 6	R/W	0 = disabled	**Discard Receive Error Cells** On receipt of any cells with an error (e.g. short cell, invalid command mnemonic, receive HEC error (if enabled), the receive FIFO queue will be cleared of this cell, and cell discarded without further intervention from outside the PHY.
Bit 5	R/W	0 = disabled	**Enable Cell Error Interrupts Only** If Bit 0 in this register is set (Interrupts Enabled), setting of this bit enables only "Received Cell Error" to trigger interrupt line.
Bit 4	R/W	0 = disabled	**Transmit Data Parity Check** Directs TC to check parity of TxData[0:7] against parity bit located in TxData[8].
Bit 3	R/W	1 = enabled	**Discard Received Idle Cells** Directs TC to discard received idle (VPI/VCI = 0) cells from PMD without signaling external systems.
Bit 2	R/W	0 = disabled	**Halt Tx** Halts transmission of data from TC to PMD.
Bit 1	R/W	0 = cell mode	**UTOPIA mode select:** 0 = cell mode, 1 = byte mode.
Bit 0	R/W	1 = enabled	**Interrupt Mask Bit (Enable Interrupt Pin)** Enables interrupt output pin. If cleared, pin is always high, and interrupt is masked. If set, an interrupt will be signaled on the interrupt pin (pin 53), by setting its output to "0".

INTERRUPT STATUS

address: 0x01

Bit	Type	Default	Function
Bit 7		Reserved	
Bit 6	R	0 = not good signal	**Good Symbol Bit** 1 = No symbol errors in past 7196 Received symbols 0 = ≥ 1 symbol in past 2048 symbols
Bit 5	sticky	0	**HEC error cell received**
Bit 4	sticky	0	**"Short Cell" Received** Interrupt signal which flags received cells with fewer than 53 bytes. This condition is detected by the TC receiving Start-of-Cell command bytes with fewer than 53 bytes between them.
Bit 3	sticky	0	**Transmit Parity Error** If Bit 4 of Register 0x00 is set (Transmit Data Parity Check), this interrupt flags a transmit data parity error condition.
Bit 2	sticky	0	**Receive Signal Condition change** This interrupt is set when the received 'signal' changes either from 'bad to good' or from 'good to bad'.
Bit 1	sticky	0	**Received Cell Symbol Error** Set on receiving a cell with an undefined symbol.
Bit 0	sticky	0	**Receive FIFO Overrun** Interrupt which flags condition where receive FIFO has reached full condition and cannot accept additional data.

8

DIAGNOSTIC CONTROL

Address: 0x02

Bit	Type	Default	Function
Bit 7	R/W	0	**Disable TxClav assertion.** Used during line loopback mode to prevent upstream system from continuing to send data to 77101.
Bit 6	R/W	0	**RxClav operation select.** The UTOPIA standard dictates that during cell mode operation, if the receive FIFO no longer has a complete cell available for transfer from PHY, RxClav is deasserted following transfer of the last byte out of the PHY to the upsteam system. Others have suggested that deassertion of this signal should occur when they are at the end of Payload byte 44 (as in octet mode for TxFull), which would provide early indication to the upstream system of this impending condition. "Standard RxClav" = 0 "Cell mode = Byte mode" = 1
Bit 5	R/W	1 = "multi"	**Single/Multi-PHY configuration select** 0 = single; 1 = "multi". "Multi" means that the following pins are tri-stated when 77101 TC is not selected via RxEnab: RxData[7:0], RxPrty RxSOC
Bit 4	R/W	0	**+RFLUSH = clear receive FIFO** This signal is used to tell the TC to flush (clear) all data in the receive FIFO. The TC signals this completion by clearing this bit.
Bit 3	R/W	0	**Insert xmit payload error** Tells TC to insert cell payload errors in transmitted cells. This can be used to test error detection and recovery systems at destination station, or , under loopback control, the local receiving station. This payoad error is accomplished by flipping bit 0 of the last cell payload byte.
Bit 2	R/W	0	**Insert Xmit HEC Error** Tells TC to insert HEC error in Byte 5 of vcell (only, ie, without modifying any bits in Bytes 1, 2, 3, or 4). This can be used to test error detection and recovery systems in down-stream switches, or, under loopback control, the local receiving station. This HEC error is accomplilshed by flipping bit 0 of the HEC byte.
Bit 1,0	R/W	00	**Loopback control** **bit# 1 0** 0 0 Normal mode (receive from network) 0 1 PMD Loopback 1 0 TC Loopback 1 1 Line Loopback

LED DRIVER AND HEC STATUS/CONTROL

Address: 0x03

Bit	Type	Default	Function
7		Reserved	
6	R/W	0 = recv HEC check enabled	**Disable Receive HEC Checking (+HEC Enable)** When not set, TC calculates HEC byte on first a4 bytes of received cell, and compares value against 5th byte. When set (= 1), TC does not check HEC byte.
5	R/W	0 = xmit HEC enabled	**Disable Xmit HEC Calculate & Replace** Directs TC not to calculate HEC on first 4 bytes of cell queued for transmit and replace 5th byte with this HEC calculation result.
4,3	R/W	00 = 1 RxClk cycle	**$\overline{\text{RxRef}}$ pulse width select** bit # 4 3 0 0 RxRef active for 1 RxClk cycle 0 1 RxRef active for 2 RxClk cycles 1 0 RxRef active for 4 RxClk cycles 1 1 RxRef active for 8 RxClk cycles
2	R	1 = xmit FIFO empty	TxLED FIFO Status
1	R	1 = TxLED is "on" (active low)	TxLED Status
0	R	1 = TxLED is "on" (active low)	RxLED Status

LOW BYTE COUNTER REGESTER [7:0]

Address: 0x04

Bit	Type	Default	Function
[7:0]	R	0x00	Provides low-byte of counter value selected via register 0x06.

HIGH BYTE COUNTER REGISTER [15:8]

Address: 0x05

Bit	Type	Default	Function
[7:0]	R	0x00	Provides high-byte of counter value selected via register 0x06.

COUNTER REGISTER READ SELECT

NOTE: Only one bit may set at any time for proper operation

Address: 0x06

Bit	Type	Default	Function
Bit 7	—	—	Reserved
Bit 6	—	—	Reserved
Bit 5	—	—	Reserved
Bit 4	—	—	Reserved
Bit 3	R/W	0	Symbol Error Counter
Bit 2	R/W	0	TxCell Counter
Bit 1	R/W	0	RxCell Counter
Bit 0	R/W	0	Receive HEC Error Counter

LED OUTPUT

LED outputs are able to source and sink current, to enable driving two-color LEDs. The Tx and Rx LEDs are driven according to the following table:

	State	Pin Voltage
RxLED	Cells being received Cells not being received	Low High
TxLED	Cells being transmitted Cells not being transmitted	Low High

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

3139 tbl 07

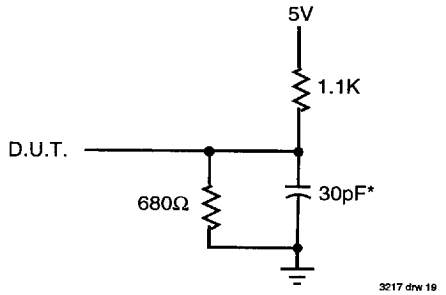

Figure 15. Output Load

* Includes jig and scope capacitances.

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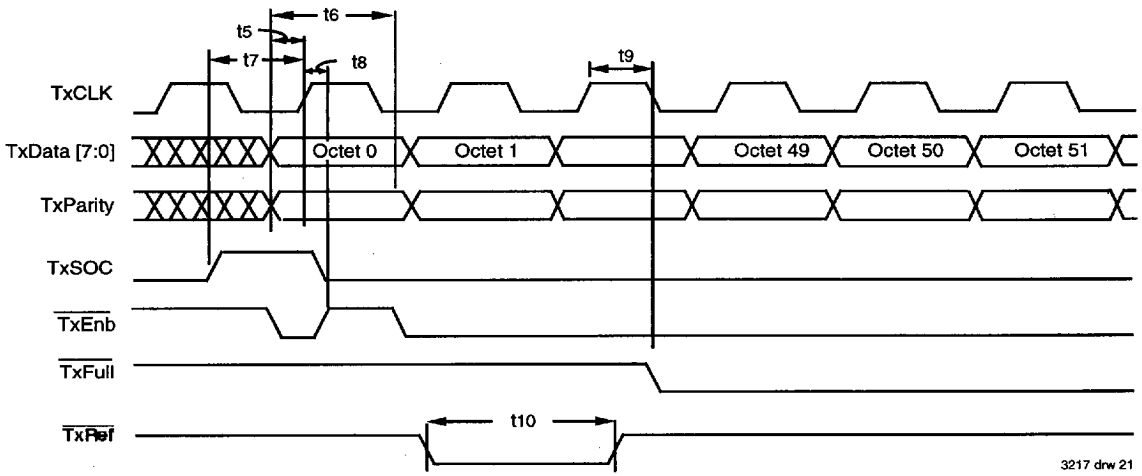


Figure 16. UTOPIA Transmit

UTOPIA Bus

Symbol	Parameter	Min.	Max.	units
t1	RxEnb setup time to RxCLK	10	—	ns
t2	RxEnb hold time from RxCLK	2	—	ns
t3	tPD from RxClk to RxSOC, RxData, and RxRef	—	20	ns
t4	RxEmpty delay from RxCLK	—	20	ns
t5	TxData[7:0], TxParity setup time to TxCLK	10	—	ns
t6	TxData[7:0], TxParity hold time from TxCLK	2	—	ns
t7	TxSOC, TxEnb setup time to TxCLK	10	—	ns
t8	TxSOC, TxEnb hold time from TxCLK	2	—	ns
t9	TxFull delay from TxCLK	—	20	ns
t10	TxRef pulse width	TxClk Period + 5 ns	—	ns

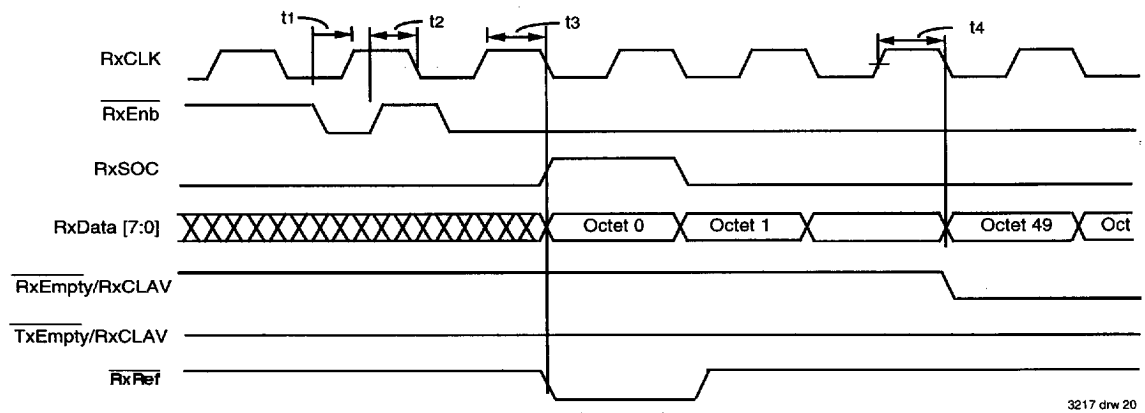


Figure 17. UTOPIA Receive

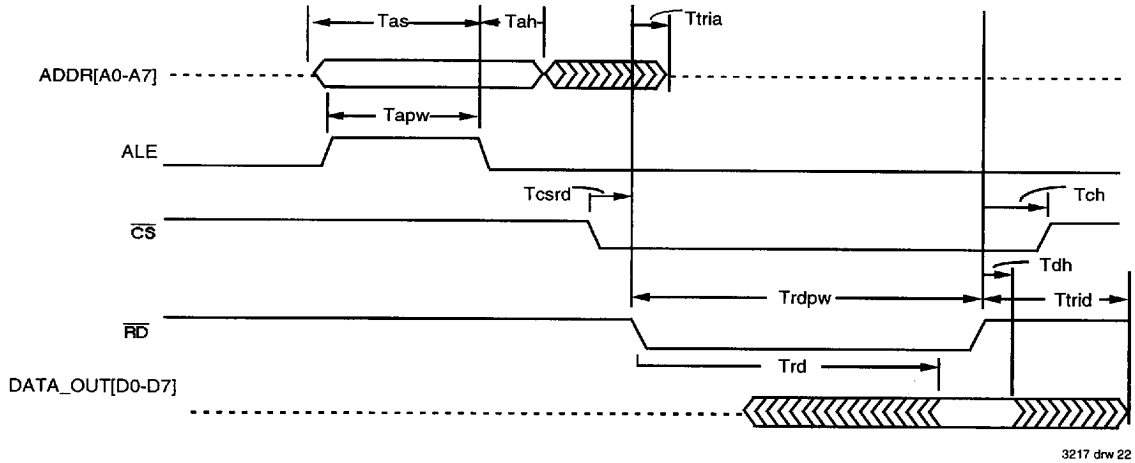


Figure 18. Utility Bus Read Cycle

Utility Bus Read Cycle

Name	Min	Max	Unit	Comment
Tas	10	—	ns	Addr setup to ALE
Tcsrd	0	—	ns	Chip select to read enable
Tah	5	—	ns	Addr hold to ALE
Tapw	10	—	ns	ALE min pulse width
Ttria	—	0	ns	Addr. trstate to RD assert
Trdpw	20	—	ns	Min. RD pulse width
Tdh	0	—	ns	Data Valid hold time
Tch	0	—	ns	RD dassert to CS deassert
Ttrid	—	10	ns	RD deassert to data tristate
Trd	5	20	ns	Read DATA access

Utility Bus Write Cycle

Name	Min	Max	Unit	Comment
Tapw	10	—	ns	ALE min pulse width
Tas	10	—	ns	ADDR set up
Tah	5	—	ns	ADDR hold time
Tcs	0	—	ns	CS to WD set up
Twpw	20	—	ns	WD pulse width
Tdws	20	—	ns	Write Data set up
Tdwh	10	—	ns	Write Data hold time
Tch	0	—	ns	WD deassert to CS deassert

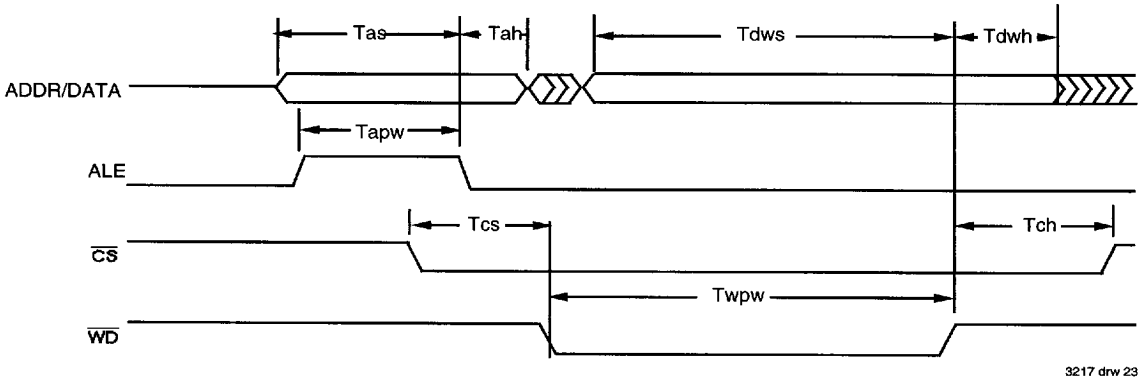


Figure 19. Utility Bus Write Cycle

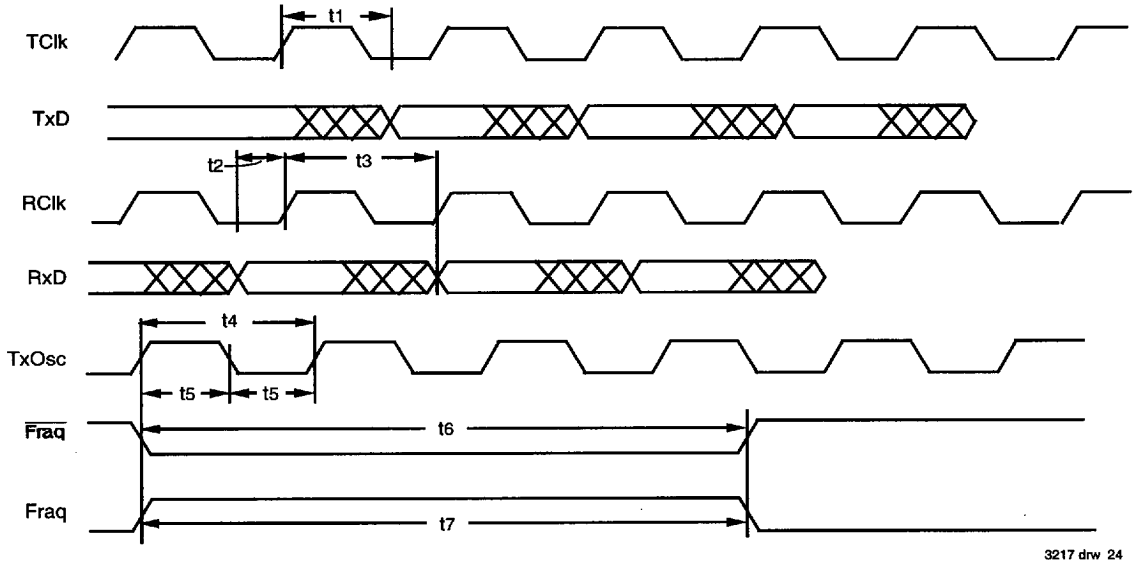
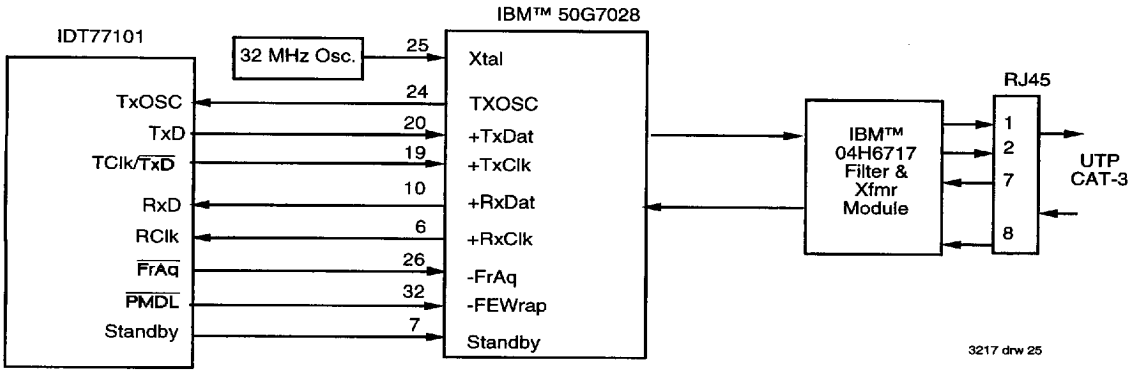


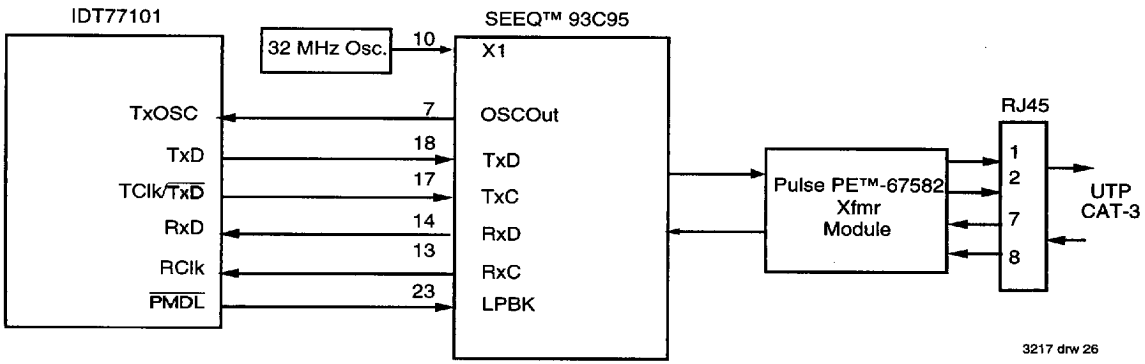
Figure 20. PMD Interface

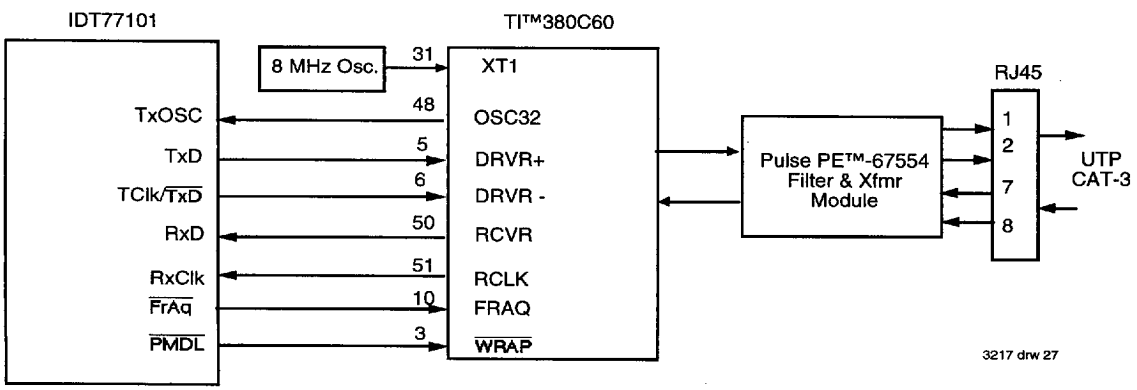
PMD INTERFACE

Symbol	Parameter	Min.	Max.	units
t1	TxD valid from TCLK	2	20	ns
t2	RxD setup time to RCLK	10	—	ns
t3	RxD hold time from RCLK	2	—	ns
t4	TxOsc frequency	32 - 100ppm	32 + 100ppm	MHz
t5	Pulse with distortion from 50/50 duty cycle	- 750	+ 750	ps
t6	$\overline{\text{Fraq}}$ (PMD SEL = IBM)	2048	2048	TxOsc Period
t7	Fraq (PMD SEL = TI)	4096	4096	

25.6 Mbps ATM PHY IMPLEMENTATION EXAMPLES







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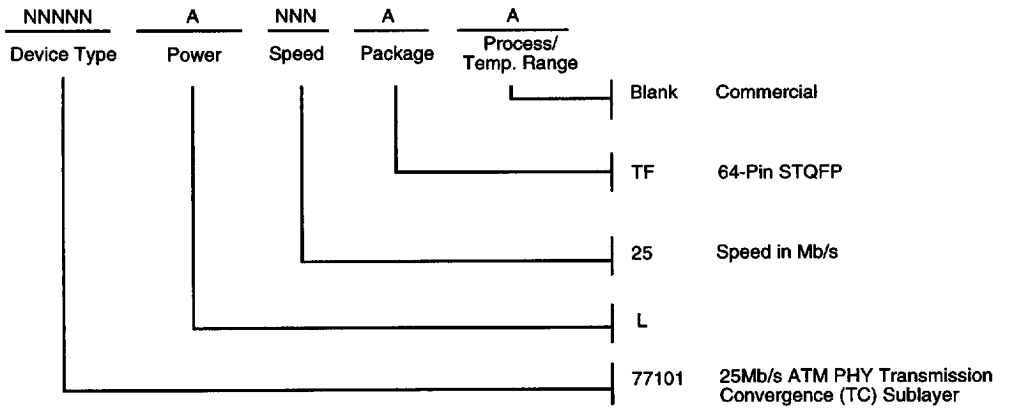
ORDERING INFORMATION

IDT



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PRILIMINARY DATASHEET: DEFINITION

"PRLIMINARY" datasheets contain descriptions for products which are in early release, including features and block diagrams.

Datasheet Document History

3/1/95: Initial Draft.
6/17/95: Revised.
8/9/95: Revised.
1/9/96: Change to "Preliminary" and added package mechanical diagram.

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