Integrated Device Technology, Inc.

SINGLE-CHIP SYSTEM CONTROLLER

IDT79R3715
ADVANCE INFORMATION

FEATURES

- System Controller for the pin-compatible IDT R30xx family of processors
- DRAM Controller
  - 1 - 40 MB directly, 1 - 3 banks directly
  - Device depth supported: 256K - 4M
  - Non-interleave
- ROM Controller
  - 1 - 20MB, Address-space support bank size: 1- 8MB
  - Support for standard and burst ROMs
  - Support for interleave or non-interleave
- Direct Interface to external DMA master
- I/O Bus follows 8/16-bit Intel 80186 style
- I/O Controller
  - Two 8-bit and two 16-bit external channels
  - DMA and non-DMA access for the 8-bit channels
  - 8-32 packing, 32-8 unpacking logic for DMA access
  - 16-32 packing, 32-16 unpacking for CPU/ external DMA master coprocessor accesses
  - Round robin arbitration
  - Programmable timing for I/O and control signals
  - Big and Little Endian support
- PCMCIA Support
  - Through 16-bit I/O bus, using simple glue logic
  - 16-bit to 32-bit packing and 32-bit to 16-bit unpacking
  - Big and Little Endian support
  - 256MB address space dedicated to 2 PCMCIA slots
- 24-bit Timer/Counter, In-Circuit testing capability
- Centronics Interface
  - Bi-directional Centronics, compliant with IEEE1284
  - Supports DMA and CPU controlled transfers
  - Supports the following modes: Compatible; Nibble; Byte; ECP; EPP
- Interrupt Controller
  - 6 external level interrupts (through the PIO pins)
  - 14 internal interrupts
  - Individual interrupt mask capability, enabling polling or interrupt-driven systems
- General Purpose I/O
  - Six programmable Input (interrupts) or Output pins

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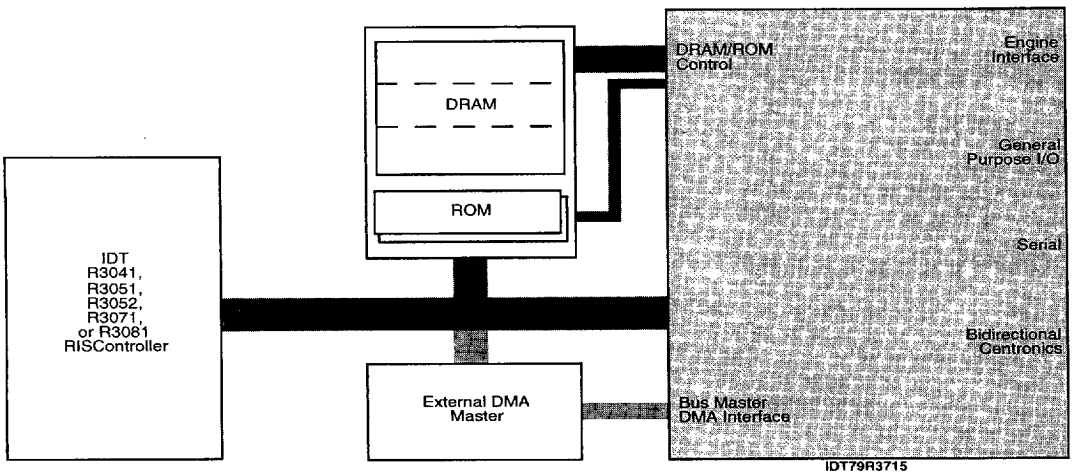


IDT79R3715 System Organization

3715-20

OVERVIEW

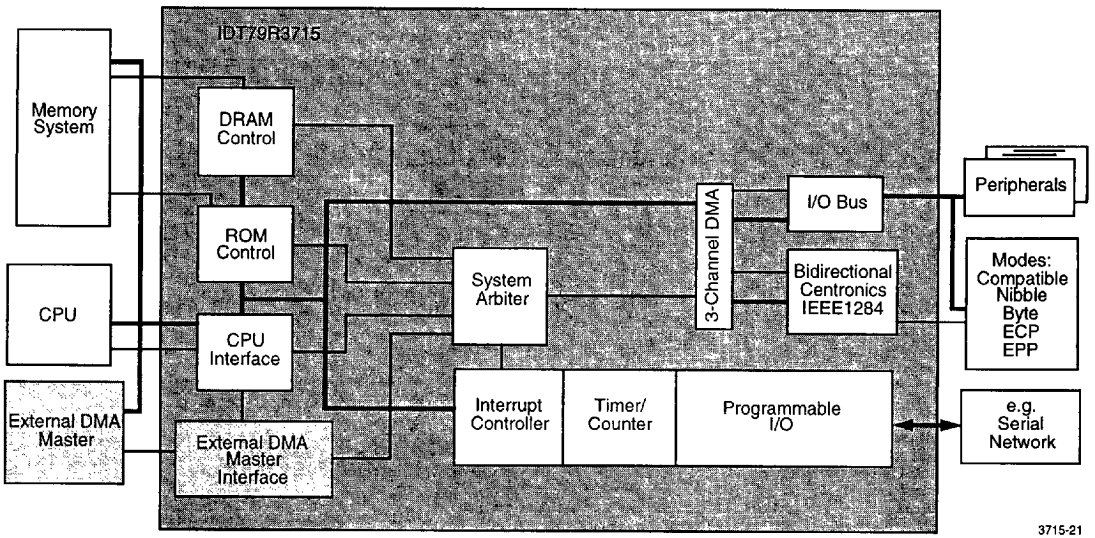
The IDT79R3715 is a single-chip System Controller designed to complement IDT's R30xx family of 32-bit embedded processors. It has all of the features necessary to maximize the performance of a RISC-based system and reduce the overall system chip count.

The R3715 can move large amounts of data quickly without the need for processor intervention. It also achieves a significant reduction in system cost by its high level of integration. Additional savings come from the architecture of the I/O controller, which allows for the utilization of low cost peripheral components (disk controller, network controller, etc.), while attaining the higher level of performance only associated with costlier components.

Some of the architectural characteristics that result in very high performance include:

- incorporating a tightly coupled interface to any of the R30xx RISC CPUs
- minimizing latency to critical resources
- partitioning the system in a balanced way to attain efficient use of shared resources
- enabling several simultaneous operations in the system

The R3715 is ideal for modular design of laser printers because it allows a high level of programmability and incorporates the control logic for an industry standard interface to peripherals. This gives OEMs the ability to offer several products from the same basic design, as well as the ability to upgrade systems in the field. The block diagram that follows shows the R3715 configuration.



IDT79R3715 Block Diagram

FUNCTIONAL DESCRIPTION

Processor Interface

The R3715 has a glueless interface to the IDT R3041/51/52/71/81 family of RISC processors. It supports these devices in both slave and master modes of operation. As slave, they support CPU access to memory and I/O devices, and as master, handle accesses on the A/D bus.

As slave the R3715 supports processor single transfer read or write, as well as burst read access. Each supports processor access to the ROM, DRAM, devices on the I/O bus, and the R3715 internal registers. Burst read is supported only for DRAM or ROM read access. ACK* and RDCEN* timing is fixed for the R3715 registers. DRAM access can be extended by one clock, and access timing for ROM and I/O are programmable.

As master the R3715 will request the bus by asserting BUSREQ* when a DMA source (internal or external) needs to transfer data to or from the DRAM / ROM / I/O Channel.

The priority between the DMA sources is in the following descending order:

- Access in process
- I/O DMA
- External DMA master

The CPU will get ownership of the A/D bus for at least one cycle after four DMA accesses. This assumes that each external DMA master (external agent) bus possession is counted as one, regardless of the number of transfers it executes on the bus. In the default state, when there is no DMA request, the bus is owned by the CPU.

Figure 2.1 shows the CPU-to-R3715 interface.

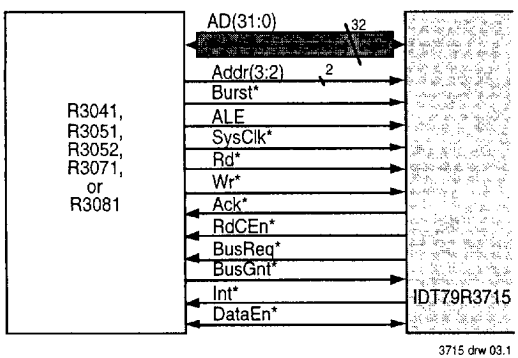


Figure 2.1 RISController to R3715 Interface

External DMA Master Interface

The R3715 has a simple interface to the external DMA master coprocessor. It supports the external DMA master operation in its slave and master modes. As slave it supports the processor read and write accesses to the external DMA master, and as master it enables access to the DRAM, ROM, and 16 bit I/O bus (for font cartridges). The R3715 directly controls the data buffers and the address buffer needed to isolate the external DMA master from the A/D bus.

The R3715 decodes CPU access to the external DMA master and asserts ECS*, EAS*, and EDS*. The address is latched into an external transparent latch (373-type) when the processor asserts ALE and is driven into the multiplexed bus (DAL[31:0]) by EATOE*. Data is driven to or from the external DMA master by transceivers controlled by EADDIR* and EADOE*. To end an external DMA master cycle the R3715 asserts RDCEN* and ACK* to the CPU when the external DMA master asserts EDTACK*.

In external DMA master mode, the external DMA master requests the bus by asserting EBREQ*. The R3715 will grant the bus by asserting EBGNT* (provided no other DMA device has requested the bus and provided also that it was granted by the CPU to the R3715). The external DMA master will assert EAS* first, and then EDS*, to initiate an access to a system resource (e.g. DRAM). The R3715 will assert EADOE* and EADDIR* to drive the external DMA master address, and ALE to latch it. In the data phase it will assert EADDIR* and EADOE* according to the access direction (Read or Write).

To end the cycle the R3715 will assert EDTACK* to the external DMA master. When it does not require the bus any longer the external DMA master will release it by deasserting EBREQ*

External access to the DRAM takes 5 clocks from EAS* to EDTACK*. Frequencies above 25 MHz may need an additional clock cycle. One clock can be added to this interval by using the ExtCas bit in the DRAM control register.

Figure 2.2 on the following page shows a typical implementation of an external DMA master interface.

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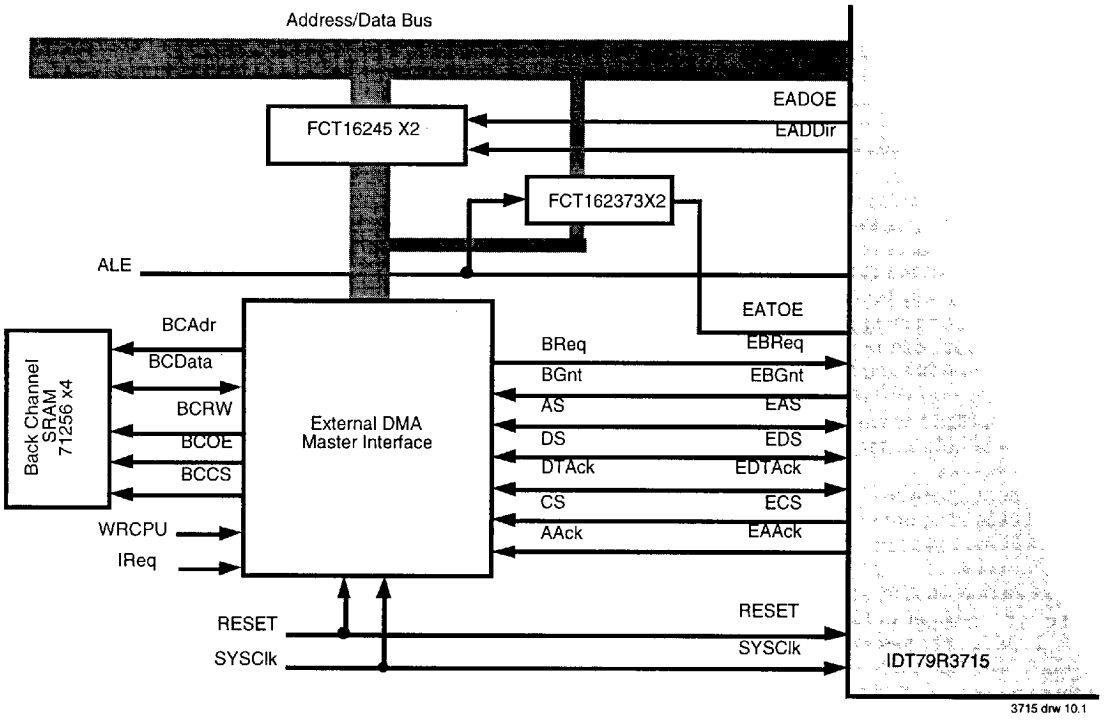


Figure 2.2 External DMA Master Coprocessor Implementation

ROM

The ROM controller supports up to 20 Mbyte of memory with several device types and system configurations. To support these system and device options, the assertion time of RDCEN* and ACK* by the R3715 can be programmed, thus accommodating different types of memory architectures, including standard ROMs, interleaved ROMs, and burst ROMs.

There are three CS signals to support up to three banks of ROM. Each ROM bank can be either non-interleaved or interleaved (composed of 2 leaves of ROM differentiated by ADDR[2]). ROMCS[2]* controls the boot bank and has a fixed address space of 4 Mbyte. Address space for ROMCS[1]* and ROMCS[0]* is programmable to 1, 2, 4, or 8 Mbyte.

The R3715 puts the 3 ROM bank address ranges in a contiguous address space. In other words, the start address of the next ROMCS[x]* will follow the last address of the previous ROMCS[x-1]*. For interleaved support, ROMOE* is provided to control the OE of the interleave multiplexer. The R3715 also supports burst ROM, and can be made to write to the ROM space (for flash or debug) with additional glue logic.

After reset, the R3715 is configured with the maximum number of wait states between each data transfer (16 clocks between each RDCEN*) and 64 clocks between ROMCS[x]* to ACK*. The initial (reset) space size for ROMCS[1]* and ROMCS[0]* is 1 Mbyte, and 4Mbytes for ROMCS[2]*.

Figure 2.3 on the following page shows the configuration of the ROM/DRAM memory system.

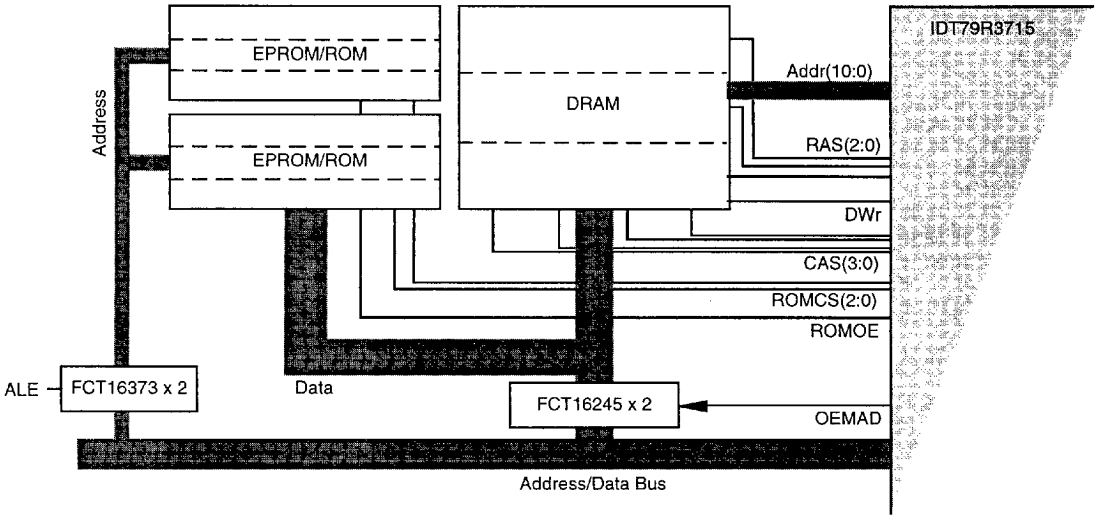


Figure 2.3 R3715 ROM/DRAM Memory System 3715 drw 04.1

DRAM

The DRAM controller supports directly 1 to 40 Mbytes of DRAM, with up to three non-interleaved banks. The address space starts at physical address 0. The DRAM device types supported have the following attributes: page mode, early write, and "CAS before RAS" refresh.

The DRAM controller supports single transfer reads and writes and burst reads. Various DRAM device depths are supported and the address space is continuous for the selected configuration. The DRAM controller can be configured to support different device depth for the base bank (RAS[0]*) and the extension banks (RAS[1]* and RAS[2]*).

For systems running at high frequency there is an option to extend the CAS* signals by an additional cycle. An external DMA master may sample data on the rising edge of SYSCLK*, and the CPU on the falling edge. It is possible to extend the CAS* by one cycle for external DMA master accesses. To minimize the refresh penalty IDT recommends that you program the refresh frequency according to the value of SYSCLK*.

The initial values of the R3715 control registers at reset are shown in the tables in Section 3.

PIO Port

Each of the PIO[5:0] pins can be individually programmed to be an output or input pin by writing to the PIO Control register. When programmed as an input pin it can be used as a level (active LOW) interrupt. The PIO pins are synchronized and pulled up internally. At reset, all PIOs are initialized as inputs.

Interrupt Controller

Each interrupt source on the R3715 is maskable. The Cause register bit will reflect the cause of the interrupt, and writing a '0' into it will acknowledge the internal interrupt. For example - if the "BandInt" bit was active, the CPU should write 'fffB' into the Cause register, in order to reset the interrupt flag.

The external interrupts, PIO[5:0], are acknowledged at the source of the interrupt (the interrupt flag is deasserted when PIO is inactive), the corresponding bits in the Interrupt Cause register are read only.

At reset, all interrupts are masked in the mask register.

DMA-Based Serial Interface

One of the DMA-supported I/O channels can be used to support protocols such as AppleTalk directly, with only the addition of an external communication controller, such as the 85C30 or 85C230, and the I/O interface devices it requires. The R3715 I/O FIFO and Burst DMA capabilities aid in separating the real-time demands of protocols such as AppleTalk from the real-time demands of the engine interface, but without the cost implications of external buffering.

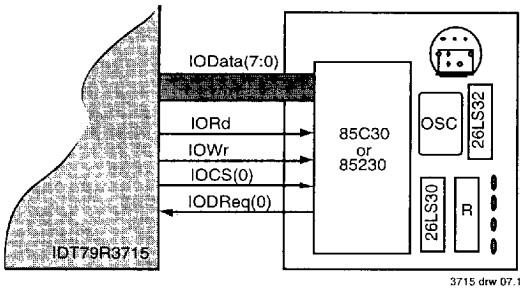


Figure 2.4 DMA-Supported AppleTalk I/O Port

Programmable Timer/Counter

The general purpose timer/counter can be programmed to function as a timer or as a counter. As a counter, it will cause an interrupt and stop counting when it reaches terminal count. Writing a new value to the counter will start the counter if the Enable bit is active. As a timer on terminal count, it will cause an interrupt, reload with the value stored in the Timer/Counter Value register and continue to count.

The Timer/Counter counting is enabled or disabled by the enable bit. The value *n* should be written to the Counter in order to count to *n* clocks. At reset, the counter is disabled.

I/O Bus

The R3715 supports two 8-bit (IOCS[1:0]*) and two 16-bit (IOGPμCS[1:0]*) external I/O channels that share the IODATA[15:0] pins. The two 8-bit I/O channels and the first 16-bit I/O channel (IOGPCS[0]*) each has a 16 Mbyte address space. The second 16 bit I/O channel (IOGPCS[1]*) has a 256 Mbyte address space.

Timing of the control signals to an I/O channel is programmable. The user can specify the length of IORD* and IOWR* signals. The IOCS[1:0]*, IOGPCS[1:0]* or DMAACK[1:0]* are asserted one cycle before the IORD* or IOWR* signals become active, and remain active for one cycle after IORD* or IOWR* are dasserted. RDCEN* and ACK* will be asserted by the R3715 to end a processor (or EDTACK* to end an external DMA master) I/O cycle.

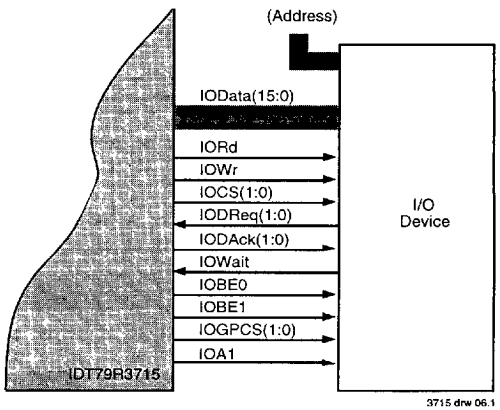


Figure 2.5 General Purpose I/O Device Interface

8-bit I/O Channels

The R3715 supports processor byte accesses (reads and writes) to devices located on the two 8 bit I/O channels. These accesses can be made using any of the four bytes on the 32 bit data bus. The R3715 will transfer the correct byte (according to the 4 Byte Enables) to the 8 bit I/O bus (IODATA[7:0]).

The I/O channel unit on the R3715 operates as a DMA controller with the two 8 bit I/O channels. DMA operations between I/O devices and the DRAM are supported. Eight bit data is packed or unpacked during DMA access into a 32 bit register for I/O DMA read or write respectively.

DMA Operations

Processor requests have priority over DMA requests. The priority for DMA operations is round robin for the Centronics and the two external 8-bit DMA engines. DMAREQ[1:0]* can be masked by writing '0' to the enable bit of the channel. A channel will not participate in the arbitration if the channel is disabled or if the I/O BIU (Bus Interface Unit) is owned by another channel.

The I/O BIU is emptied into memory in a DMA read access under the following conditions: 1) if the I/O BIU is full, or 2) if there is no DMA request (DMAREQ[1:0]) from the channel which owns the I/O BIU for a time out period, or 3) the byte count reaches zero.

In the write direction if the DMAREQ* from the channel that owns the I/O BIU is not active for a time out period, and the I/O BIU is not empty, arbitration will resume on the I/O bus. The time out period is set to 32 clocks. The clock period value cannot be changed, only enabled or disabled.

16-bit I/O Channels

The R3715 supports processor and external DMA master accesses (reads and writes) to devices located on the two 16-bit I/O channels.

For 16-bit devices, the CPU can read or write to any byte or half word. Processor or external DMA master access to the 16-bit I/O channels with any combination of byte enables active, will be performed in two consecutive I/O cycles in case of 3 or 4 byte accesses. In the two cycles, data will be packed or unpacked from a 32-bit register for an I/O read or write respectively. Conversion between big and little endian is supported for 16-bit devices.

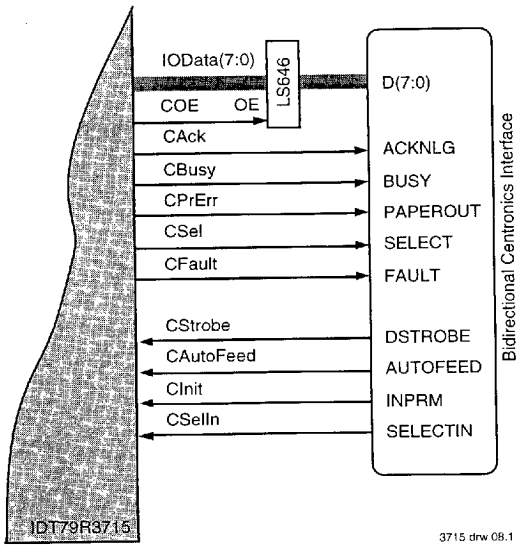


Figure 2.6 IEEE P1284 Bidirectional Centronics I/O Port

Centronics IEEE 1284 Communication

IDT's Centronics implementation meets the IEEE 1284 definition of a compliant device. It supports the following modes: Compatible, Nibble, Byte, ECP and EPP, as well as the negotiation necessary for transition between different modes. Support for the Compatible mode includes the following three variations: Standard, IBM Epson, and Classic.

Note: IDT urges designers to review the IEEE1284 Rev. 2 specification for a complete discussion of this Centronics standard.

There are two ways to handle the Centronics protocol. In the first option, data is transferred in DMA fashion and is only applicable in the Compatible, ECP, and EPP modes. The second option is interrupt driven, and applies to all modes. That is, Byte and Nibble modes are only interrupt driven.

There is support for special character detection in the Centronics incoming data. Control data characters like ^C or ^T can be detected and the CPU will be interrupted.

Figure 2.6 shows the configuration of the IEEE P1284 bidirectional centronics I/O port.

Negotiation

The R3715 defaults after reset to Compatible mode. The negotiation phase starts when the host sets CSELECTIN* HIGH and CAUTOFD* LOW. The R3715 interrupts the CPU by asserting the CentWrInt interrupt. The CPU interrupt routine includes reading the extensibility request value from the Centronics External register, and writing to the Centronics Control register to specify the supported mode. Note that the interpretation of the CenRdInt and CentWrInt interrupts, and the interrupt handler response, will be different in each mode.

Table 2.1 summarizes the values of host requests and the CPU interrupt routine response.

Request mode	Request value	Interrupt response: Mode-supported value	Interrupt response: Mode-not-supported value
Extensibility link first byte	1000 0000 xxxx xxxx	1110 1xxx	0111 0110
EPP	0100 0000	1100	0111
ECP with RLE	0011 0000	1011	0111
ECP	0001 0000	1011	0111
Device ID: -Nibble -Byte -ECP with RLE -ECP without RLE	 0000 0100 0000 0101 0001 0100 0011 0100	 1001 1010 1011 1011	 0111 0111 0111 0111
Byte	0000 0001	1010	0111
Nibble	0000 0000	0001	1111

Table 2.1 Interrupt Responses During Negotiation Phase

Compatible Mode

The CPU needs to configure the Compatible mode to one of the three supported modes: IBM, Classic or Standard, and to a data transfer option (DMA or interrupt per byte). Setting the modes and options is done by writing to the mode register (values are specified in the Centronics Mode register table).

In the interrupt per byte mode, the CPU will read data

responds to the CentRdInt interrupt. In DMA mode the CPU will initialize the DMA registers (addresses 1d0000a0, 1d000080 & 1d00098) before starting the DMA operation. The R3715 will assert interrupt CentDMAInt when the DMA counter will reach terminal count.

A host request to return to Compatible mode from any of the other modes is indicated to the CPU by the assertion of the CentRstInt interrupt.

Nibble Mode

The R3715 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to the Nibble data register. The R3715 sends the byte to the host over the control lines in two consecutive nibble transactions.

Byte Mode

The R3715 will interrupt the CPU by asserting CentWrInt when the host requests a byte transfer. The CPU will respond by writing data to Centronics External register.

Extensibility Link

Assertion of CentWrInt interrupt while in Compatible. mode indicates to the CPU an extensibility request. The CPU will read from the Centronics External register the extensibility request value, and write to the control register the next mode and proper response.

ECP Mode

DMA and interrupt per byte options are supported for the ECP mode.

In the interrupt per byte option, the R3715 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt.

In reverse transfer, in response to CentWrInt*, the CPU must first write to the Centronics status register (to the Busy bit). This indicates whether the CPU sends a command or data byte, and then write the data to the Centronics External register.

In forward transfer, in response to CentRdInt the CPU needs to read from the Centronics host register (Autofeed bit) to know whether the host is sending data or command, and then read the data from the Centronics register.

Note: RLE compression is supported only in interrupt per byte mode.

In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA. CentWrInt* will be asserted when the host requests data and the DmaDir bit in the Mode register indicates a read direction (From the IEEE1284 port to memory). CentRdInt will be asserted when the host sends data and the DmaDir bit indicates a write direction or when the host sends a command byte.

EPP Mode

DMA and interrupt per byte options are supported for the EPP mode, as follows:

In the interrupt per byte option, the R3715 will assert CentRdInt for host read requests, and will assert CentWrInt for host write requests. The CPU will read or write from the Centronics External register in response to the interrupt. It will distinguish between data and address by the contents of the strobe Selectin and AutoFd bits in the host buffer.

In the DMA transfer option, data will be transferred by the DMA as long as the direction of the host requests matches the direction of the DMA.

CentWrInt will be asserted: 1) when the host requests data, and the DmaDir bit in the Mode register indicates a read direction (from the Centronics port to memory), or 2) when the host asks for an address byte.

CentRdInt will be asserted: 1) when the host sends data and the DmaDir bit indicates a write direction, or 2) when the host sends an address byte.

CPU Control

This mode enables the CPU to set the values of the Centronics status register, and communicate with the host in compatible mode.

Character Detection.

The value of the three CentDetect 8-bit registers is constantly compared to the Centronics incoming data. When a match occurs the CPU is interrupted. Characters as ^C or ^T can be detected during Centronics DMA operations and the CPU can respond without the need to wait to the end of the DMA operation.

Programmable Timing

To allow for higher than specified (by the IEEE1284 standard) data rates, the minimum delay can be programmed to values lower than the minimum required by this standard.

PIN INFORMATION

Logic Symbols

Signals marked with an asterisk are active when low. Dashed arrows in figure 1.2 indicate MUX'ed signals.

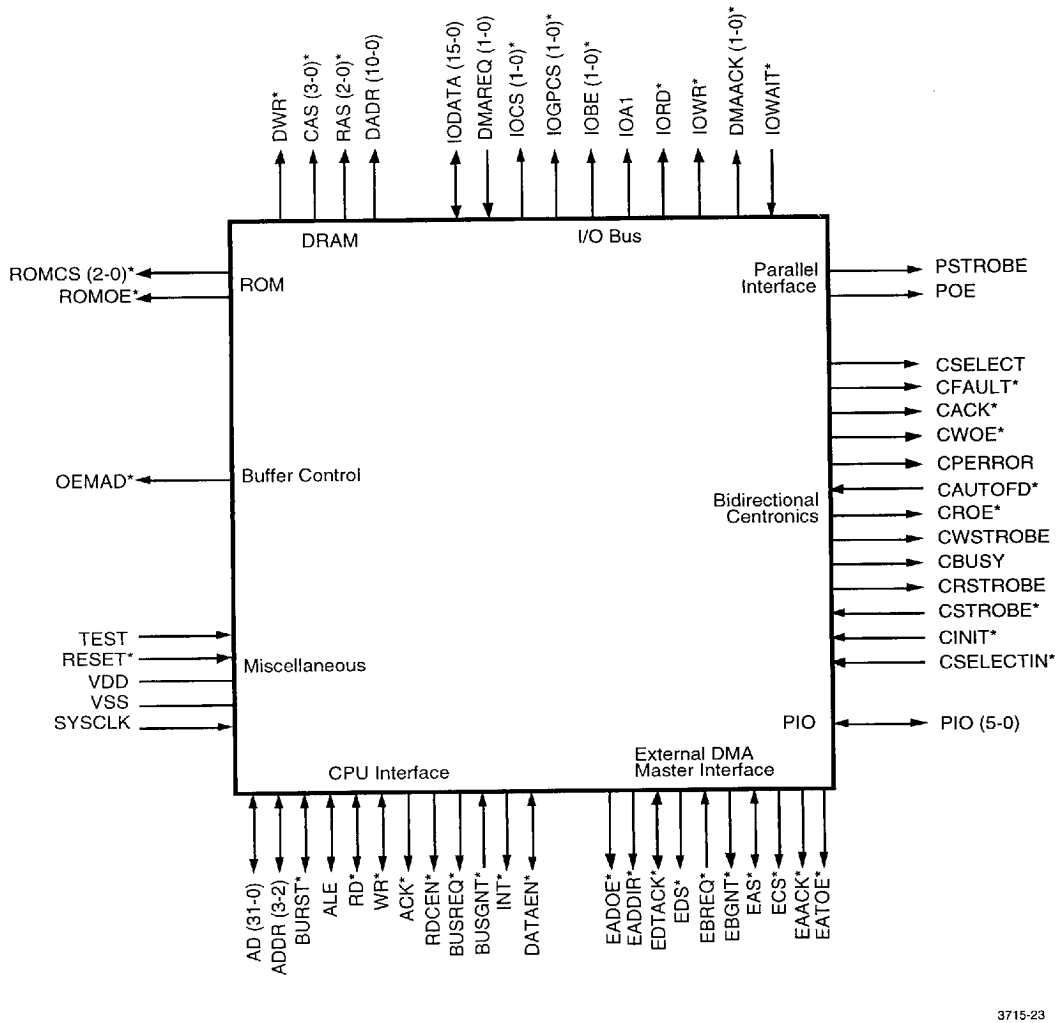


Figure 1.1 Logic Symbol for R3715

Pin Assignment Table

Pin names with a trailing asterisk (*) identify pins that are active when low.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CPU Interface				
A/D[31:0]	P.U.	I/O	8mA	**Address/Data:** Multiplexed address and data bus. In the Address phase: A/D[31:4] are address, A/D[3:0] are Byte Enable[3:0]. During external DMA Master cycles, A/D[3:2] contain address bits 3 and 2, and not Byte Enables. In the Data phase: Data[31:0]
ADDR[3:2]	P.U.	I/O	4mA	**Non Multiplexed Address:** Connected to the CPU ADDR[3:2]. In DMA cycles the R3715 drives these lines.
BURST*	P.U.	I/O	2mA	**Burst Transfer:** Used only during read cycles, the BURST* signal indicates that the current bus read is requesting a block of four contiguous words from memory. The pin connects to the CPU's BURSTWRNEAR* signal. In DMA cycles the R3715 drives this signal HIGH.
ALE	P.D.	I/O	4mA	**Address Latch Enable:** Used by the CPU to indicate that the A/D bus contains valid address information for the bus transaction. During external DMA master cycles, the R3715 asserts ALE to capture the address supplied by the external DMA master.
SYSCLK		I		**System Clock:** Connected directly to the CPU SYSCLK* output.
RD*	P.U.	I/O	2mA	**Read:** Indicates a read access by the CPU. In DMA cycles the R3715 drives the signal HIGH.
WR*	P.U.	I/O	2mA	**Write:** Indicates a write access by the CPU or the external DMA master. In a non-external DMA master cycle the R3715 drives this signal HIGH. Its negation indicates a read access by the external DMA master (during external DMA master).
ACK*		O	2mA	**Acknowledge:** Indicates to the CPU that the memory system has sufficiently processed the bus transaction i.e. that the CPU may either terminate a write cycle or process read data.
RDCEN*		O	2mA	**Read Buffer Clock Enable:** Indicates to the CPU that there is valid data on the A/D bus. Used during read cycles only.
BUSREQ*		O	2mA	**Bus Request:** The R3715 requests the CPU bus which is required for I/O and External DMA's.
BUSGNT*		I		**Bus Grant:** Indicates that the CPU has relinquished the bus.
INT*		O	2mA	**Interrupt:** "OR's" the internal and external interrupt sources.
DATAEN*		I/O	4mA	**Data Enable:** indicates the data phase in CPU read cycles. In DMA the R3715 asserts DATAEN* when the ROM/DRAM drives data onto A/D[31:0].
ROM				
ROMCS*[2:0]		O	4mA	**ROM Chip Select:** Select one of the 3 ROM banks. They can be connected to the ROM's Chip Select or Output Enable. ROMCS[2]* is connected to the boot ROM, with starting physical address 0x1fc00000.
ROMOE*		O	4mA	**ROM Output Enable:** Asserted when there is an access to any of the ROM banks. Used to output- enable the ROM data in systems where there is a buffer between ROM and DRAM data bus; eg. when using an interleaved ROM configuration.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
DRAM				
DADR[10:0]		O	8ma	**DRAM Address:** Multiplexed row and column address connected to the DRAM address.
RAS[2:0]*		O	4mA	**Row Adress Select:** Directly connected, on a bank basis, with the RAS* inputs of the DRAMs. Supports up to three banks of DRAMs.
CAS[3:0]*		O	4mA	**Column Address Select:** Directly connected, on a byte basis (can be across banks), to the CAS* inputs of the DRAMs. Connects a CAS* to each of the four bytes in every bank.
DWR*		O	12mA	**DRAM Write:** Connects to the write pin of each of the DRAMs.
External DMA Master Interface				
EBREQ*	P.U.	I		**External DMA Master Bus Request:** An external DMA master bus request to make a system resource access in master mode.
EBGNT*		O	2mA	**External DMA Master Bus Grant:** The R3715 asserts EBGNT* to grant the CPU bus to the external DMA master. Once the EBGNT* is asserted, it remains so until EBREQ* is deasserted.
EAS*	P.U.	I/O	2mA	**External DMA Master Address Strobe:** Master Mode (input) - the coprocessor indicates that it is driving valid data on the A/D bus. Slave mode (output) - the R3715 indicates that it is driving valid data on the A/D bus
EDS*		O	2mA	**External DMA Master Data Strobe:** Master mode (input) - during Write indicates that there is valid data on the A/D bus. During Read indicates data phase. Slave mode (output) - the R3715 drives EDS* to indicate that it is ready to accept data during reads or that valid data is available during write on the A/D bus.
EDTACK*	P.U.	I/O	2mA	**External DMA Master Data Acknowledge:** Master mode (output) - The R3715 asserts EDTACK* to indicate that the system is receiving or driving the requested data to/from the A/D bus. Slave mode (input) - The external DMA master asserts EDTACK* to signal that it has supplied or received data on its bus.
EAACK*		O	2mA	**External DMA Master Address Acknowledge:** The R3715 asserts EAACK* in the same clock that it asserts ALE for the external DMA master. This insures that the external DMA master continues driving the address until latched by the system.
ECS*		O	2mA	**External DMA Master Chip Select:** When the CPU accesses the external DMA master, the R3715 asserts ECS*. It is active one clock before R3715 asserts EAS*.
EADOE*		O	4mA	**External DMA Master A/D Output Enable:** The R3715 asserts EADOE* when the external DMA master drives the address to the A/D bus, and in the data phases of the external DMA master.
EADDIR*		O	4mA	**External DMA Master A/D Direction:** The R3715 asserts EADDIR* (LOW) when the external DMA master drives the A/D bus.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
EATOE*		O	4mA	**External DMA Master Address To Output Enable:** The R3715 asserts EATOE* in the address phase of cycles in which the CPU accesses the external DMA master.
Buffer Control				
OEMAD*		O	4mA	**Output Enable between Memory and A/D:** Output enable for the data path transceiver between the memory system (ROM and DRAM) and the A/D bus.
I/O Bus				
IODATA[15:0]	P.U.	I/O	8mA	**Input/Output Device Data:** Bidirectional 16-bit I/O Data bus.
IORD*		O	12mA	**Input/Output Device Read:** Active during Read from an I/O device.
IOWR*		O	12mA	**Input/Output Device Write:** Active during Write to an I/O device.
IOCS[1:0]*		O	2mA	**Input/Output Device Chip Select:** Chip selects for 8 bit I/O channels 0 and 1.
IOGPCS[1:0]*		O	2mA	**Input/ Output Device Chip Select:** Chip selects for 16 bit I/O channels 0 and 1.
DMAREQ[1:0]*	P.D.	I		**DMA Request:** Requesting DMA service on 8-bit channels 0 and 1.
DMAACK[1:0]*		O	2mA	**DMA Acknowledge:** Indicating that DMA access is granted on 8-bit channels 0 and 1.
IOA1		O	8mA	**Input/Output Device Address bit 1:** Provides a half word (16 bit) address on the I/O bus.
IOBE[1:0]*		O	2mA	**Input/Output Device Byte Enable:** Indicates which byte data bus is valid on the 16 bit I/O bus. IOBE[1]* corresponds to IODATA[15:8] and IOBE[0] corresponds to IODATA[7:0].
IOWAIT*	P.U.	I		**Input/Output Device Wait:** Indicates to the R3715 that a transfer cycle on the I/O bus needs to be extended.
PIO[5:0]	P.U.	I/O	8mA	**Programmable Input/Output:** Individually programmed pins for inputs, interrupt inputs or outputs.
Bidirectional Centronics				
CWOE*		O	2mA	**Centronics Write Output Enable:** Controls the Output Enable signal of the data register from the printer to the host.
CROE*		O	2mA	**Centronics Read Output Enable:** Controls the OE* of the Centronics external register in the direction from the host to the printer (the IODATA[7:0] bus).
CWSTROBE		O	2mA	**Centronics Write Strobe:** Clocks data from IODATA[7:0] into the Centronics register (from printer to host).
CRSTROBE		O	2mA	**Centronics Read Strobe:** Clocks data from the host into the Centronics register (from host to printer).

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CSTROBE*	P.U.	I		**Centronics Strobe:** Host driven. Compatibility mode: Set active low to transfer data into peripheral device's input latch. Data is valid while signal is low. Negotiation phase: Set active low to transfer extensibility request value into peripheral device's input latch. Data is valid on the leading (falling) edge of HostClk (CSTROBE*). Reverse data transfer phase: Set high during Nibble Mode transfers to avoid latching data into peripheral device. Pulsed low during Byte Mode transfers to acknowledge transfer of data from the peripheral. The peripheral device shall ensure that this pulse does not transfer a new data byte into the peripheral's input latch. ECP mode: Used in a closed-loop handshake with PeriphAck (CBUSY) to transfer data or address information from the host to the peripheral device. EPP mode: Set low to denote an address or data write operation to the peripheral device. Set high to denote an address or data read operation from the peripheral device. For a more detailed description refer to section 4.1 of the IEEE P1284 D2.00 specification.
CACK*		O	2mA	**Centronics acknowledge:** Peripheral device driven. Compatibility mode: Pulsed low by the peripheral device to acknowledge transfer of a data byte from the host. Negotiation phase: Set low to acknowledge 1284 support, then set high to indicate that the Xflag (CSELECT) and data available flags may be read. Reverse data transfer phase: Used in both Nibble and Byte Modes to qualify data being sent to the host. Reverse idle phase: Set low then high by peripheral device to cause an interrupt indicating to host that data is available. ECP mode: Used in a closed-loop handshake with HostAck (CAUTOFD*) to transfer data from the peripheral device to the host. EPP mode: Used by the peripheral device to interrupt the host. This signal is active high and positive edge triggered. For a more detailed description refer to section 4.3 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CBUSY		O	2mA	**Centronics Busy:** Peripheral device driven. Compatibility mode: Driven high to indicate the peripheral device is not ready to receive data. Negotiation phase: Reflects the present state of the peripheral device's forward channel. Reverse data transfer phase: Nibble mode: Data bits 3 then 7, then forward channel busy status. Byte mode: Forward channel busy status. Reverse idle phase: Forward channel busy status. ECP mode: Used by peripheral for flow control in the forward direction. PeriphAck (CBUSY) also provides a ninth data bit used to determine whether command or data information is present on the data signals in the reverse direction. EPP mode: Driven inactive as a positive acknowledgment from the peripheral device that transfer of data or address os completed. Signal is active when low, and should be driven active as an indication that the device is ready for the next address or data transfer. For a more detailed description refer to section 4.4 of the IEEE P1284 D2.00 specification.
CPERROR		O	2mA	**Centronics Printer Error:** Peripheral device driven. Compatibility mode: Driven high to indicate that the peripheral device has encountered an error in its paper path. Note that this signal's meaning varies among peripheral devices. Peripherals shall set nFault (CFAULT*) low whenever they set Perror (CPERROR) high. Negotiation phase: Set high to indicate 1284 support, then follows nDataAvail (CFAULT*). Reverse data transfer phase: Nibble mode: Data bits 2 then 6. Byte mode: Same as nDataAvail (CFAULT*). ECP mode: The peripheral drives this signal low to acknowledge nReverseRequest (CINIT*). The host relies upon nAckReverse (CPERROR) to determine when it is permitted to drive the data signals. EPP mode (User Defined 1): A manufacturer-specific signal. For a more detailed description refer to section 4.5 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn[1]	Type	Drive	Description
CSELECT		O	2mA	**Centronics Select:** Peripheral device driven. Compatibility mode: Set high to indicate that the peripheral device is online. Negotiation phase: Used by peripheral device to reply to the requested extensibility byte sent by the host during the negotiation phase. Affirmative response is indicated with the signal high for all request values except for Nibble Mode Reverse Channel Transfer, which is indicated affirmative with the signal low. Reverse data transfer phase: Nibble mode: Data bits 1 then 5. Byte mode: Same as negotiation phase. Reverse idle phase: Same as negotiation phase. ECP mode: Same as negotiation phase. EPP mode (User Defined 3): A manufacturer-specific signal. For a more detailed description of this signal refer to section 4.6 of the IEEE P1284 D2.00 specification. For more details about the negotiation phase refer to section 6.4 of the same specification.
CAUTOFD*	P.U.	I		**Centronics Autofeed:** Host driven. Compatibility mode: Interpretation varies among peripheral devices. Set low by host to put some printers into auto line feed mode. Also may be used as a 9th data, parity, or command/data control bit. Negotiation phase: Set low in conjunction with 1284 Active (CSELECTIN*) being set high to request a 1284 mode, then set high after peripheral device sets PtrClk (CACK*) low. Reverse data transfer phase: Nibble mode: Set low to indicate host can receive peripheral device to host data, then set high to acknowledge receipt of that nibble. Byte mode: Same as Nibble mode to request and acknowledge bytes. Following a reverse channel transfer, the interface transitions to idle phase when HostBusy (CAUTOFD*) is set low and peripheral device has no data available. Reverse idle phase: Set high in response to PtrClk (CACK*) low pulse to re-enter reverse data transfer phase. If set high with 1284 Active (CSELECTIN*) being set low, the 1284 idle phase is aborted and the interface returns to Compatibility mode. ECP mode: The host drives this signal for flow control in the reverse direction. It is used in an interlocked handshake with PeriphClk (CACK*). HostAck (CAUTOFD*) also provides a 9th data bit used to determine whether command or data information is present on the data signals in the forward direction. EPP mode: Used to denote a data cycle, and is active when low. For a more detailed description refer to section 4.7 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CINIT*	P.U.	I		**Centronics Initialize:** Host driven. Compatibility mode: Pulsed low in conjunction with 1284 Active (CSELECTIN*) low to reset the interface and force a return to Compatibility mode idle phase. Negotiation phase: Set high. Reverse data transfer phase: Set high. ECP mode: Driven low to place the channel in the reverse direction. While in this mode the peripheral is allowed to drive only the bidirectional data signals when nReverseRequest (CINIT*) is low and 1284 Active (CSELECTIN*) is high. EPP mode: When driven active (low), initiates a termination cycle that returns the interface to Compatibility mode. For a more detailed description refer to section 4.9 of the IEEE P1284 D2.00 specification.
CFAULT*		O	2mA	**Centronics Fault:** Peripheral device driven. Compatibility mode: Set low by peripheral device to indicate that an error has occurred. The meaning of this signal varies among peripheral devices. Negotiation phase: Set high to acknowledge 1284 compatibility. In Nibble or Byte mode it is then set low to indicate peripheral device to host data is available following host setting HostBusy (CAUTOFD*) high. Reverse data transfer phase: Nibble mode: Set low to indicate that peripheral device has data ready to send to host, then used to send data bits 0, then 4. Byte mode: Used to indicate that data is available. ECP mode: In this mode the peripheral may drive this pin low to request communication with the host. The request is only a suggestion to the host, who has ultimate control over the transfer direction. Typically used to generate an interrupt to the host, also provides a mechanism for peer-to-peer communication. Signal is valid in both forward and reverse directions. EPP mode (User Defined 2): Manufacturer-specific signal. For a more detailed description refer to section 4.10 of the IEEE P1284 D2.00 specification.

Pin Name	Pull Up/ Pull Dn [1]	Type	Drive	Description
CSELECTIN*	P.U.	I		**Centronics Select Input:** Host driven. Compatibility mode: Set low by host to select peripheral device. Negotiation phase: Set high in conjunction with HostBusy (CAUTOFD*) being set low to request a 1284 mode. Reverse data transfer phase: Set high to indicate that bus direction is peripheral device to host. Set low to terminate 1784 mode and set bus direction host to peripheral device. Reverse idle phase: Same as Reverse data transfer phase. ECP mode: Driven high by the host while in ECP mode. Set low by the host to terminate ECP mode and return the link to the Compatibility mode. EPP mode: Used to denote an address cycle, and is active low. For a more detailed description refer to section 4.11 of the IEEE P1284 D2.00 specification.
Parallel Port Control				
PSTROBE*		O		**Parallel Strobe:** Clocks 8-bit or 16-bit parallel data from IODATA[15:0].
POE*		O		**Parallel Output Enable:** When active (LOW) it controls the output enable of a data buffer for 8-bit or 16-bit wide parallel data into IODATA[15:0].
Misc.				
TEST	P.D.	I		**Master Output Enable:** When TEST is HIGH and RESET* is active, ALL the device outputs and I/Os are tri-stated (in a system, TEST should be pulled down to GND).
RESET*		I		**Reset:** Will reset the R3715 to the initial state.
VDD				**+5V** (+/-5%)
VSS				**Ground**

NOTE:
[1] Pull Up/Pull Dn identifies pins with internal Pull Up (P.U.) or Pull Down (P.D.) resistors. P.U./P.D. values are 35K-150Kohm depending on the process variation.

6

AC TIMING CHARACTERISTICS

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Signal(s)	Description	Min	Max	Unit
t1	SYSCLK	Pulse Width High	12		ns
t2	SYSCLK	Pulse Width Low	12		ns
t3	SYSCLK	Clock period	30		ns
t4	RESET*	Pulse Width from VDD Valid	200		us
t5	Reserved				
t6	BUSREQ*, ACK*, RDCEN*	Valid from SYSCLK rising	2	17	ns
t7	A/D[31:0], OEMAD*, EADOE*	Valid from SYSCLK falling	2	15	ns
t8	A/D[31:0], ADDR[3:2], WR*, PIO[5:0], EAS*, EDS*, EDTACK*	Driven from SYSCLK rising	0	20	ns
t9	A/D[31:0]	Tri-state from SYSCLK rising	0	15	ns
t10	A/D[31:0]	Set-up to SYSCLK falling	6		ns
t11	A/D[31:0]	Set-up to ALE falling	7		ns
t12	ALE	Set-up to SYSCLK falling	7		ns
t13	BURST*, RD*, DATAEN*, WR*, ADDR[3:2], BUSGNT*	Set-up to SYSCLK rising	10		ns
t14	ALE, BURST*, RD*, DATAEN*, INT*, PIO[5:0], IODATA[15:0], EAS*, EDS*, EDTACK*	Tri-state from SYSCLK rising	0	20	ns
t15	ALE, BURST*, RD*, DATAEN*, PIO[5:0]	Driven from SYSCLK rising	0	20	ns
t16	ALE, BURST*, RD*, DATAEN*, IOGPCS*, ROMCS*[2:0], IORD*, IOWR*, ROMOE*, IOA1, IOBE*[1:0], INT*, DMAACK*[1:0], PIO[5:0], ADDR[3:2], WR*, EAS*, EDS*, EDTACK*, ECS*, EBGNT*, EAACK*	Valid from SYSCLK rising	3	15	ns
t17	ADDR[3:2], WR*	Tri-state from SYSCLK rising	2	20	ns
t18	DADR[10:0]	Valid from AD address valid	6	25	ns
t19	DADR[10:0]	Valid from SYSCLK rising	3	27	ns
t20	RAS*[2:0], DWR*	Valid from SYSCLK rising	2	17	ns
t21	CAS*[3:0]	SYSCLK rising to CAS* LOW	2	13	ns
t22	CAS*[3:0]	SYSCLK falling to CAS* HIGH	2	13	ns
t23	IODATA[15:0]	Hold from IOWR* rising	15		ns
t24	IODATA[15:0]	Set-up to SYSCLK rising	9		ns
t25	IODATA[15:0]	Driven from SYSCLK rising	0	15	ns
t26	IOWAIT*	Set-up to SYSCLK rising	18		ns
t27	DMAREQ*[1:0], PIO[5:0]	Asynchronous Inputs		Asynch	
t28	Reserved				
t29	Reserved				
t30	Reserved				
t31	TEST, EBREQ*	Setup to SYSCLK rising	8		ns
t32	EAS*, EDS*, EDTACK*	Setup to SYSCLK rising	13		ns
t33	EADDIR*, EATOE*	Valid from SYSCLK rising	2	20	ns

Note:
[1] Internal VCLK frequency (divided or not) should be lower than 85% of SYSCLK frequency. Valid only in the SYSCLK during which IODATA is sampled.

DC ELECTRICAL SPECIFICATIONS

(TC= 0-70°C; VDD= +5V, +/- 5%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	
VIL	Input LOW Voltage	-0.5	0.8	V	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IIN	Input Leakage Current	-10	10	uA	VIN = VDD or GND
IOZ	3-State Output Leakage current	-10	10	uA	VOUT = VDD or GND
ICC	Operating Current		200	mA	VDD = 5V, Ta=25C
CINCLK	CLK Input Capacitance		11	pF	
CIN	Input Capacitance		5	pF	

REGISTER MAP AND TABLES—R3715

For the register map and tables in this section, please note:

- Reads and Writes to and from the R3715 internal registers should be word (32-bit) accesses.
- The 0x notations indicate hexadecimal values, as in notations for the C language.
- Bit 0 is the least significant bit.

6

REGISTER MAP

Description	Physical Address	Description	Physical Address
ROM Configuration	0x1d000000	DMA Count 0	0x1d000090
PIO Value	0x1d000040	DMA Count 1	0x1d000094
PIO Control	0x1d000044	DMA Centronics Count	0x1d000098
PIO Read Pins	0x1d00005c	I/O Channel Timing	0x1d0000a0
Timer/Counter Value	0x1d000048	Centronics Status	0x1d000100
Timer/Counter Control	0x1d00004c	Centronics Control	0x1d000104
Interrupt Cause	0x1d000050	Centronics Nibble Data	0x1d000108
Interrupt Mask	0x1d000054	Centronics Host	0x1d00010c
Interrupt Write	0x1d000060	Centronics Mode	0x1d000110
Test	0x1d000064	Centronics Minimum Delay	0x1d000114
DRAM Control	0x1d000058	Centronics Data Detect 0	0x1d0000a4
DMA Address 0	0x1d000080	Centronics Data Detect 1	0x1d0000a8
DMA Address 1	0x1d000084	Centronics Data Detect 2	0x1d0000ac
DMA Centronics Address	0x1d000088		

REGISTER TABLES

The remainder of this section contains register tables for the R3715.

ROM Configuration

This register is used to set the ROM address space for the two configurable ROM banks (ROMCS[1:0]*) and to set the number of wait state cycles inserted between data phases.[1]

Address: 1d000000

Bits	Field name	Function	Initial Value
0-3	First	The gap (number of cycles) from ROMCS* active to the first RDCEN*. 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
4-7	Gap1	The gap between the first RDCEN* and the second RDCEN* 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
8-11	Gap2	The gap between the second RDCEN* and the third RDCEN*. 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
12-15	Gap3	The gap between the third RDCEN* and the fourth RDCEN* 0000 - one cycle 0001 - two cycles n cycles (1 to 16 cycles range)	0xf
16-21	AckTime	The gap from ROMCS* active to AckTime in block read 000000 - one cycle 000001 - two cycles n cycles (1 to 64 cycles range)	0x3f
22-23	SpaceSize	ROMCS[1:0]* address space size (ROMCS[2] has a fixed 4 Mbyte address space) 00 - 8 Mbyte 01 - 4 Mbyte 10 - 2 Mbyte 11 - 1 Mbyte	0x3

NOTE:

[1]It is the user's responsibility to set AckTime timing correctly.

PIO Value

This register is used to set the value for those PIO pins configured by the PIO Control register as outputs.

Address: 1d000040

Bits	Field name	Function	Initial Value
0-5	PIO Value	Value of the PIO pins configured as outputs	0x0

PIO Control

This register sets the direction of the PIO pins.

Address: 1d000044

Bits	Field name	Function	Initial Value
0-5	PIO Control	Sets the direction of the corresponding PIO pin: 0 - Output 1 - Input	0x3f
6	Reserved	Must be 0	0

PIO Read Pins

This address is used to read inputs from the PIO pins.

Address: 1d00005C

Bits	Field name	Function	Initial Value
0-5	PIO Input Value	Value on the PIO pins	

Timer/Counter Value

This register is used to set the number of clocks to be counted by the Timer/Counter.

Address: 1d000048

Bits	Field name	Function	Initial Value
0-23	T/C Value	Number of clocks to count. Set to n to count to n.	0x000000

Timer/Counter Control

This register is used to enable and disable the Timer/Counter and to select the specific mode of use.

Address: 1d00004c

Bits	Field name	Function	Initial Value
0	Enable	Timer/Counter count enable 0 - Disable 1 - Enable	0x0
1	Select	Select mode of operation 0 - Counter 1 - Timer	0x0

Interrupt Cause

This register is used to identify the source behind an interrupt; it can also be used for polling of a specific interrupt or set of interrupts. A value of 1 indicates assertion of the interrupt. This register is also used to clear internal interrupts, writing a 0 will reset the corresponding internal interrupt. Writing a 1 will have no effect on the interrupt. External interrupts should be cleared via an external mechanism.

Address: 1d000050

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

Interrupt Mask

This interrupt is used to mask (disable) specific interrupt sources, both internal and external (PIO). All the interrupts are maskable. A value of 0 masks the corresponding interrupt.

Address: 1d000054

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CenRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	
17-19	Reserved		
20-25	PIOInt[5:0]	Programmable external interrupts (read only) Bit 20 = PIOInt[0], etc.	

Interrupt Write

This register is used to write to the Interrupt Cause register. This register should be used for interrupt testing only.

Address: 1d000060

Bits	Field name	Function	Initial Value
0	Reserved		
1	Reserved		
2	Reserved		
3	Reserved		
4	TimInt	Timer/Counter interrupt	
5-6	IODMAInt[1:0]	I/O Channel end-of-DMA interrupts Bit 5 = Channel 0 Bit 6 = Channel 1	
7	CentDMAInt	Centronics end-of-DMA interrupt	
8	Reserved		
9	Reserved		
10	Reserved		
11	CentRstInt	Centronics reset interrupt	
12	CentWrInt	Centronics write interrupt	
13	CentRdInt	Centronics read interrupt	
14-16	EqualInt	Centronics equal interrupts Bit 14 = Centronics Data Detect 0 Bit 15 = Centronics Data Detect 1 Bit 16 = Centronics Data Detect 2	

Test

No reading or writing from/to this address. Doing so may result in improper generation of this device.

Address: 1d000064

DRAM Control

This register is used to set the desired DRAM device depth, access time (both for the CPU and external DMA master) and refresh frequency.

Address: 1d000058

Bits	Field name	Function	Initial Value
0-2	DevDepth Bank 1-2	Depth of the DRAM device used, in words. 000 - 256K 001 - 512K 010 - 1M 011 - 2M 100 - 4M	0x0
3-4	DevDepth Bank 0	Depth of the DRAM device used, in words. 00 - 256K 01 - 512K 10 - 1M 11 - 2M	0x0
5	ExtCas	CAS duration for both CPU and external DMA master accesses. 0 - CAS is active for one and a half cycles 1 - CAS is active for two and a half cycles	0x0
6	ExtCas	CAS duration for external DMA master accesses only. 0 - CAS is active in external DMA master accesses for one and a half cycles 1 - CAS is active in external DMA master accesses for two and a half cycles	0x0
7-8	RefFreq	SYSCLK frequency. 00 - 15.6 uS refresh time at 16MHz 01 - 15.6 uS refresh time at 20MHz 10 - 15.6 uS refresh time at 25MHz 11 - 15.6 uS refresh time at 33MHz	0x0

DMA Address 0

This register is used to set the first DRAM address used in channel 0 DMA operations.

Address: 1d000080

Bits	Field name	Function	Initial Value
0-25	DmaAddr0	First address for DMA channel 0.	0x0

DMA Address 1

This register is used to set the first DRAM address used in channel 1 DMA operations.

Address: 1d000084

Bits	Field name	Function	Initial Value
0-25	DmaAddr1	First address for DMA channel 1.	0x0

DMA Centronics Address

This register is used to set the first DRAM address used in Centronics DMA operation.

Address: 1d000088

Bits	Field name	Function	Initial Value
0-25	DmaAddrCent	First address for Centronics DMA.	0x0

DMA Count 0

This register is used to set the number of bytes to be transferred in a channel 0 DMA operation.

Address: 1d000090

Bits	Field name	Function	Initial Value
0-15	DmaCnt0	DMA count channel 0. Load with n-1 to transfer n.	0x0

DMA Count 1

This register is used to set the number of bytes to be transferred in a channel 1 DMA operation.

Address: 1d000094

Bits	Field name	Function	Initial Value
0-15	DmaCnt1	DMA count channel 1. Load with n-1 to transfer n.	0x0

DMA Centronics Count

This register is used to set the number of bytes to be transferred in a Centronics DMA operation.

Address: 1d000098

Bits	Field name	Function	Initial Value
0-15	DmaCntCen	Centronics DMA count. Load with n-1 to transfer n.	0x0

I/O Channel Timing

This register is used to configure the I/O bus parameters, including signal timing; DMA enabling, time-out, and direction; and the endianess of the 16-bit I/O channels. The DevTime fields specify the number of cycles IORD* or IOWR* are asserted in an I/O or DMA access. The Time Out Enable (TOEn) field chooses between inserting 32 clock cycles between arbitration cycles or not; normally, enabling this bit results in better system performance.

Address: 1d00000a0

Bits	Field name	Function	Initial Value
0-3	DevTime0	8-bit I/O channel 0 (IOCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
4	DmaEn0	DMA enable 8-bit channel 0. 0 - DMA disable 1 - DMA enable	0x0
5	DmaR/W0	DMA Read or Write 8-bit channel 0. 0 - DMA write 1 - DMA read	0x0
6-9	DevTime1	8-bit channel 1 (IOCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
10	DmaEn1	DMA enable 8-bit channel 1. 0 - DMA disable 1 - DMA enable	0x0
11	DmaR/W1	DMA Read or Write 8-bit channel 1. 0 - DMA write 1 - DMA read	0x0
12-15	CenTime	Centronics external register access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
16	DmaEnCen	Centronics DMA enable. 0 - DMA disable 1 - DMA enable	0x0
17	DmaR/WCen	DMA Read or Write for the Centronics interface. 0 - DMA write 1 - DMA read	
18-21	DevTime3	16-bit I/O channel 0 (IOGPCS0*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
22-25	DevTime4	16-bit I/O channel 1 (IOGPCS1*) access time. 0000 - one cycle 0001 - two cycles n - n+1 cycles (1 to 16 cycles range)	0x0
26	BigEndian0	Big or Little Endian for the 16-bit I/O channel 0 0 - Big Endian 1 - Little Endian	0x0
27	BigEndian1	Big or Little Endian for the 16-bit I/O channel 1 0 - Big Endian 1 - Little Endian	0x0
28	TOEn	Time Out Enable for both DMA channels 0 - Time out disabled, time out is 0 clocks 1 - Time out enabled, time out is 32 clocks	0x0

Centronics Status

This register is used to implement the Centronics hand-shake protocol via software by the CPU.

Address: 1d000100

Bits	Field name	Function	Initial Value
0	Busy	Busy indication 0 - Ready 1 - Busy	0x0
1	Ack	Acknowledge 0 - acknowledge 1 - Normal	
2	Fault	Fault indication 0 - Fault 1 - Normal	
3	Select	Select 0 - Off line 1- On line	
4	Perror	Paper Error indication 0 - No error 1- Error	

Centronics Control

This register is used to set the Centronics transfer mode per the IEEE 1284 specification Rev. 2.

Address: 1d000104

Bits	Field name	Function	Initial Value
0-2	Mode	IEEE 1284 modes 000 - Compatible 001 - Nibble 010 - Byte 011 - ECP 100 - EPP 101 - CPU control 110 - extensibility link 111 - termination	0x0
3	NegRep	Negotiation Reply All modes except nibble mode: 0 - mode requested by host is not supported by the peripheral 1- mode requested is supported Nibble mode: 0- mode requested by host is supported by the peripheral 1- mode requested is not supported	0x0

Centronics Nibble Data

This register is used to post the data to be transferred in nibble mode.

Address: 1d000108

Bits	Field name	Function	Initial Value
0-7	NibData	Nibble mode Centronics data to be sent to the host	

Centronics Host

This register is used to read inputs from the host in the Centronics protocol pins.

Address: 1d00010c

Bits	Field name	Function (In compatible mode)	Initial Value
0	Strobe	Set LOW by the host to transfer data	
1	SelectIn	Set LOW by host to select printer	
2	Init	Pulsed LOW with SelectIn active LOW to reset the Centronics interface	
3	AutoFd	Set LOW by the host to put the printer in auto-feed mode.	

Centronics Mode

This register is used to set the Centronics DMA parameters and select the protocol options in Compatible mode.

Address: 1d000110

Bits	Field name	Function	Initial Value
0-1	Application	See IEEE 1284 standard for details 00 - Standard 01 - IBM Epson 10 - Reserved 11 - Classic	
2	DmaEn	0 - transmission executed by CPU 1 - transmission executed by DMA	
3	DmaDir	0 - DMA write 1 - DMA reads	

Centronics Minimum Delay

This register contains the values that are needed for each operating frequency to comply with the IEEE 1284 standard (minimum of 500ns and 2500ns). However for systems with higher performance requirements, it is possible to program the minimum delays for lower values.

Address:1d000114

Bits	Field name	Function	Initial Value
0-6	2500ns	16MHz - 0x28	
		20MHz - 0x32	
		25MHz - 0x3f	
		33MHz - 0x53	
7-13	500ns	16MHz - 0x08	
		20MHz - 0x0a	
		25MHz - 0x0d	
		33MHz - 0x11	

Centronics Data Detect 0

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000a4

Bits	Field name	Function	Initial Value
0-7	DataDet0	Data to be used for comparison with the incoming data.	

Centronics Data Detect 1

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000a8

Bits	Field name	Function	Initial Value
0-7	DataDet1	Data to be used for comparison with the incoming data.	

Centronics Data Detect 2

This register is used to hold a value to be compared against incoming bytes. In case of a match, an interrupt will be issued. The corresponding interrupt can be masked in the Interrupt Mask register.

Address: 1d0000ac

Bits	Field name	Function	Initial Value
0-7	DataDet2	Data to be used for comparison with the incoming data.	

EXTERNAL ADDRESS SPACE

The address space allocated to the different resources in the system is shown in Table 4.1. Bits 29-31 are not decoded so that physical aliases of 512 Mbyte are created. This enables the software to access the same system resource using different attributes (i.e cached space vs. uncached space, kernel vs. user).

Description	Size	Physical Address Range[1]
DRAM	40M	0X00000000: 0x027FFFFF
ROMCS[2]*.	4M	0x1FC00000: 0x1FFFFFFF
ROMCS[1]*	8M	0x1F400000: 0x1FBFFFFF
ROMCS[0]*	8M	0x1EC00000: 0x1F3FFFFF
IO channel 0	16M	0x08000000: 0x08FFFFFF
IO channel 1	16M	0x09000000: 0x09FFFFFF
IO channel 2	16M	0x0B000000: 0x0BFFFFFF
IO channel 3	256M	0x0C000000: 0x1BFFFFFF
Centronics external register	1M	0x0A000000: 0x0A0FFFFF
External DMA master address space	16M	0x1C000000: 0x1CFFFFFF
Internal registers	16M	0x1D000000: 0x1DFFFFFF

Table Note: [1]This column specifies maximum range.

Table 4.1 External Address Space

6

IMPLEMENTATION EXAMPLES

Full Implementation

A possible implementation of a fully featured system is shown in Figure 5.1. This system includes a 2-way interleaved ROM array, and uses external multiplexers (FCT257x8) that are controlled by MUX_ADDR[2] to choose one bank or the other. The R3715 directly provides the output enable signal to these multiplexers (ROMOE*), as well as the chip select signal to the ROM banks (ROMCS*[2:0]).

The control to the DRAM banks is provided directly by signals coming out of the R3715. These signals can directly control up to 3 banks of DRAM and 40MB. This implementation supports an external DMA master, and so an extra set of latches and transceivers are used to accommodate it. All control signals necessary to provide DMA master and slave operations to the external DMA master are provided. Multiplexing between the external DMA master and CPU is done via BUSGNT*.

The R3715 video/engine interface processes line and page synchronization signals from the engine and provides it with a serial video data stream.

The R3715 also generates the control signals necessary to transfer parallel byte or word data to and from the parallel interface (POE* and PSTROBE*).

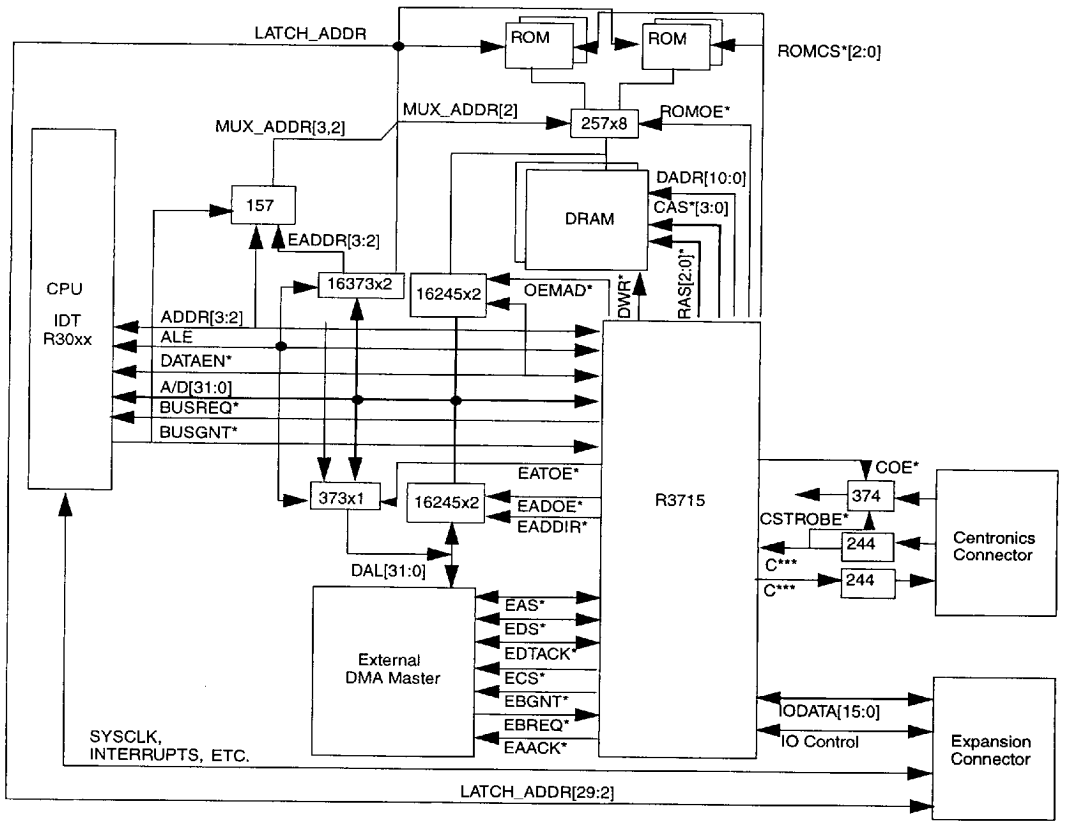


Figure Note: C***=Centronics Control Signals

Figure 5.1 Full Implementation With Interleaved ROM

A full complement of signals is provided by the R3715 to implement an IEEE1284 bi-directional Centronics interface.

The 80186-style I/O bus interfaces to a connector that can be used to expand features by adding standard industry peripherals like SCSI, PCMCIA cards, UARTs, Ethernet, etc.

Minimal Implementation

Figure 5.2 shows a minimal implementation. In this case, we show the lower end CPU in the R3051 Family, the R3041.

A simple non-interleaved ROM subsystem is used in this case, with only 1 bank - the boot bank ROMCS[2]*.

The DRAM system contains only 1 bank and as we mentioned before, the R3715 directly provides all the necessary signals.

Since a coprocessor is not used in this case, the interface to the AD bus is very simple.

The balance of the features shown is the same, but this could conceivably include simpler implementations of each, like less peripherals via the IODATA bus, or a lower video rate that could be associated with an engine with less dots per inch or less pages per minute.

Both the full and the minimal implementations shown demonstrate the flexibility of the R3715 as a common block that enables modular designs or designs that can be upgraded in the field.

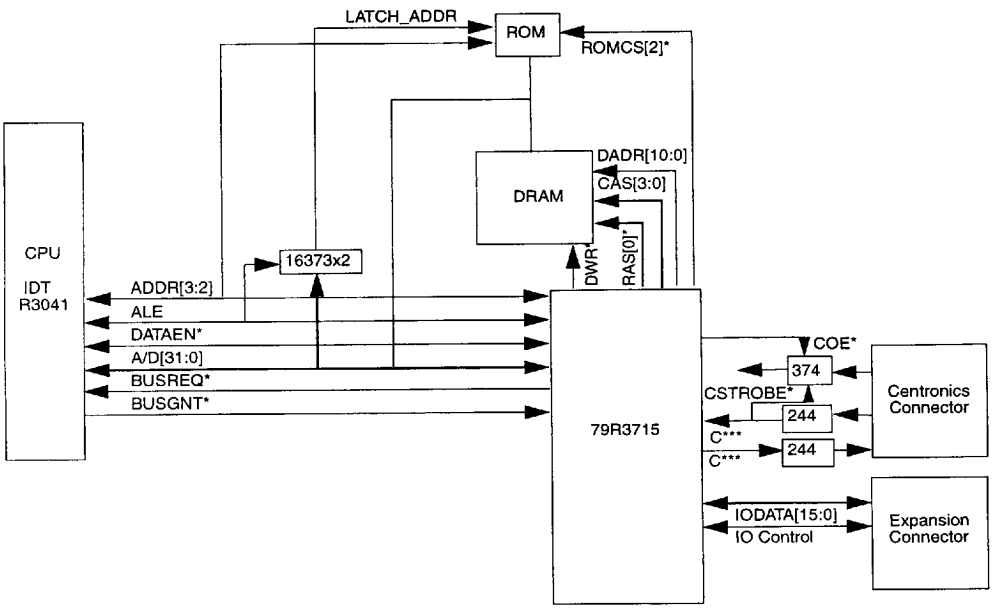


Figure Note: C***=Centronics Control Signals

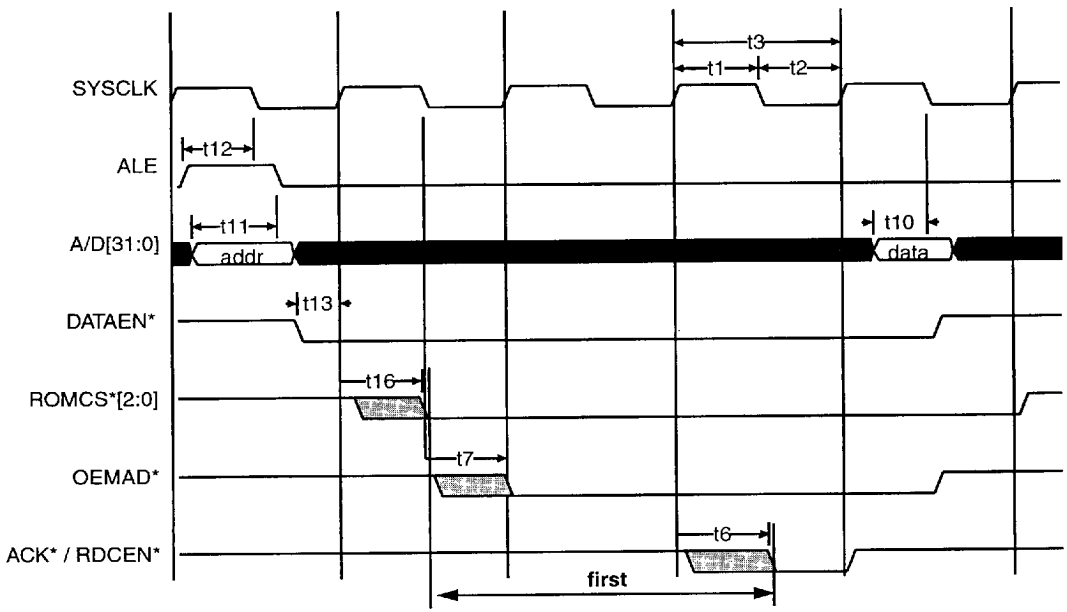
Figure 5.2 Minimal Implementation

PINOUT TABLE

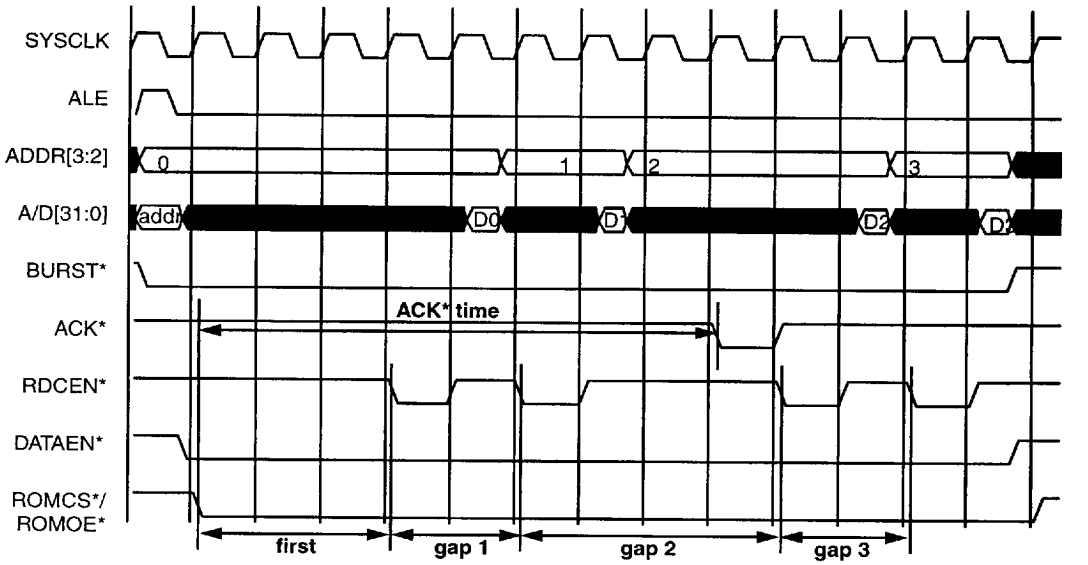
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	AD(14)	41	EAS*	81	IOBE(1)*	121	RAS*[0]
2	AD(13)	42	ECS*	82	IOBE(0)*	122	RAS(1)*
3	AD(12)	43	EAACK*	83	IOGPCS[1]*	123	RAS(2)*
4	AD(11)	44	PIO(0)	84	IOGPCS[0]*	124	CAS(0)*
5	AD(10)	45	PIO(1)	85	IOCS(1)*	125	CAS(1)*
6	VDD	46	PIO(2)	86	IOCS(0)*	126	CAS(2)*
7	VSS	47	PIO(3)	87	DMAREQ(0)	127	CAS(3)*
8	AD(9)	48	PIO(4)	88	DMAREQ(1)	128	DWR*
9	AD(8)	49	PIO(5)	89	IODATA(15)	129	ROMCS(2)*
10	AD(7)	50	CSELECTIN*	90	IODATA(14)	130	VDD
11	AD(6)	51	CINIT*	91	IODATA(13)	131	VSS
12	AD(5)	52	CSTROBE*	92	IODATA(12)	132	ROMCS(1)*
13	AD(4)	53	CRSTROBE	93	IODATA(11)	133	ROMCS(0)*
14	AD(3)	54	CBUSY	94	IODATA(10)	134	ROMOE*
15	AD(2)	55	VDD	95	IODATA(9)	135	Reserved
16	AD(1)	56	SYSCLK	96	IODATA(8)	136	Reserved
17	AD(0)	57	VSS	97	IODATA(7)	137	Reserved
18	VDD	58	CWSTROBE	98	IODATA(6)	138	Reserved
19	VSS	59	CROE*	99	IODATA(5)	139	AD(31)
20	VSS	60	VDD	100	IODATA(4)	140	AD(30)
21	BURST*	61	CAUTOFD*	101	VDD	141	AD(29)
22	ADDR(3)	62	CPERROR	102	VDD	142	AD(28)
23	ADDR(2)	63	CSELECT	103	VSS	143	VSS
24	ALE	64	CWOE*	104	IODATA(3)	144	AD(27)
25	RD*	65	CACK*	105	IODATA(2)	145	AD(26)
26	WR*	66	CFAULT*	106	IODATA(1)	146	AD(25)
27	DATAEN*	67	POE*	107	IODATA(0)	147	AD(24)
28	BUSGNT*	68	PSTROBE*	108	DADR(10)	148	AD(23)
29	RESET*	69	N.C.	109	DADR(9)	149	AD(22)
30	ACK*	70	N.C.	110	DADR(8)	150	VDD
31	RDCEN*	71	N.C.	111	DADR(7)	151	VSS
32	BUSREQ*	72	N.C.	112	VDD	152	AD(21)
33	INT*	73	VDD	113	VSS	153	AD(20)
34	EADOE*	74	VSS	114	DADR(6)	154	AD(19)
35	EADDIR*	75	IOWAIT*	115	DADR(5)	155	AD(18)
36	EATOE*	76	DMAACK(1)*	116	DADR(4)	156	AD(17)
37	EDTACK*	77	DMAACK(0)*	117	DADR(3)	157	AD(16)
38	EDS*	78	IOWR*	118	DADR(2)	158	AD(15)
39	EBREQ*	79	IORD*	119	DADR(1)	159	OEMAD*
40	EBGNT*	80	IOA1	120	DADR(0)	160	TEST

TIMING DIAGRAMS

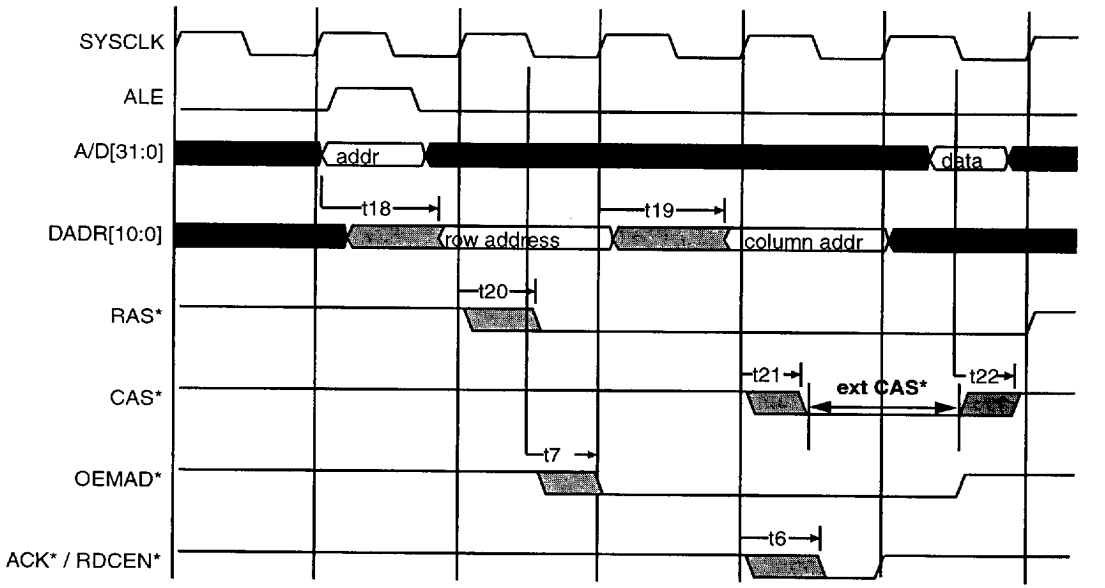
This section contains timing diagrams for the R3715 signals.



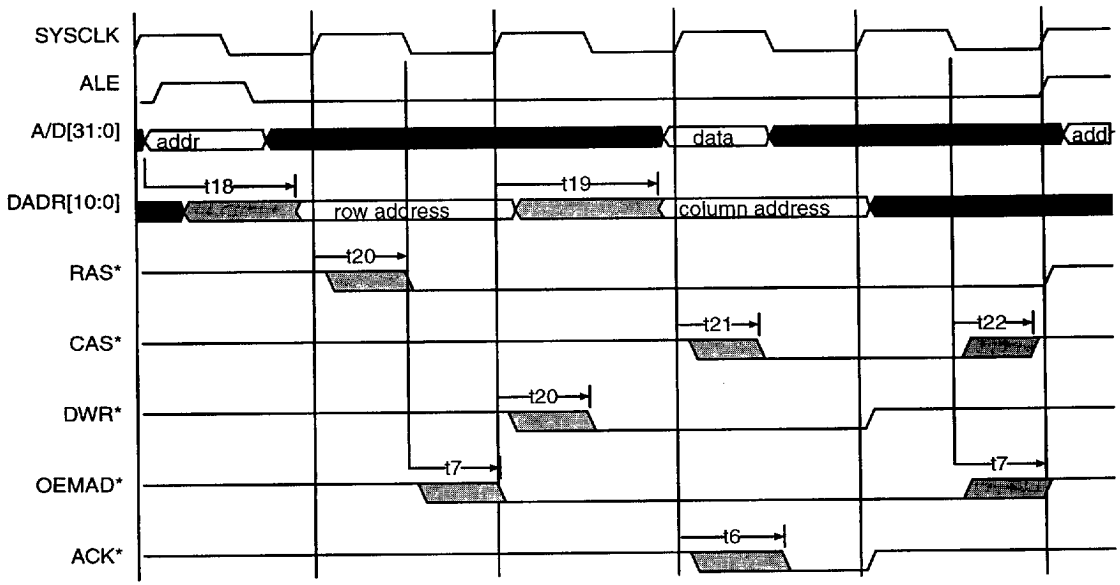
ROM Read (Programmable)



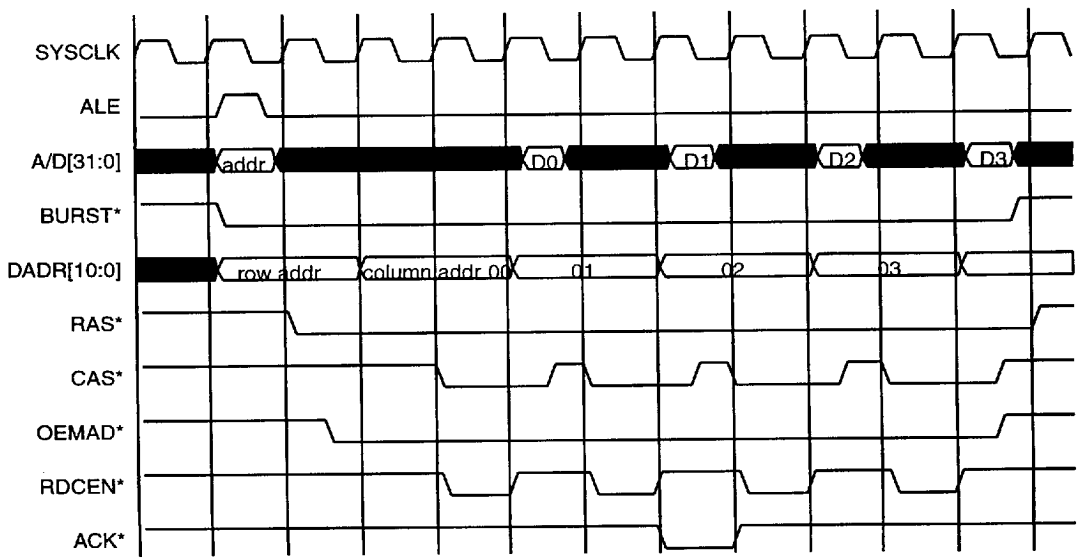
Interleaved ROM Burst Read (Programmable)



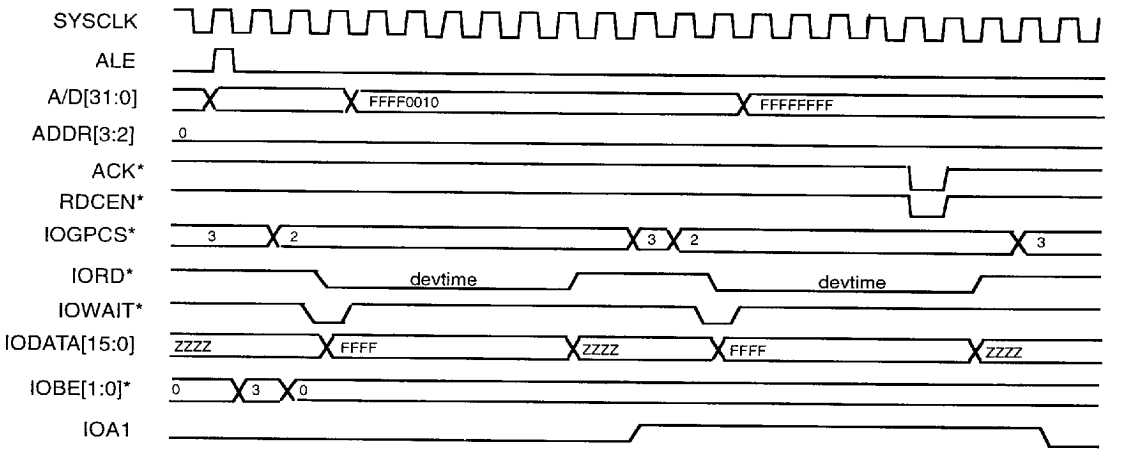
DRAM Read (Programmable)



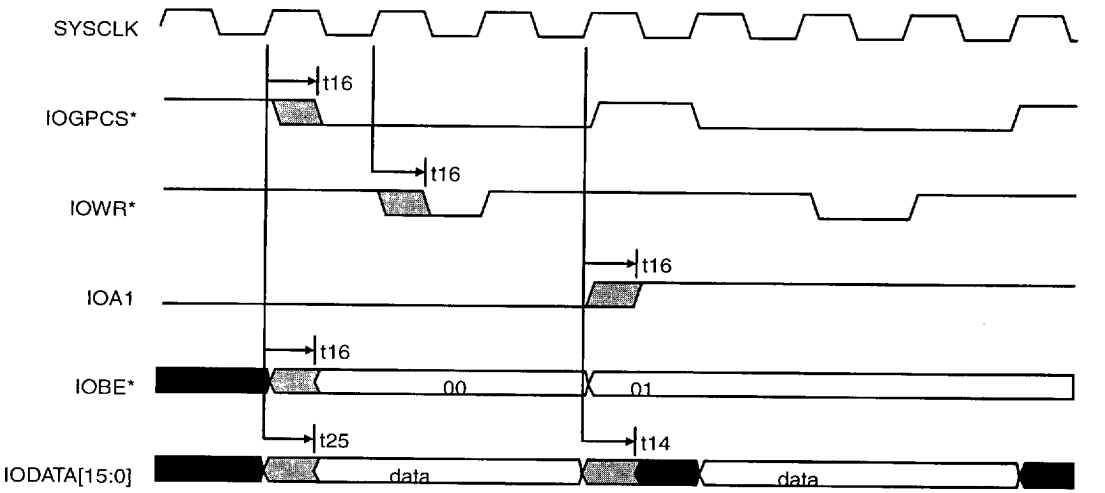
DRAM Write



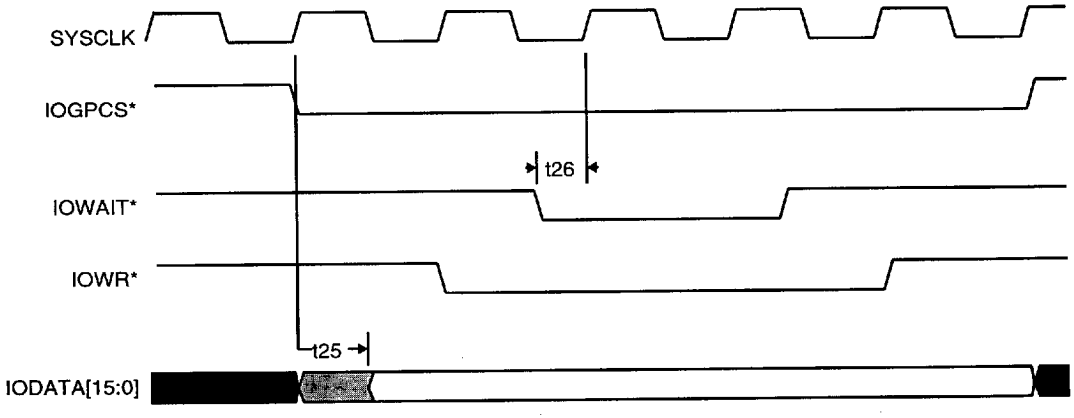
DRAM Burst Read



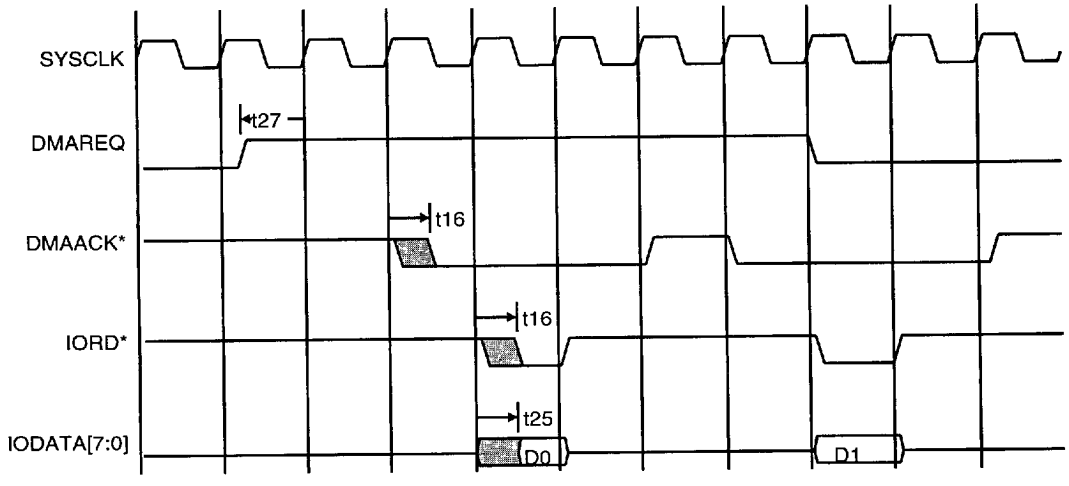
I/O Read 16-Bit



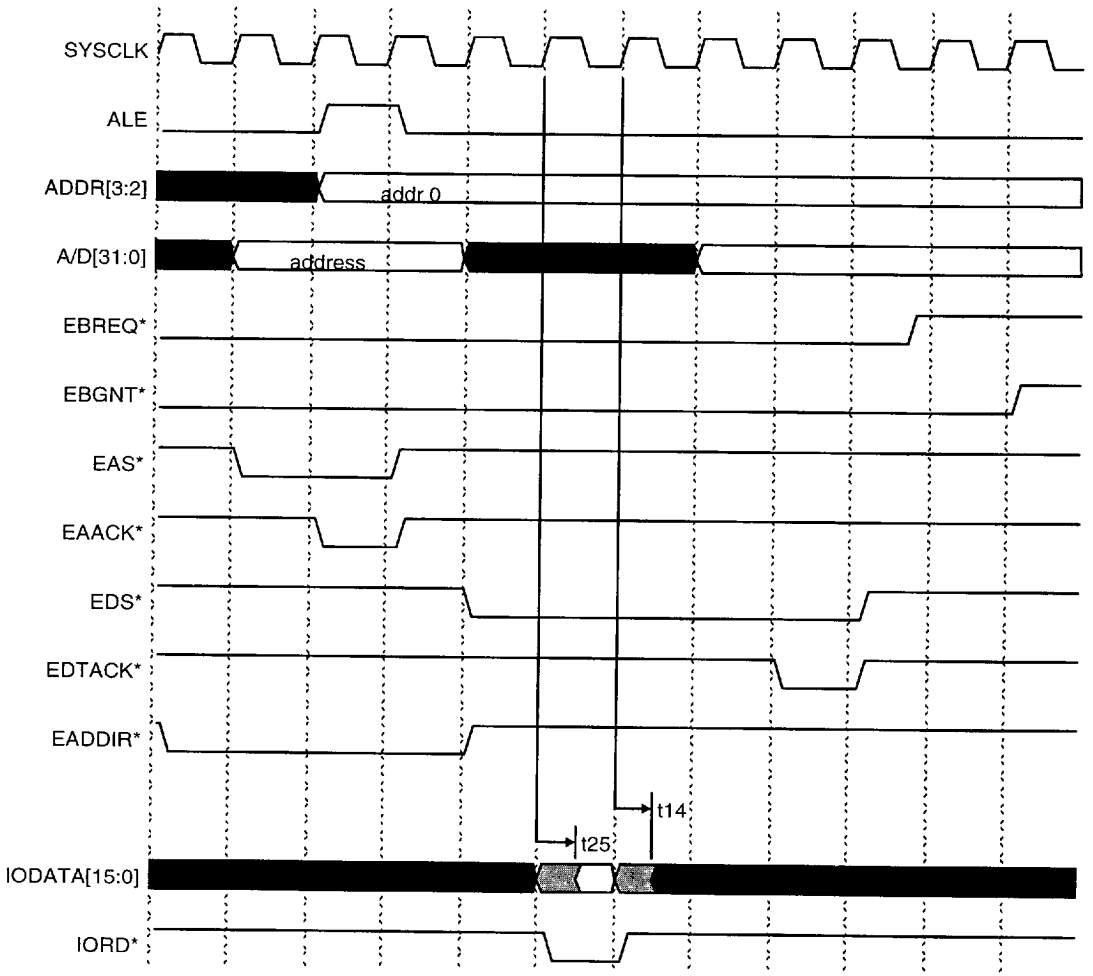
I/O Write 24-Bit



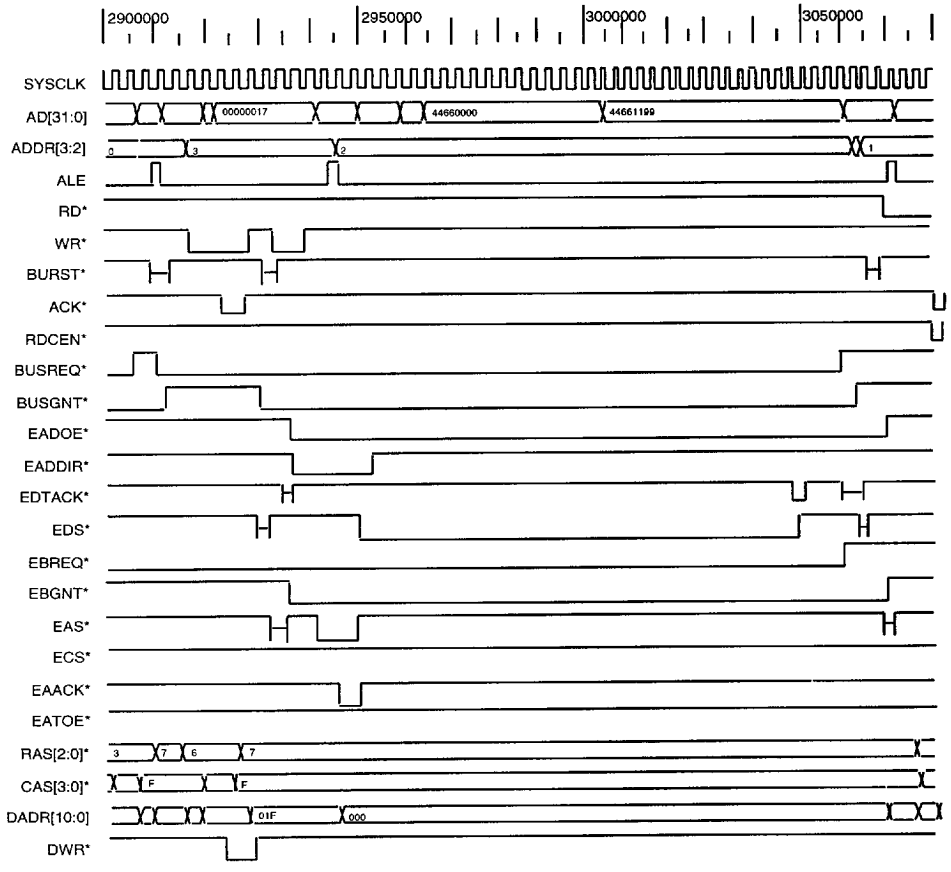
I/O Write (With Wait State)



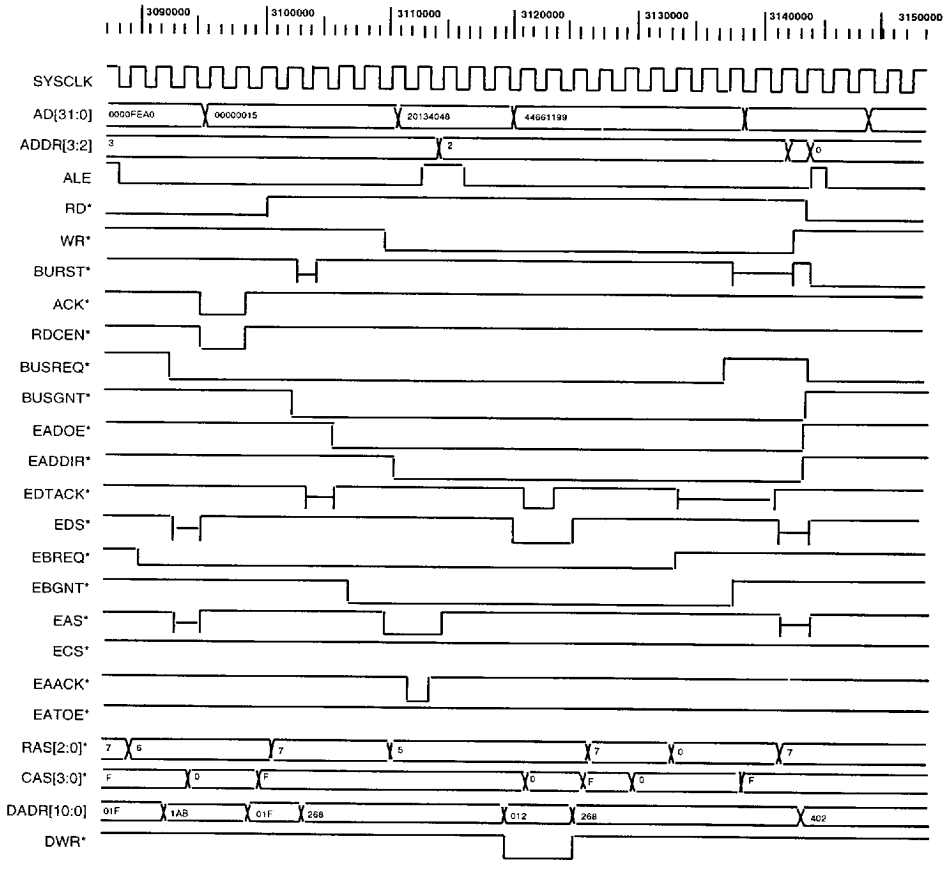
I/O Bus DMA Read



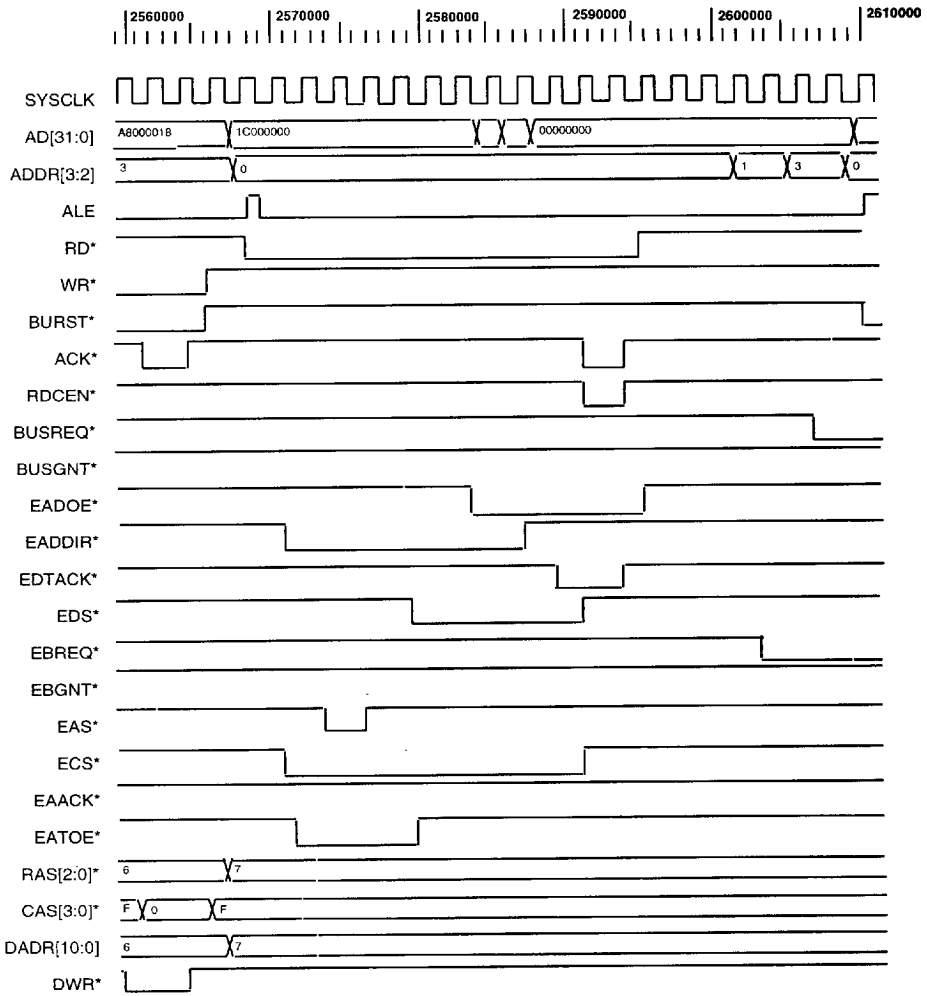
External DMA Master— Master I/O Read



External DMA Master— Master Read

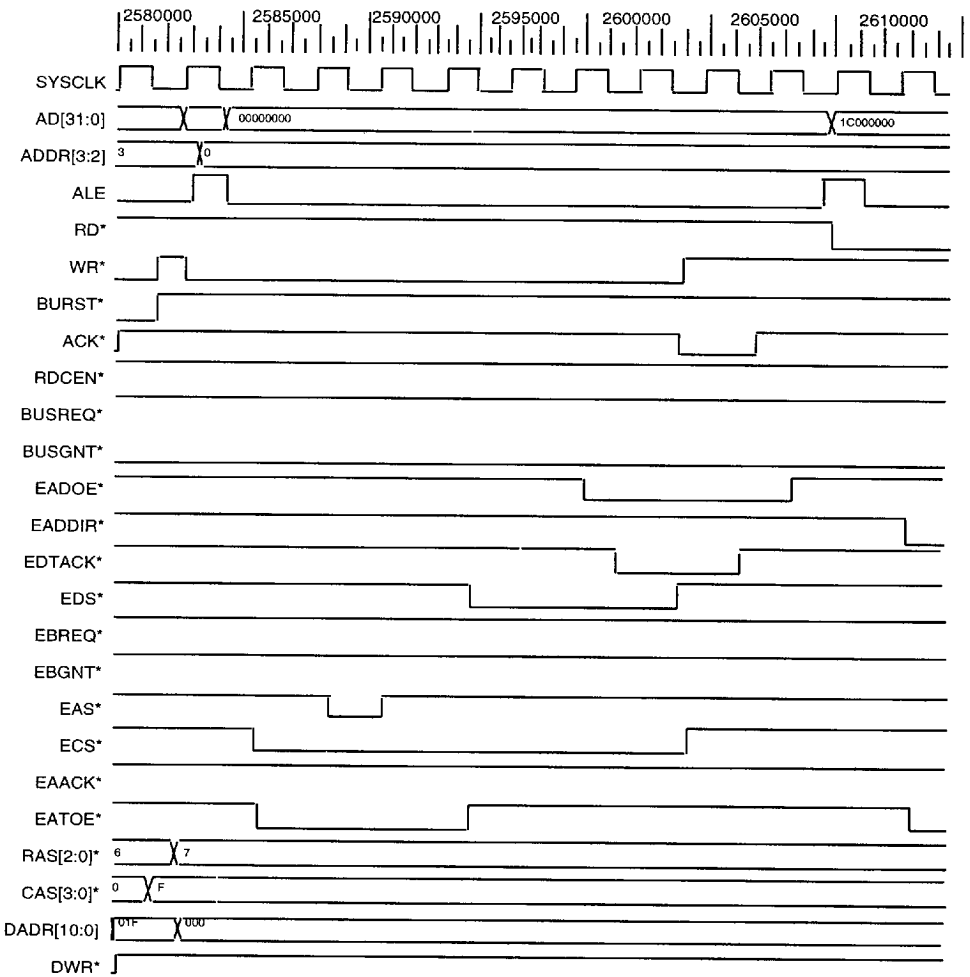


External DMA Master— Master Write

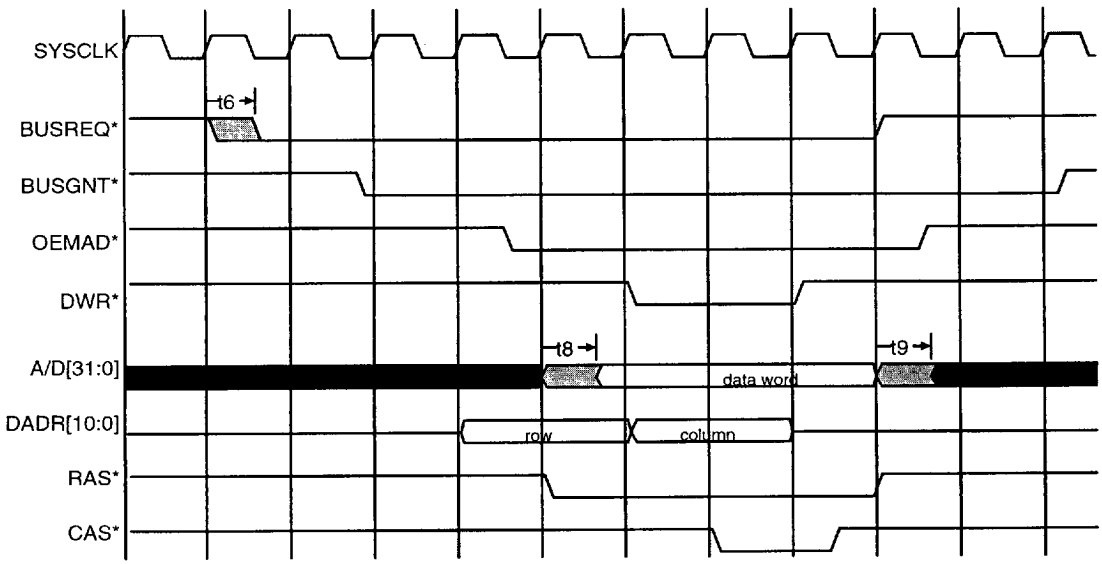


External DMA Master— Slave Read

6

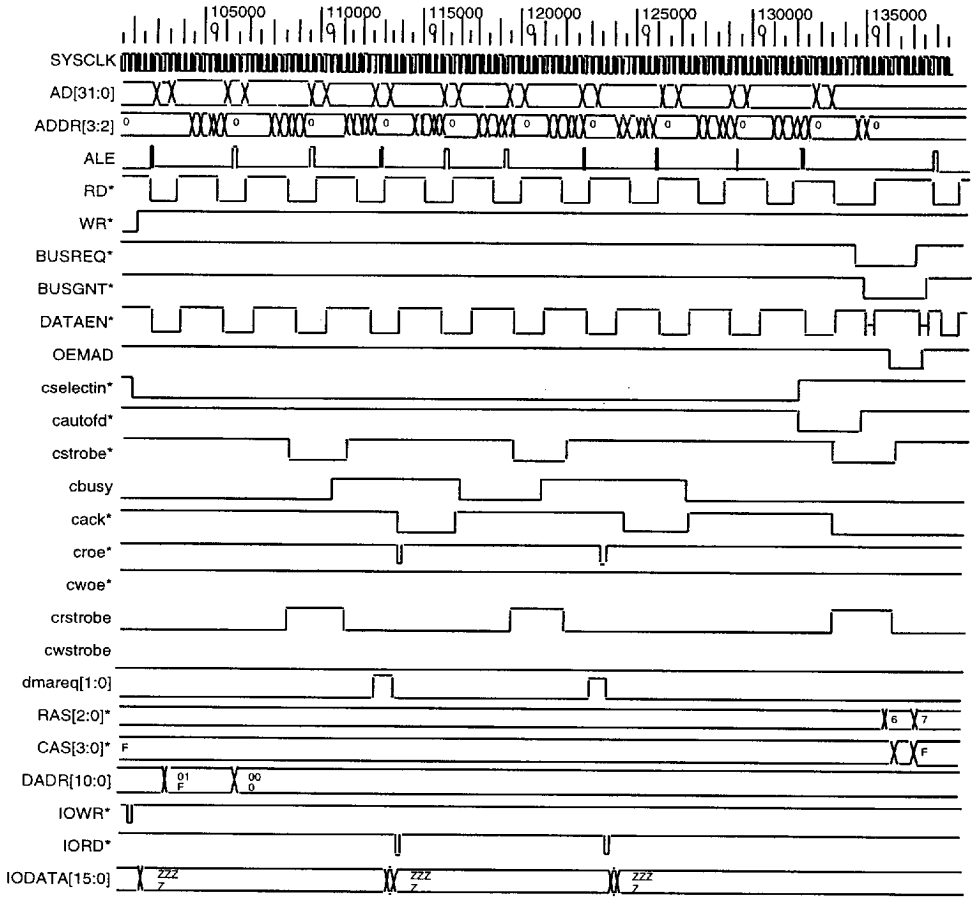


External DMA Master— Slave Write

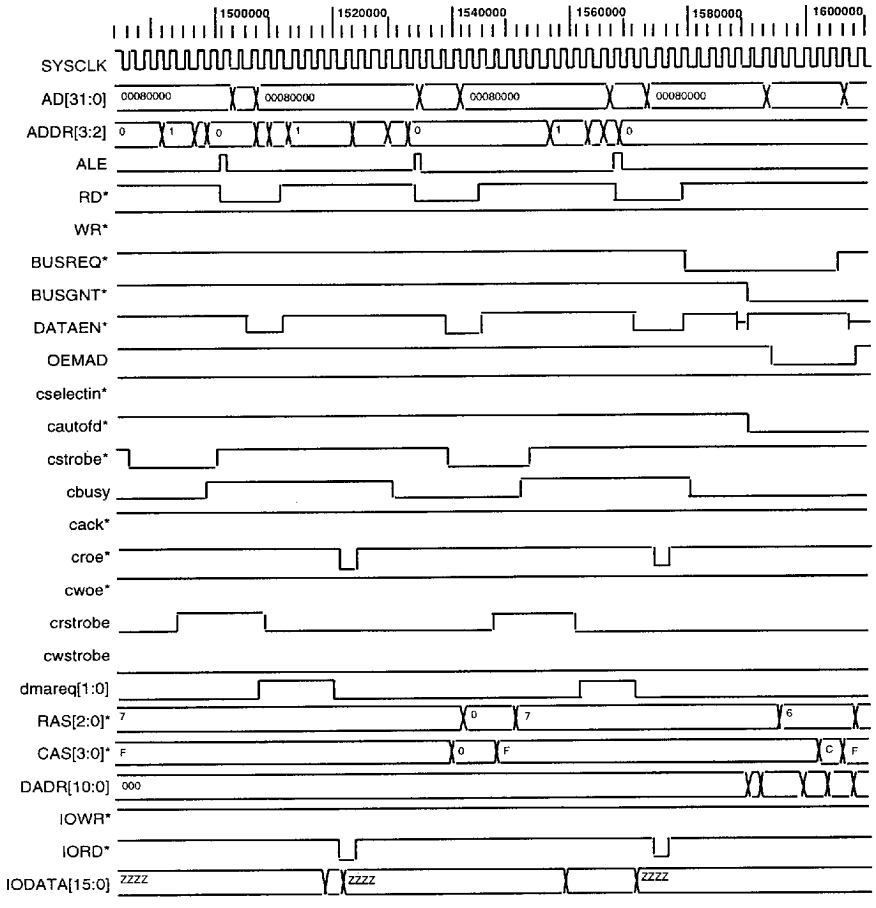


A/D Bus DMA Write

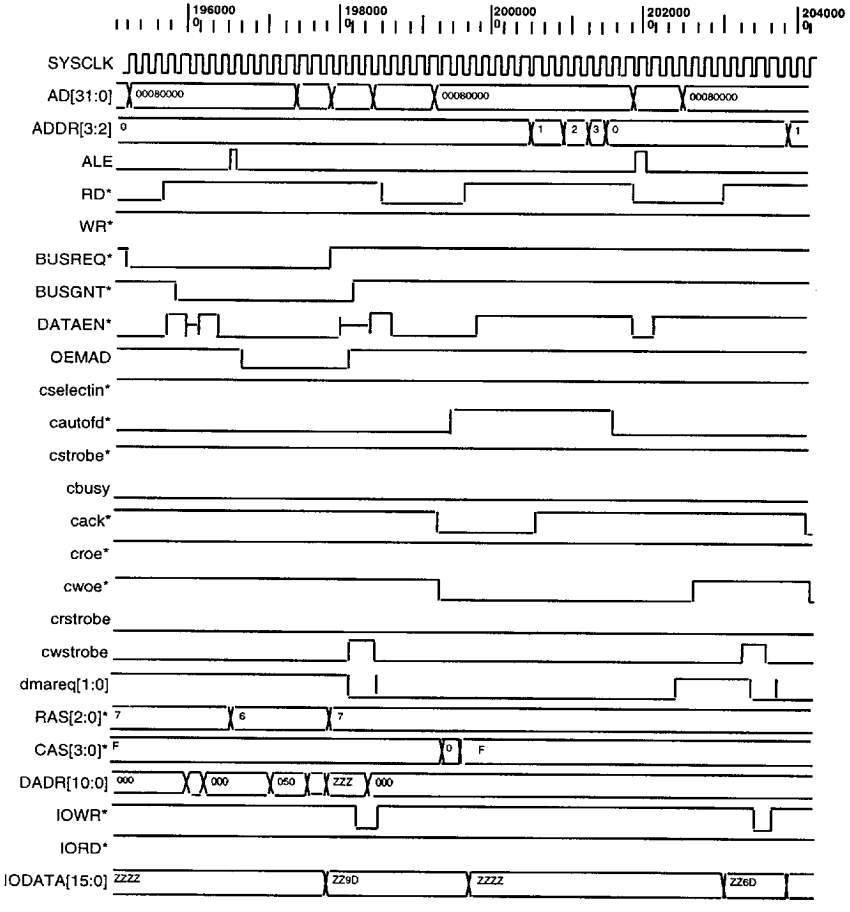
6



Centronics Compatible DMA—Standard
(Application=00)



ECP Forward Transfer



ECP Reverse Transfer

PACKAGE

160-Pin Quad Flat Package (QFP, EIAJ)

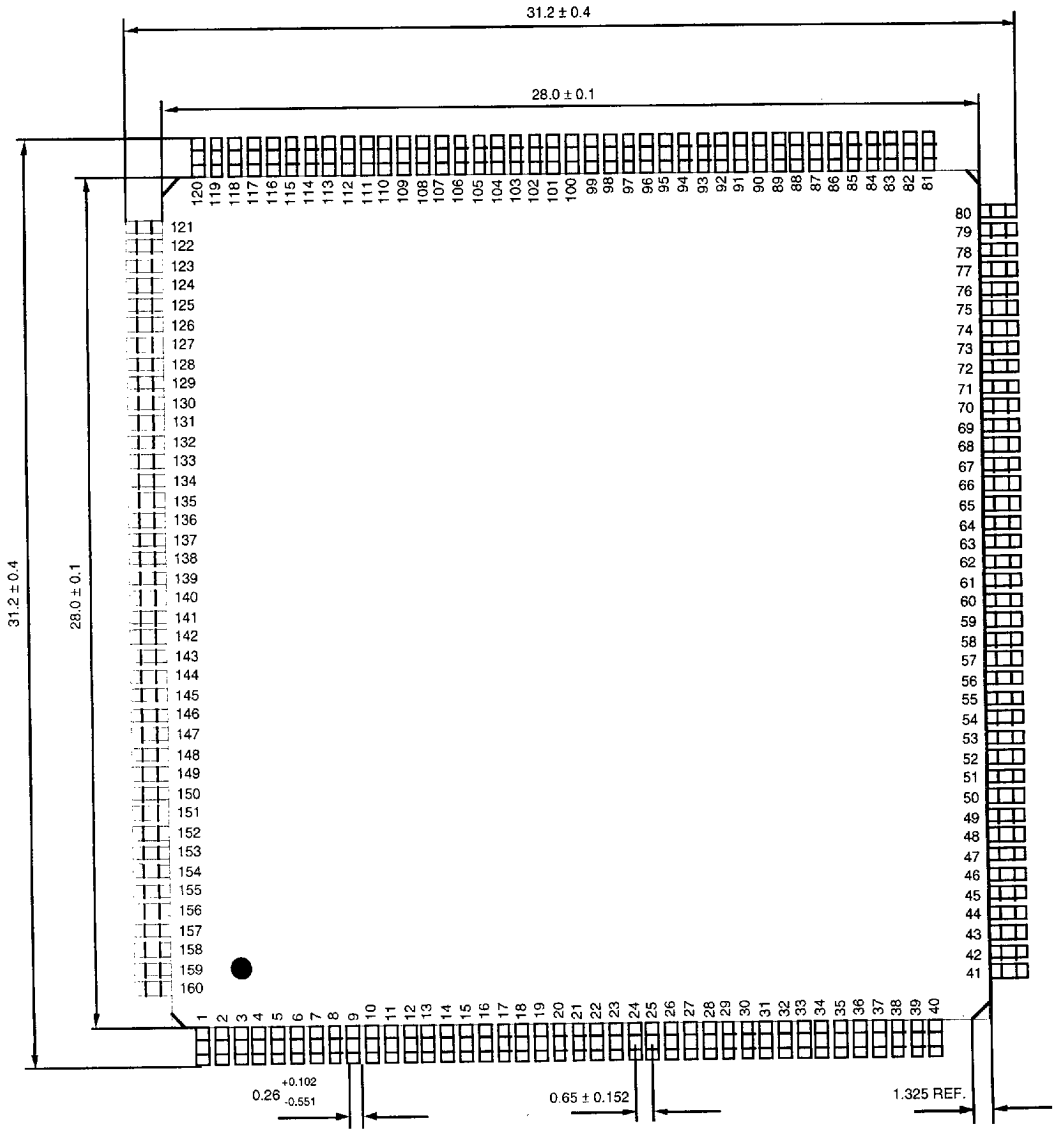


Figure 10.1 160-Pin Quad Flat Package

3134 drw 03

160 - Pin Quad Flat Package—Expanded View (QFP, EIAJ)

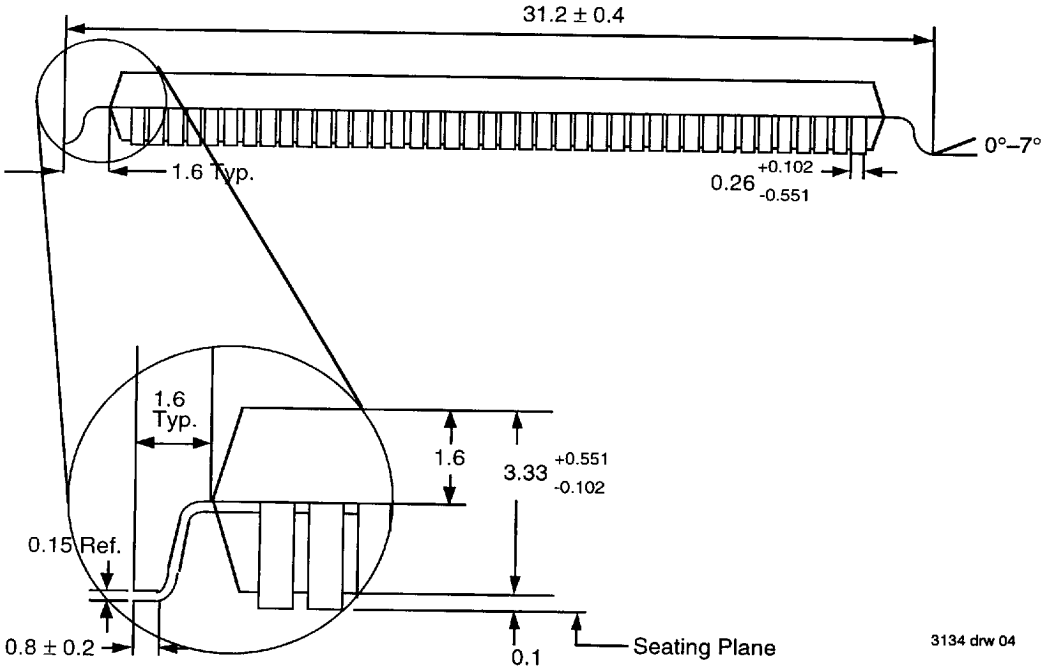


Figure 10.2 Expanded View of Figure 10.1 Detail

VALID COMBINATIONS

79R3715PF	160-pin PQFP