Advanced 64-bit Microprocessors Product Family

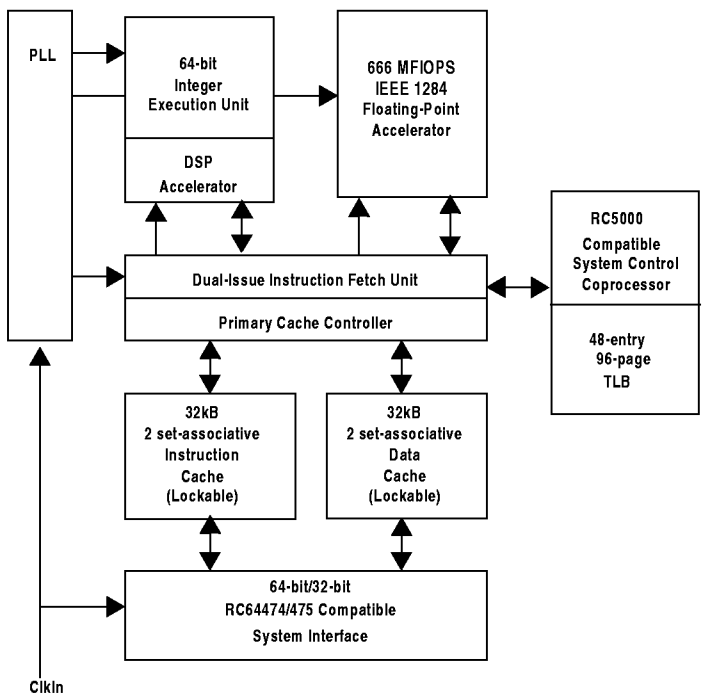
RC64574™
RC64575™
Preliminary Information*

RISController

Features

- **High-performance 64-bit embedded Microprocessor**
  - *333MHz operating frequency*
  - *>440 Dhrystone MIPS performance*
  - *666MFLOPS/s floating-point performance*
  - *Up to 125 million multiply accumulate per second (MAC/s)*
  - *MIPS-IV Instruction Set Architecture (ISA), with integer DSP and 3-operand integer multiply extensions*
  - *Limited dual-issue microarchitecture*
- **Compatible with RC4640 and RC32364 DSP extensions**
  - *DSP Extensions, for consumer applications*
  - *2-cycle repeat rate, on atomic Multiply-add*
  - *Multiply-subtract (MSUB) support, for complex number processing*
  - *Count-leading-zero/one support, for string searches and normalization*
- **High-performance on-chip cache subsystem**
  - *32kB, two-set associative instruction cache (I-cache)*
  - *32kB, two-set associative data cache (D-cache)*
  - *Write-through and write-back data cache operations*
  - *High-performance cache-ops, bandwidth management*
- **I-cache and D-cache locking capability (per line), provides improved real-time support**
- **Joint TLB on-chip, for virtual-to-physical address mapping**
- **Big- or Little-endian capability**
- **RC5000 compatible memory management**
  - *On-chip 48-entry, 96-page TLB, for advanced operating system support*
  - *Compatible with major operating systems: Windows®CE, VxWorks, and others*
- **Bus compatible with IDT 64-bit microprocessor families**
  - *Pipeline runs at 2 to 8 times the bus frequency*
  - *Bus speeds to 125MHz*
  - *32-bit bus option, for lower cost systems*
  - *Enhanced timing protocol for SyncDRAM systems (compatible with IDT79RC64474/475)*
- **RC64574:**
  - *32-bit SysAd bus, for low-cost systems*
  - *Pin compatible with RC4640 and RC64474*
  - *128-pin QFP package*
- **RC64575:**
  - *64-bit SysAd bus interface*
  - *Pin compatible with RC4650 and RC64475*
  - *208-pin QFP package*
- **JTAG Boundary Scan Interface**
- **2.5V operation with 3.3V tolerant I/O**

Block Diagram



*Notice: The information in this document is subject to change without notice

Device Overview[1]

IDT's 79RC64574/575 processors serve a wide range of performance-critical embedded applications that include high-end internetworking systems, digital set-top boxes, web browsers, color printers, and graphics terminals.

The RC64574/575 allow a socket compatible upgrade path for IDT's RC4640/50 and RC64474/475 processors. This unprecedented upgradability allows a 2:1 range of frequencies; 4:1 range of cache size; 15:1 range of floating-point; and 4:1 range of DSP performance in a single socket.

With special emphasis on system bandwidth, floating- point and DSP operations, the RC64574/575 have been optimized for high-performance applications through the integration of high-performance computational units and a high-performance memory hierarchy. The result is a low-cost CPU that is capable of more than 400 Dhrystone MIPS. Through the RC64574/64575 processors IDT offers:

- **High-performance upgrade paths to existing embedded customers in the internetworking, office automation and visualization markets.**
- **Significant floating-point performance improvements over currently available, moderately priced MIPS CPUs.**
- **Performance improvements through the use of the MIPS-IV ISA.**
- **High-performance DSP acceleration**

1. Detailed system operation information is provided in the RC64574/RC64575 user's manual.

Instruction Issue Mechanism

The RC64574 and RC64575 are limited dual-issue super-scalar machines that use a traditional 5-stage integer pipeline, as shown in the pipeline diagram on Page 3. For multi-issue operations, these devices recognize the following two general classes of instructions:

- **Floating-point ALU**
- **All others**

Such a broad separation of instruction classes insure that there are no data dependencies to restrict multi-issue performance. As they are brought on-chip, these instruction classes are pre-decoded by the RC64574/575, and the class information is then stored in the instruction cache. Assuming there are no pending resource conflicts, the devices can issue one instruction per class per pipeline clock cycle.

However, longer latency resources—in either the floating-point ALU (for example, division or square root instructions) or integer unit (such as multiply)—can restrict the issue of instructions. Note that these processors do not perform out-of-order or speculative execution; instead, the pipeline slips until the required resource becomes available.

On dual-issue instruction pairs, there are no alignment restrictions, and the RC64574/575 fetch two instructions from the cache per cycle. Thus, for optimal performance, compilers should attempt to align branch targets to allow dual-issue on the first target cycle, because the instruction cache only performs aligned fetches.

RISCore4000/RISCore5000 Family of Socket Compatible Processors

	32-bit Processors			64-bit Processors		
	RC4640	**RC64474**	**RC64574**	**RC4650**	**RC64475**	**RC64575**
CPU	64-bit RISCore4000 w/ DSP extensions	64-bit RISCore4000	64-bit RISCore5000	64-bit RISCore4000 w/ DSP extensions	64-bit RISCore4000	64-bit RISCore5000
Performance	>350MIPS	>330MIPS	>440MIPS	>350MIPS	>330MIPS	>440MIPS
FPA	89 mflops, single precision only	125 mflops, single and double precision	666 mflops, single and double precision	89 mflops, single precision only	125 mflops, single and double precision	666 mflops, single and double precision
Caches	8kB/8kB, 2-way, lockable by set	16kB/16kB, 2-way, lockable by set	32kB/32kB, 2-way, lockable by set	8kB/8kB, 2-way, lockable by set	16kB/16kB, 2-way, lockable by set	32kB/32kB, 2-way, lockable by set
External Bus	32-bit	32-bit, Superset pin compatible w/RC4640	32-bit, Superset pin compatible w/RC4640, RC64474	32- or 64-bit	32-or 64-bit, Superset pin compatible w/ RC4650	32-or 64-bit, Superset pin compatible w/ RC4650, RC64475
Voltage	3.3V	3.3V	2.5V	3.3V	3.3V	2.5V
Frequencies	100-267 MHz	180-250 MHz	200-333 MHz	100-267 MHz	180-250 MHz	250-333 MHz
Packages	128 PQFP	128 QFP	128 QFP	208 QFP	208 QFP	208 QFP
MMU	Base-Bounds	96 page TLB	96 page TLB	Base-Bounds	96 page TLB	96 page TLB
Key Features	Cache locking, on-chip MAC, 32-bit external bus	Cache locking, JTAG, syncDRAM mode, 32-bit external bus	Cache locking, JTAG, syncDRAM mode, 32-bit external bus	Cache locking, on-chip MAC, 32-bit & 64 bit bus option	Cache locking, JTAG, syncDRAM mode, 32-64- bit bus option	Cache locking, JTAG, syncDRAM mode, 32-64- bit bus option

Table 1 RISCore4000/RISCore5000 Processor Family

Instruction Set Architecture

The RC64574/575 implement a superset of the MIPS-IV 64-bit ISA, including CP1 and CP1X functional units and their instruction set. Both 32- and 64-bit data operations are performed by utilizing thirty-two general purpose 64-bit registers (GPR) that are used for integer operations and address calculation. The complete on-chip floating-point coprocessor (CP1)—which includes a floating-point register file and execution units—forms a "seamless" interface, decoding and executing instructions in parallel with the integer unit.

CP1's floating-point execution units support both single and double precision arithmetic—as specified in the IEEE Standard 754—and are separated into a multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported, and the multiplier is partially pipelined, allowing the initiation of a new multiply instruction every fourth pipeline cycle. The **floating-point register file** is made up of thirty-two 64-bit registers. The floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store doubleword instruction in every cycle.

The **system control coprocessor (CP0) registers** are also incorporated on-chip and provide the path through which the virtual memory system's page mapping is examined and changed, exceptions are handled, and any operating mode selections are controlled. A secure user processing environment is provided through the **user, supervisor, and kernel operating modes** of virtual addressing to system software. Bits in a status register determine which of these modes is used.

Integer Pipeline

The integer instruction execution speed is tabulated—in number of pipeline clocks—as follows:

Operation	Latency	Repeat
Load	2	1
Store	2	1
MULT/MULTU	4	3
DMULT/DMULTU	6	5
DIV/DIVU	36	36
DDIV/DDIVU	68	68
MAD/MADU	3	2
MSUB/MSUBU	4	3
Other Integer ALU	1	1
Branch	2	2
Jump	2	2

Table 2 Integer Instruction Execution Speed

To insure that the maximum frequency of operation is not limited by the speed of the multiplier unit, a **"fast multiply"** disable reset mode bit (see Table 2) is featured. When this bit is asserted, each multiply operation shown in Table 1 has its latency and repeat rate increased by one cycle.

Load and branch latencies are minimized by the short pipeline of the RC64574/575, and the caches contain special logic that will allow any combination of loads and stores to execute in back-to-back cycles without requiring pipeline slips or stalls, assuming the operation does not miss in the cache.

Computational Units

The RC64574/575 implement a full, single-cycle 64-bit arithmetic logic unit (ALU), for **Integer ALU** functions other than multiply and divide. Bypassing is used to support back-to-back ALU operations at the full pipeline rate, without requiring stalls for data dependencies.

To allow the longer latency operations to run in parallel with other operations, the **Integer Multiply/Divide** unit of the RC64574/ 575 is separated from the primary ALU. The pipeline stalls only if an attempt to access the HI or LO registers is made before an operation completes.

The **Floating-point ALU** unit is responsible for all of the CP1/CP1X ALU operations—other than DIV/SQRT operations—and is pipelined to allow a single-cycle repeat rate for single-precision operations.

The **Floating-point DIV/SQRT** unit is separated from the floating-point ALU, to ensure that these longer latency operations do not prevent the issue of other floating-point operations. Separate logical units are also provided on the RC64574/575 to implement load, store, and branch operations.

Intended to enhance the performance of DSP algorithms such as fast fused multiply-adds, multiply-subtracts and three operand multiply operations**, new instructions** have been added over and above the MIPS-IV ISA.

System Interfaces

The **RC64575 supports a 64-bit system interface** that is pin and bus compatible with the RC4650 and RC64475 system interface. The system interface consists of a 64-bit Address/Data bus with eight parity-check bits and a 9-bit command bus.

During 64-bit operation, RC64575 system address/data (SysAD) transfers are protected with an 8-bit parity check bus, SysADC. When initialized for 32-bit operation, the RC64575's SysAD can be viewed as a 32-bit multiplexed bus that is protected by four parity-check bits.

The **RC64574 supports a 32-bit system interface** that is pin and bus compatible with the RC4640 and RC64474. During 32-bit operation, SysAD transfers are performed on a 32-bit multiplexed bus (SysAD 31:0) that is protected by 4 parity check bits (SysADC 6:0).

Writes to external memory—whether they are cache miss write-backs, stores to uncached or write-through addresses—use the on-chip **write buffer**. The write buffer holds a maximum of four 64-bit addresses and 64-bit data pairs. The entire buffer is used for a data cache write-back and allows the processor to proceed in parallel with memory updates.

Included in the system interface are **six handshake signals**: RdRdy*, WrRdy*, ExtRqst*, Release*, ValidOut*, and ValidIn*; **six interrupt inputs,** and a **simple timing** specification that is capable of trans-

ferring data between the processor and memory at a peak rate of 1000MB/sec. A boot-time selectable option to run the system interface as 32-bits wide—using basically the same protocols as the 64-bit system—is also supported.

A **boot-time mode control interface** initializes fundamental processor modes and is a serial interface that operates at a very low frequency (SysClock divided by 256). This low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively, the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL. The boot-time serial stream is shown in Table 3.

Serial Bit	Description	Value & Mode Setting
0	Reserved	Must be set to 0.
1:4	Transmit-data-pattern. Bit 4 is MSB	64-bit bus width: 0: DDDD 1: DDxDDx 2: DDxxDDxx 3: DxDxDxDx 4: DDxxxDDxxx 5: DDxxxxDDxxxx 6: DxxDxxDxxDxx 7: DDxxxxxxDDxxxxxx 8: DxxxDxxxDxxxDxxx 9-15: Reserved. Must not be selected. 32-bit bus width: 0: WWWWWWWW 1: WWxWWxWWxWWx 2: WWxxWWxxWWxxWWxx 3: WxWxWxWxWxWxWxWx 4: WWxxxWWxxxWWxxxWWxxx 5: WWxxxxWWxxxxWWxxxxWWxxxx 6: WxxWxxWxxWxxWxxWxxWxxWxx 7: WWxxxxxxWWxxxxxxWWxxxxxxWWxxxxxx 8: WxxxWxxxWxxxWxxxWxxxWxxxWxxxWxxx 9-15: Reserved. Must not be selected.
5:7	PClock-to-SysClk-Ratio. Bit 7 is MSB	0: 2 1: 3 2: 4 3: 5 4: 6 5: 7 6: 8 7: Reserved
8	Endianness	0: Little endian 1: Big endian
9:10	Non-block write Mode. Bit 10 is MSB	00: R4400 compatible 01: Reserved 10: Pipelined-Write-Mode 11: Write-Reissue-Mode

Table 3 Boot-time Mode Stream (Page 1 of 2)

Serial Bit	Description	Value & Mode Setting
11	TimerIntEn	Timer interrupt settings: 0: Enable Timer Interrupt on Int(5) 1: Disable Timer Interrupt on Int(5)
12	System Interface Bus Width.	Interface bus width control settings: 0: 64-bit system interface 1: 32-bit system interface
13:14	Drv_Out Bit 14 is MSB	Slew rate control of the output drivers: 10: 100% strength (fastest) 11: 83% strength 00: 67% strength 01: 50% strength (slowest)
15:17	Write address to write data delay.	From 0 to 7 SysClk cycles: 0: AD... 1: AxD... 2: AxxD... 3: AxxxD... 4: AxxxxD... 5: AxxxxxD... 6: AxxxxxxD... 7: AxxxxxxxD...
18	Reserved	User must select '0'
19	Extend Multiplication Repeat Rate.	Initial setting of the "Fast Multiply" bit. 0: Enable Fast Multiply 1: Do not Enable Fast Multiply **Note:** For pipeline speeds >250MHz, this bit must be set to '1'.
20:24	Reserved	User must select '0'
25:26	System configuration identifier.	Software visible in processorConfig[21:20] 0: Config[21:20] = Mode Bit [25:26]
27:256	Reserved	User must select '0'

Table 3 Boot-time Mode Stream (Page 2 of 2)

The **clocking interface** allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock and can be between 33 and 125MHz. An on-chip **phase-locked-loop (PLL)** generates the pipeline clock (PClock) through multiplication of the system interface clock by values of 2,3,4,5,6,7 or 8, as defined at system reset. This allows the pipeline clock to be implemented at a significantly higher frequency than the system interface clock. The RC64574/575 support both single data (one byte through full CPU bus width) and 8-word block transfers on the SysAD bus.

The RC64574/575 implement additional **write protocols** that **double the effective write bandwidth**. The write re-issue has a repeat rate of 2 cycles per write. Pipelined writes have the same 2-cycle per write repeat rate, but can issue an additional write after WrRdy* de-asserts.

Choosing a 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles as well as whether a single data transfer—larger than 4 bytes—must be divided into two smaller transfers.

As shown in Table 3, the bus delay can be defined as 0 to 7 SysClock cycles and is activated and controlled through mode bit (17:15) settings selected during the reset initialization sequence. The '000' setting provides the same write operations timing protocol as the RC4640, RC4650, and RC5000 processors.

To facilitate discrete **interface to SyncDRAM**, the RC64574/575 bus interface is enhanced during write cycles with a programmable delay that is inserted between the write address and the write data (for both block and non-block writes).

Board-level testing during Run-Time mode is facilitated through the full JTAG boundary scan facility. Five pins—TDI, TDO, TMS, TCK, TRST*—have been incorporated to support the standard JTAG interface.

The RC64574/575 devices offer a direct migration path for designs that are based on IDT's RC4640/RC4650 and RC64474/RC64475 processors[2], through full pin and socket compatibility. Full 64-bit-family software and bus protocol compatibility ensures the RC64574/575 processors access to an existing market and development infrastructure, allowing quicker time to market.

Development Tools

An array of hardware and software tools is available to assist system designers in the rapid development of RC64574/575 based systems. This accessibility allows a wide variety of customers to take full advantage of the device's high-performance features while addressing today's aggressive time-to-market demands.

Cache Memory

To keep the high-performance pipeline of the RC64574/575 full and operating efficiently, on-chip instruction and data caches have been incorporated. Each cache has its own data path and can be accessed in the same single pipeline clock cycle.

The 32kB two-way set associative **instruction cache** is virtually indexed, physically tagged, and word parity protected. Because this cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, further increasing performance by allowing both operations to occur simultaneously. The instruction cache provides a peak instruction bandwidth of 2667MB/sec at 333MHz.

The 32kB two-way set associative **data cache** is byte parity protected and has a fixed 32-byte (eight words) line size. Its tag is protected with a single parity bit. To allow simultaneous address translation and data cache access, the D-cache is virtually indexed and physically tagged. The data cache can provide 8 bytes each clock cycle, for a peak bandwidth of 2667MB/s.

To lock critical sections of code and/or data into the caches for quick access, a per line **"cache locking"** feature has been implemented. Once enabled, a cache is said to be locked when a particular piece of code or data is loaded into the cache and that cache location will not be selected later for refill by other data.

Power Management

Executing the WAIT instruction enables the processor to enter Standby mode. The internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*) will continue to run. Once in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Thermal Considerations

The RC64574 is packaged in a 128-pin QFP footprint package and uses a 32-bit external bus, offering the ideal combination of 64-bit processing power and 32-bit low-cost memory systems. The RC64575 is packaged in a 208-pin QFP footprint package and uses the full 64-bit external bus. The RC64575 is ideal for applications requiring 64-bit performance and 64-bit external bandwidth.

Both devices are guaranteed in a case temperature range of 0° to +85° C, for commercial temperature devices. Package type, speed (power) of the device, and air flow conditions affect the equivalent ambient temperature conditions that will meet these specifications.

Using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package, the equivalent allowable ambient temperature, T_A, can be calculated. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device. Typical values for $\varnothing_{CA}$ at various air flow are shown in Table 4. Note that the RC64574/575 processor implements advanced power management, which substantially reduces the typical power dissipation of the device.

	ØCA					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
128 QFP	16	10	9	7	6	5
208 QFP	20	13	10	9	8	7

Table 4 Thermal Resistance (ØCA) at Various Airflows

[2] To ensure socket compatibility, refer to Table 8 and Table 9.

Revision History

July 22, 1999: Original data sheet.

September 9, 1999: Made several changes in JTAG Interface section of Table 5. Added information on Pin 63 in Table 5.

October 14, 1999: Revised data in the Power Consumption tables for RC64574 and RC64575.

This space intentionally reserved for future revisions.

Pin Description Table

The following is a list of system interface pins available on the RC64574/575. Pin names ending with an asterisk (*) are active when low.

Pin Name	Type	Description
System Interface		
ExtRqst*	I	**External request** An external agent asserts ExtRqst* to request use of the System interface. The processor grants the request by asserting Release*.
Release*	O	**Release interface** In response to the assertion of ExtRqst* or a CPU read request, the processor asserts Release* and signals to the requesting device that the system interface is available.
RdRdy*	I	**Read Ready** The external agent asserts RdRdy* to indicate that it can accept a processor read request.
WrRdy*	I	**Write Ready** An external agent asserts WrRdy* when it can now accept a processor write request.
ValidIn*	I	**Valid Input** Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.

Table 5 Pin Descriptions (Page 1 of 3)

Pin Name	Type	Description
ValidOut*	O	**Valid Output** Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	I/O	**System address/data bus** A 64-bit address and data bus for communication between the processor and an external agent. In 64 bit interface mode, during address phases only, SysAd(35:0) contains invalid address information. The remaining SysAD(63:36) pins are not used. The whole 64-bit SysAD(63:0) may be used during the data transfer phase. For all double-word accesses (read or write), the low-order 3 bits (SysAD[2:0]) will always be output as zero during the address phase. In 32-bit interface mode and in the RC64574, SysAD(63:32) is not used, regardless of Endianness. A 32-bit address and data communication between processor and external agent is performed via SysAD(31:0).
SysADC(7:0)	I/O	**System address/data check bus** An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles. In 32-bit mode and in the RC64574, SysADC(7:4) is not used. The SysADC(3:0) contains check bits for SysAD(31:0).
SysCmd(8:0)	I/O	**System command/data identifier bus** A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	I/O	**System Command Parity** A single, even-parity bit for the Syscmd bus. This signal is always driven low.
Clock/Control Interface		
SysClock	I	**SystemClock** The system clock input establishes the processor and bus operating frequency. It is multiplied internally by 2,3,4,5,6,7, or 8 to generate the pipeline clock (PClock).
$V_{CC}P$	I	**Quiet VCC for PLL** Quiet Vcc for the internal phase locked loop.
$V_{SS}P$	I	**Quiet V_{SS} for PLL** Quiet Vss for the internal phase locked loop.
Interrupt Interface		
Int*(5:0)	I	**Interrupt** Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	I	**Non-maskable interrupt** Non-maskable interrupt, ORed with bit 6 of the interrupt register.
Initialization Interface		
$V_{CC}ok$	I	**V_{CC} is OK** When asserted, this signal indicates to the processor that the power supply has been above the Vcc minimum for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the initialization sequence.
ColdReset*	I	**Cold reset** This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with SysClock.
Reset*	I	**Reset** This signal must be asserted for any reset sequence. It can be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with SysClock.
ModeClock	O	**Boot-mode clock** Serial boot-mode data clock output at the system clock frequency divided by two hundred fifty-six.

Table 5 Pin Descriptions (Page 2 of 3)

Pin Name	Type	Description
ModeIn	I	**Boot-mode data in** Serial boot-mode data input.

JTAG Interface

TDI	I	**JTAG Data In** On the rising edge of TCK, serial input data are shifted into either the Instruction register or Data register, depending on the TAP controller state. An external pull-up resistor is required.
TDO	O	**JTAG Data Out** On the falling edge of TCK, the TDO is serial data shifted out from either the instruction or data register. When no data is shifted out, the TDO is tri-stated (high impedance).
TCK	I	**JTAG Clock Input** An input test clock used to shift into or out of the boundary-scan register cells. TCK is independent of the system and processor clock with nominal 40-60% duty cycle.
TMS	I	**JTAG Command Select** The logic signal received at the TMS input is decoded by the TAP controller to control test operation. TMS is sampled on the rising edge of TCK. An external pull-up resistor is required.
TRST*	I	**JTAG Reset** The TRST* pin is an active-low signal used for asynchronous reset of the debug unit, independent of the processor logic. During normal CPU operation, the JTAG controller will be held in the reset mode, asserting this active low pin. When asserted low, this pin will also tristate the TDO pin. An external pull-down resistor is required.
JTAG32*	I	**JTAG 32-bit scan** This pin is used to control length of the scan chain for SysAD (32-bit or 64-bit) for the JTAG mode. When set to Vss, 32-bit bus mode is selected. In this mode, only SysAD(31:0) are part of the scan chain. When set to Vcc, 64-bit bus mode is selected. In this mode, SysAD(63:0) are part of the scan chain. This pin has a built-in pull-down device to guarantee 32-bit scan, if it is left un connected.
JR_V_{cc}	I	**JTAG VCC** This pin has an internal pull-down to continuously reset the JTAG controller (if left unconnected) bypassing the TRst* pin. When supplied with Vcc, the TRst* pin will be the primary control for the JTAG reset.

Table 5 Pin Descriptions (Page 3 of 3)

Logic Diagram — RC64574/RC64575

Figure 1 illustrates the direction and functional groupings for the processor signals.

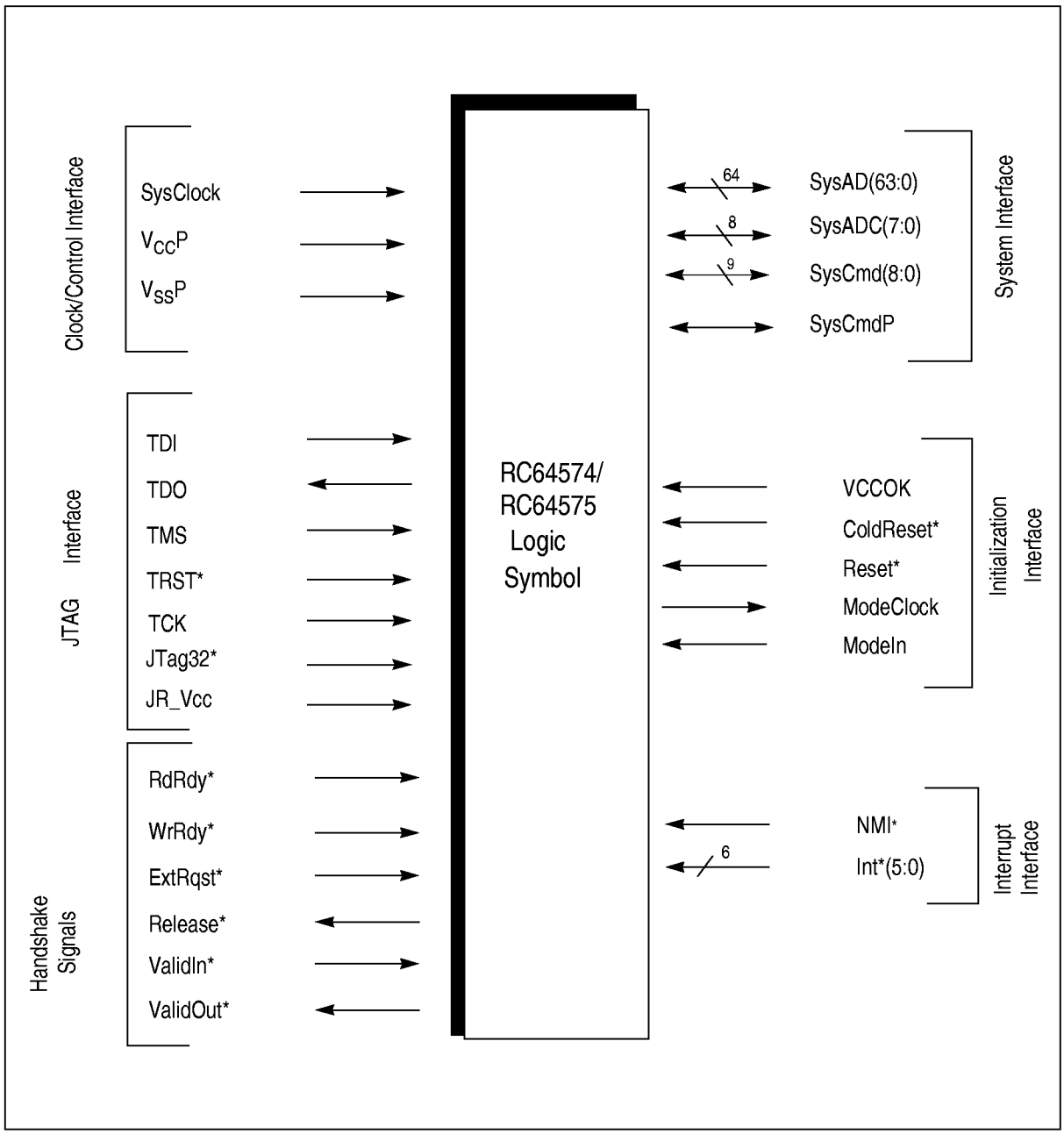


Figure 1 Logic Symbol for RC64574/RC64575

RC64575 208-pin QFP Package Pin-out

Pin names followed by an asterisk (*) are active when low. For maximum flexibility and compatibility with future designs, N.C. pins should be left floating.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	JTAG32*	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	N.C.	55	N.C.	107	N.C.	159	SysAD59
4	N.C.	56	N.C.	108	N.C.	160	ColdReset*
5	N.C.	57	SysCmd2	109	N.C.	161	SysAD28
6	N.C.	58	SysAD36	110	N.C.	162	V_{cc}
7	N.C.	59	SysAD4	111	N.C.	163	V_{ss}
8	N.C.	60	SysCmd1	112	N.C.	164	SysAD60
9	N.C.	61	V_{ss}	113	N.C.	165	Reset*
10	SysAD11	62	V_{cc}	114	SysAD52	166	SysAD29
11	V_{ss}	63	SysAD35	115	ExtRqst*	167	SysAD61
12	V_{cc}	64	SysAD3	116	V_{cc}	168	SysAD30
13	SysCmd8	65	SysCmd0	117	V_{ss}	169	V_{cc}
14	SysAD42	66	SysAD34	118	SysAD21	170	V_{ss}
15	SysAD10	67	V_{ss}	119	SysAD53	171	SysAD62
16	SysCmd7	68	V_{cc}	120	RdRdy*	172	SysAD31
17	V_{ss}	69	SysAD2	121	Modein	173	SysAD63
18	V_{cc}	70	Int5*	122	SysAD22	174	V_{cc}
19	SysAD41	71	SysAD33	123	SysAD54	175	V_{ss}
20	SysAD9	72	SysAD1	124	V_{cc}	176	V_{cc}OK
21	SysCmd6	73	V_{ss}	125	V_{ss}	177	SysADC3
22	SysAD40	74	V_{cc}	126	Release*	178	SysADC7
23	V_{ss}	75	Int4*	127	SysAD23	179	N.C.
24	V_{cc}	76	SysAD32	128	SysAD55	180	TDI
25	SysAD8	77	SysAD0	129	NMI*	181	TRst*
26	SysCmd5	78	Int3*	130	V_{cc}	182	TCK
27	SysADC4	79	V_{ss}	131	V_{ss}	183	TMS
28	SysADC0	80	V_{cc}	132	SysADC2	184	TDO
29	V_{ss}	81	Int2*	133	SysADC6	185	V_{cc}P
30	V_{cc}	82	SysAD16	134	SysAD24	186	V_{ss}P
31	SysCmd4	83	SysAD48	135	V_{cc}	187	SysClock
32	SysAD39	84	Int1*	136	V_{ss}	188	V_{cc}

Table 6 RC64575 208-pin QFP Package Pin-Out (Page 1 of 2)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
33	SysAD7	85	V_{ss}	137	SysAD56	189	V_{ss}
34	SysCmd3	86	V_{cc}	138	SysAD25	190	SysADC5
35	V_{ss}	87	SysAD17	139	SysAD57	191	SysADC1
36	V_{cc}	88	SysAD49	140	V_{cc}	192	V_{cc}
37	SysAD38	89	Int0*	141	V_{ss}	193	V_{ss}
38	SysAD6	90	SysAD18	142	N.C	194	SysAD47
39	ModeClock	91	V_{ss}	143	SysAD26	195	SysAD15
40	WrRdy*	92	V_{cc}	144	SysAD58	196	SysAD46
41	SysAD37	93	SysAD50	145	N.C.	197	V_{cc}
42	SysAD5	94	ValidIn*	146	V_{cc}	198	V_{ss}
43	V_{ss}	95	SysAD19	147	V_{ss}	199	SysAD14
44	V_{cc}	96	SysAD51	148	SysAD27	200	SysAD45
45	N.C.	97	V_{ss}	149	N.C.	201	SysAD13
46	N.C.	98	V_{cc}	150	JR_V_{cc}	202	SysAD44
47	N.C.	99	ValidOut*	151	N.C.	203	V_{ss}
48	N.C.	100	SysAD20	152	N.C.	204	V_{cc}
49	N.C.	101	N.C.	153	N.C.	205	SysAD12
50	N.C.	102	N.C.	154	N.C.	206	SysCmdP
51	N.C.	103	N.C.	155	N.C.	207	SysAD43
52	N.C.	104	N.C.	156	N.C.	208	N.C.

Table 6 RC64575 208-pin QFP Package Pin-Out (Page 2 of 2)

RC64574 128-pin Package Pin-out

N.C. pins should be left floating for maximum flexibility as well as for compatibility with future designs. An asterisk (*) identifies a pin that is active when low.

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	JTAG32*	33	V_{cc}	65	V_{cc}	97	V_{cc}
2	SysCmd2	34	V_{ss}	66	SysAD28	98	V_{ss}
3	V_{cc}	35	SysAD13	67	ColdReset*	99	SysAD19
4	V_{ss}	36	SysAD14	68	SysAD27	100	ValidIn*
5	SysAD5	37	V_{ss}	69	V_{ss}	101	V_{cc}
6	WrRdy*	38	V_{cc}	70	V_{cc}	102	V_{ss}
7	ModeClock	39	SysAD15	71	JR_V_{cc}	103	SysAD18
8	SysAD6	40	V_{ss}	72	SysAD26	104	Int0*
9	V_{cc}	41	V_{cc}	73	N.C.	105	SysAD17
10	V_{ss}	42	SysADC1	74	V_{ss}	106	V_{cc}
11	SysCmd3	43	V_{ss}	75	V_{cc}	107	V_{ss}
12	SysAD7	44	V_{cc}	76	SysAD25	108	Int1*
13	SysCmd4	45	SysClock	77	V_{ss}	109	SysAD16
14	V_{cc}	46	V_{ss}P	78	V_{cc}	110	Int2*
15	V_{ss}	47	V_{cc}P	79	SysAD24	111	V_{cc}
16	SysADC0	48	TDO	80	SysADC2	112	V_{ss}
17	SysCmd5	49	TMS	81	V_{ss}	113	Int3*
18	SysAD8	50	TCK	82	V_{cc}	114	SysAD0
19	V_{cc}	51	TRst*	83	NMI*	115	Int4*
20	V_{ss}	52	TDI	84	SysAD23	116	V_{cc}
21	SysCmd6	53	V_{ss}	85	Release*	117	V_{ss}
22	SysAD9	54	SysADC3	86	V_{ss}	118	SysAD1
23	V_{cc}	55	V_{cc}OK	87	V_{cc}	119	Int5*
24	V_{ss}	56	V_{ss}	88	SysAD22	120	SysAD2
25	SysCmd7	57	Vcc	89	Modein	121	V_{cc}
26	SysAD10	58	SysAD31	90	RdRdy*	122	V_{ss}
27	SysCmd8	59	V_{ss}	91	SysAD21	123	SysCmd0
28	V_{cc}	60	V_{cc}	92	V_{ss}	124	SysAD3
29	V_{ss}	61	SysAD30	93	V_{cc}	125	V_{cc}
30	SysAD11	62	SysAD29	94	ExtRqst*	126	V_{ss}
31	SysCmdP	63	Reset*	95	SysAD20	127	SysCmd1
32	SysAD12	64	V_{ss}	96	ValidOut*	128	SysAD4

Table 7 RC64574 128-Pin Package

RC64574 Socket Compatibility to RC64474 & RC4640

The RC64574/575 is 100% pin compatible with the RC64474/475 with the supply voltage being the only difference. RC64474/475 requires a 3.3V supply, while RC64574/575 requires a 2.5V supply.

To ensure socket compatibility between the RC64574/RC64474 and the RC4640 devices, several pin changes are required, as shown in the tables below. **Note:** The RC64574/575 are 2.5V parts and as such all Vcc must be at the correct voltage for a given part.

Pin	RC4640	RC64574/ RC64474	Compatible to RV4640?	Comments
1	N.C	JTAG32*	Yes.	Pin has an internal pull-down, to enable 32-bit scan. Can also be left a N.C.
48	V_{ss}	TDO	Yes.	Can be driven with V_{ss}, if JTAG is not needed. Is tristated when TRst* is low.
49	V_{ss}	TMS	Yes.	Can be driven with V_{ss} if JTAG is not needed.
50	V_{ss}	TCK	Yes.	Can be driven with V_{ss} if JTAG is not needed.
51	V_{ss}	TRst*	Yes.	Can be driven with V_{ss} if JTAG is not needed.
52	V_{ss}	TDI	Yes.	Can be driven with V_{ss} if JTAG is not needed.
71	N.C.	JR_V_{cc}	Yes.	Can be left N.C. in RC64574, if JTAG is not need. If JTAG is needed, it must be driven to V_{cc}.

Table 8 RC64574 Socket Compatibility to RC64474 and R4640

RC64575 Socket Compatibility to RC64475 & RC4650

Pin	RV4650 32-bit	RC64575 32-bit RC64475 32-bit	RV4650 64-bit	RC64575 64-bit RC64475 64-bit	Compatible to RV4650?	Comments
53	N.C.	JTAG32*	No Connect	JTAG32*	Yes	In 32-bit, this pin can be left unconnected because of internal pull-down. In 64-bit, this assumes that JTAG will not be used. If using JTAG, this pin must be at V_{cc}.
150	N.C.	JR_V_{cc}	No Connect	JR_V_{cc}	Yes	In RC64475, can be left a N.C, if JTAG is not need. If JTAG is needed, it must be driven to V_{cc}.
180	N.C.	TDI	No Connect	TDO	Yes	If JTAG is not needed, can be left a N.C.
181	N.C.	TRsT*	No Connect	TRsT*	Yes	If JTAG is not needed, can be left a N.C.
182	N.C.	TCK	No Connect	TCK	Yes	If JTAG is not needed, can be left a N.C.
183	N.C.	TMS	No Connect	TMS	Yes	If JTAG is not needed, can be left a N.C.
184	N.C.	TDO	No Connect	TDIO	Yes	If JTAG is not needed, can be left a N.C.

Table 9 RC64575 Socket Compatibility to RC64475 & RC4650

Absolute Maximum Ratings

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Symbol	Rating	Commercial (2.5V±5%)	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5[1] to +4.0	V
T_C	Operating Temperature (case)	0 to +85	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{IN}	DC Input Current	20[2]	mA
I_{OUT}	DC Output Current	50[3]	mA

1. V_{In} minimum = –2.0V for pulse width less than 15ns. V_{IN} should not exceed VCC +0.5 Volts.

2. When V_{IN} < 0V or V_{IN} > V_{CC}.

3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

Recommended Operation Temperature and Supply Voltage

Grade	Temperature	GND	RC64574/ 575
			Vcc
Commercial	0°C to +85°C (Case)	0V	2.5V±5%

DC Electrical Characteristics

Commercial Temperature Range—RC64574/575

(V_{cc} = 2.5V± 5%; T_{case} = 0°C to +85°C)

Parameter	RC64574 200MHz		RC64574/RC64575 250MHz		RC64574/RC64575 300MHz[1]		RC64574/RC64575 333MHz[1]		Conditions
	Min	Max	Min	Max	Min	Max	Min	Max	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	—	0.1V	IIOUTI= 20uA
V_{OH}	V_{cc} - 0.1V	—	V_{cc} - 0.1V	—	V_{cc} - 0.1V	—	V_{cc} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	—	0.4V	IIOUTI= 4mA
V_{OH}	2.0V	—	2.0V	—	2.0V	—	2.0V	—	
V_{IL}	–0.5V	$0.2V_{cc}$	–0.5V	$0.2V_{cc}$	–0.5V	$0.2V_{cc}$	–0.5V	$0.2V_{cc}$	—
V_{IH}	0.7 V_{cc}	3.3V	0.7 V_{cc}	3.3V	0.7 V_{cc}	3.3V	0.7 V_{cc}	3.3V	—
I_{IN}	—	±10uA	—	±10uA	—	±10uA	—	±10uA	0 ≤ VIN ≤ VCC
C_{IN}	—	10pF	—	10pF	—	10pF	—	10pF	—
C_{IO}	—	10pF	—	10pF	—	10pF	—	10pF	—
C_{clk}	—	10pF	—	10pF	—	10pF	—	10pF	
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	—	20uA	Input/Output Leakage

1. At pipeline speeds >250MHz, the "Fast Multiply" bit must be disabled.

Power Consumption—RC64574

Parameter		RC64574 200MHz		RC64574 250MHz		RC64574 300MHz		RC64574 333MHz		Conditions
		Typical[1]	Max	Typical[1]	Max	Typical[1]	Max	Typical[1]	Max	
I_{CC}	stand-by	—	60 mA[2]	—	60 mA[2]	—	100 mA[2]	—	100 mA[2]	C_L = 0pF[3]
		—	120 mA[2]	—	120 mA[2]	—	120 mA[2]	—	120 mA[2]	C_L = 50pF
	active	500 mA[2]	600 mA[2]	550mA[2]	700 mA[2]	700 mA[2]	800mA[2]	750 mA[2]	900mA[2]	C_L = 0pF No SysAd activity[3] Vcc = 2.63V
		550mA[2]	650 mA[2]	650 mA[2]	800 mA[2]	800mA[2]	1000mA[2]	850mA[2]	1100mA[2]	C_L = 50pF R4x00 compatible writes, T_C = 25°C Vcc = 2.63V
		680 mA[2]	850 mA[4]	800 mA[2]	1000 mA[4]	950mA[2]	1200mA[2]	1000mA[2]	1300mA[2]	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[3] Vcc = 2.63V

1. Typical integer instruction mix and cache miss rates

2. These are not tested. They are the results of engineering analysis and are provided for reference only

3. Guaranteed by design.

4. These are the specifications IDT tests to insure compliance.

Power Consumption—RC64575

Parameter		RC64575 250MHz		RC64575 300MHz		RC64575 333MHz		Conditions
		Typical[1]	Max	Typical[1]	Max	Typical[1]	Max	
I_{CC}	stand-by	—	60 mA[2]	—	60 mA[2]	—	100 mA[2]	C_L = 0pF[3]
		—	120 m^2A	—	120 mA[2]	—	120 mA[2]	C_L = 50pF
	active, 64-bit bus option[4]	550 mA[2]	700 mA[2]	700 mA[2]	800 mA[2]	800 mA[2]	1000 mA[2]	C_L = 0pF No SysAd activity[3] Vcc = 2.63V
		800 mA[2]	1000 mA[2]	850 mA[2]	1100 mA[2]	900mA[2]	1200mA[2]	C_L = 50pF R4x00 compatible writes, T_C = 25°C Vcc = 2.63V
		850 mA[2]	1200 mA[5]	950 mA[2]	1300 mA[5]	1200 mA[2]	1500 mA[2]	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[3] Vcc = 2.63V

1. Typical integer instruction mix and cache miss rates

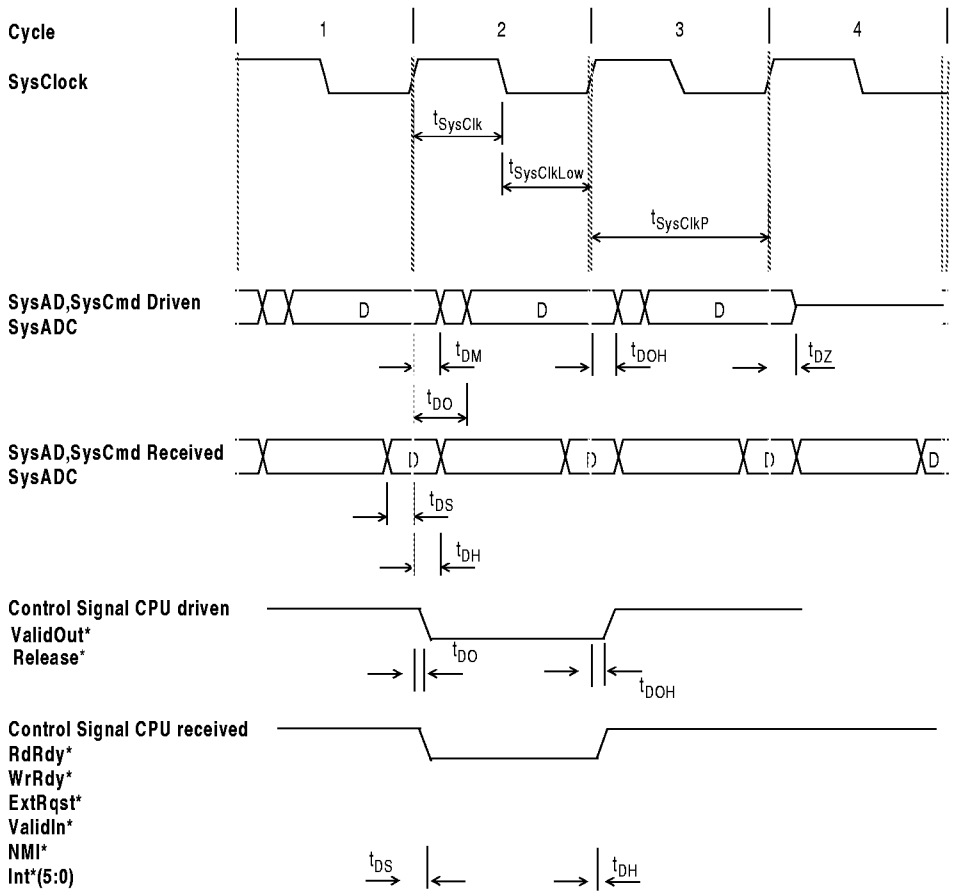
2. These are not tested. They are the results of engineering analysis and are provided for reference only.

3. Guaranteed by design.

4. In 32-bit bus option, use RC64474 power consumption values.

5. These are the specifications IDT tests to insure compliance.

Timing Characteristics—RC64574/RC64575



* = active low signal

Figure 2 System Clocks Data Setup, Output, and Hold timing

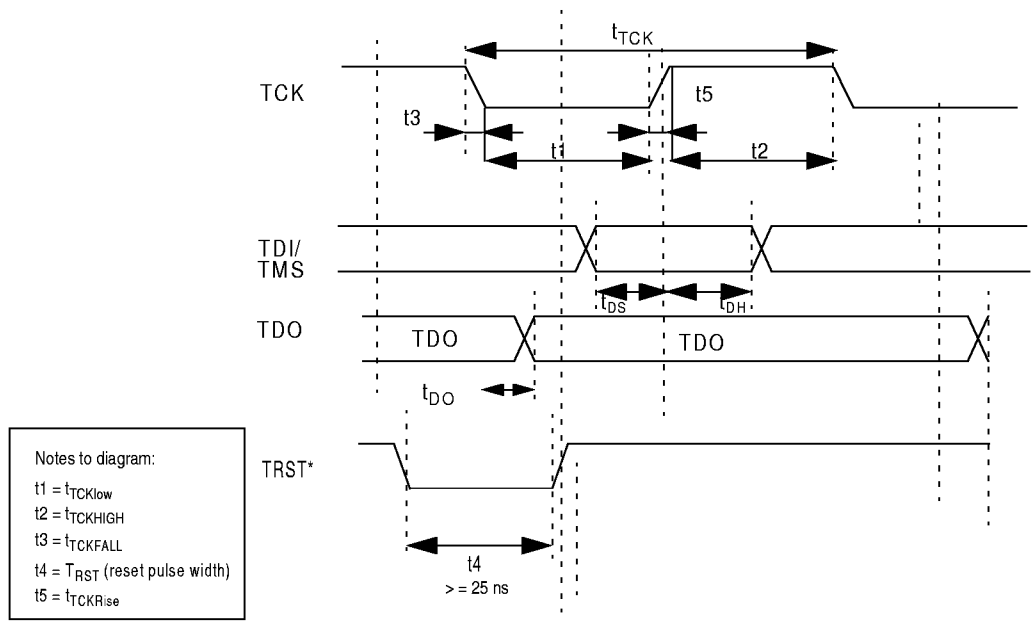


Figure 3 Standard JTAG Timing

System Interface Parameters

Parameter	Symbol	Test Conditions	RC64574 200MHz		RC64574/ RC64575 250MHz		RC64574/ RC64575 300MHz		RC64574/ RC64575 333MHz		Units
			Min	Max	Min	Max	Min	Max	Max	Max	
Data Output	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0[1]	5	1.0[1]	4.7	1.0	4.7	1.0	4.7	ns
		$mode_{14..13}$ = 01 (slowest)	1.0[2]	8	1.0[2]	7	1.0	7	1.0	7	ns
Data Output Hold	t_{DOH}[2]	$mode_{14..13}$ = 10 (fastest)	1.0	—	1.0	—	1.0	—	1.0	—	ns
Data Input	t_{DS}	t_{rise} = 3ns t_{fall} = 3ns	2	—	2	—	2	—	2	—	ns
	t_{DH}		1.0	—	1.0	—	1.0	—	1.0	—	ns

1. Guaranteed by design

2. 50 pf loading on external output signals

Boot-time Interface Parameters

Parameter	Symbol	Test Conditions	RC64574 200MHz		RC64574/ RC64575 250MHz		RC64574/ RC64575 300MHz		RC64574/ RC64575 333MHz		Conditions
			Min	Max	Min	Max	Min	Max	Max	Max	
Mode Data Setup	t_{DS}	—	4	—	4	—	4	—	4	—	SysClock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	0	—	SysClock Cycle

Mode Configuration Interface Reset Sequence

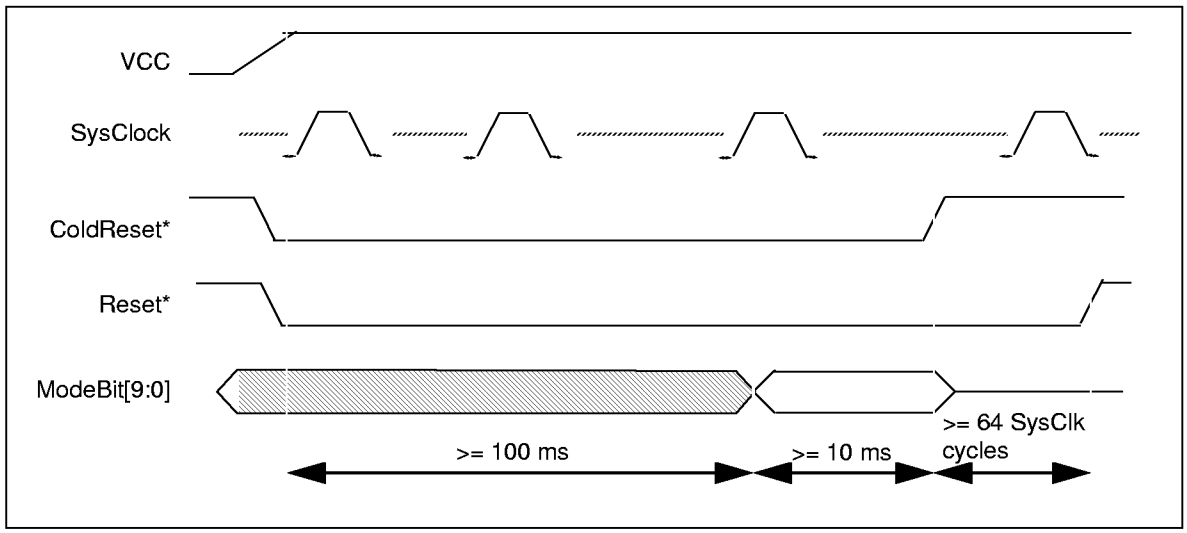


Figure 4 Mode Configuration Interface Reset Sequence

AC Electrical Characteristics

(V_{cc} = 2.5V ± 5%; T_{case} = 0°C to +85°C)

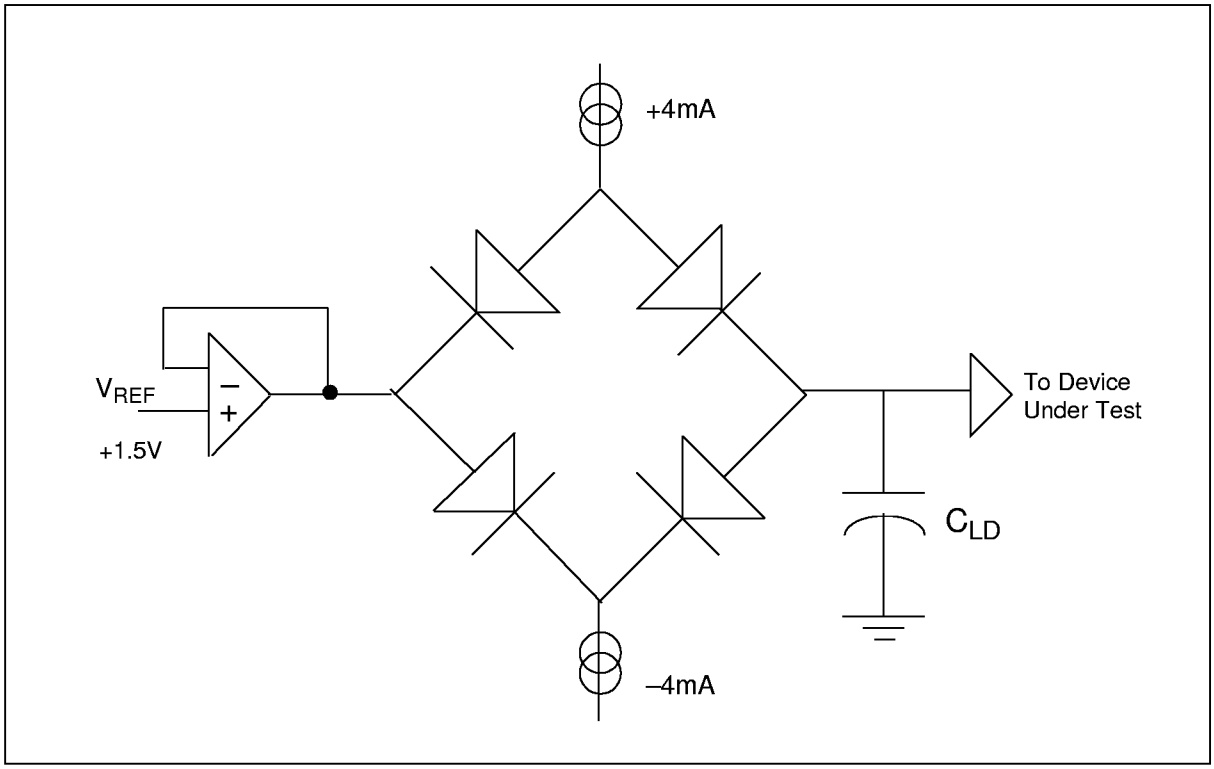
Clock Parameters—RC64574/575

Parameter	Symbol	Test Conditions	RC64574 200MHz		RC64574/ RC64575 250MHz		RC64574/ RC64575 300MHz		RC64574/ RC64575 333MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline Clock Frequency	PCLk	—	100	200	100	250	100	300	100	333	MHz
System Clock HIGH	t_{SCHIGH}	Transition ≤ 3ns	3	—	3	—	3	—	3	—	ns
System Clock LOW	t_{SCLOW}	Transition ≤ 3ns	3	—	3	—	3	—	3	—	ns
System Clock Frequency	_	—	33	100	33	125	33	125	33	125	MHz
System Clock Period	t_{SCP}	—	10	30	8	30	8	30	8	30	ns
System Clock Rise Time	t_{SCRise}	—	—	2	—	2	—	2	—	2	ns
System Clock Fall Time	t_{SCFall}	—	—	2	—	2	—	2	—	2	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256 t_{SCP}	—	256 t_{SCP}	—	256 t_{SCP}	—	256 t_{SCP}	ns
JTAG Clock Input Period	t_{TCK}	—	—	100	—	100	—	100	—	100	ns
JTAG Clock HIGH	$t_{TCKHIGH}$	—	—	40	—	40	—	40	—	40	ns
JTAG Clock Low	t_{TCKLOW}	—	—	40	—	40	—	40	—	40	ns
JTAG Clock Rise Time	$t_{TCKRise}$	—	—	5	—	5	—	5	—	5	ns
JTAG Clock Fall Time	$t_{TCKFall}$	—	—	5	—	5	—	5	—	5	ns

Capacitive Load Deration—RC64574/575

Parameter	Symbol	Test Conditions	200MHz		250MHz		300MHz		333MHz		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Load Derate	C_{LD}	—	—	2	—	2	—	2	—	2	ns/25pF

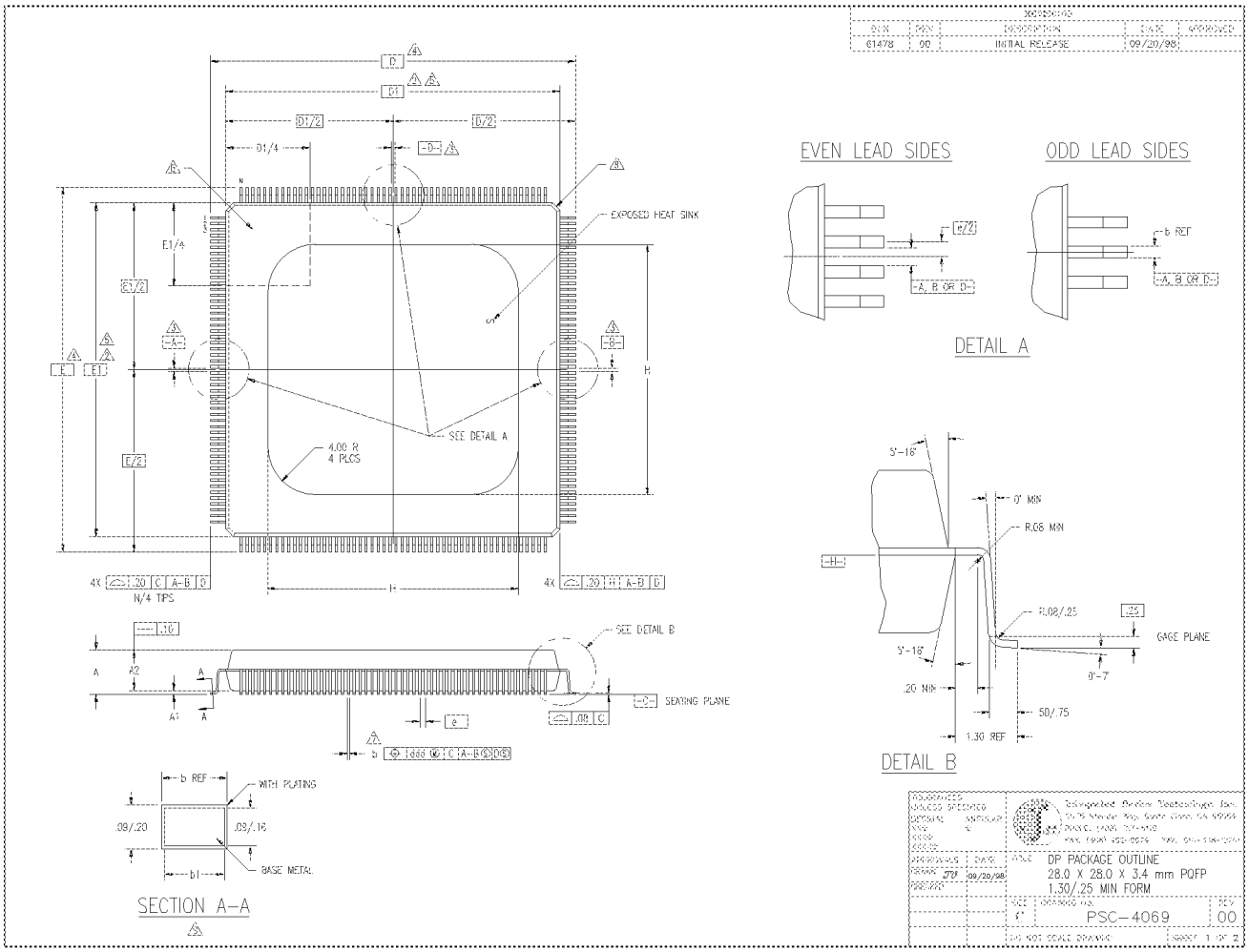
Output Loading for AC Testing



Signal	Cld
All Signals	50 pF

RC64575 208-pin Package Diagram

The RC64575 is available in a 208-pin QFP package.

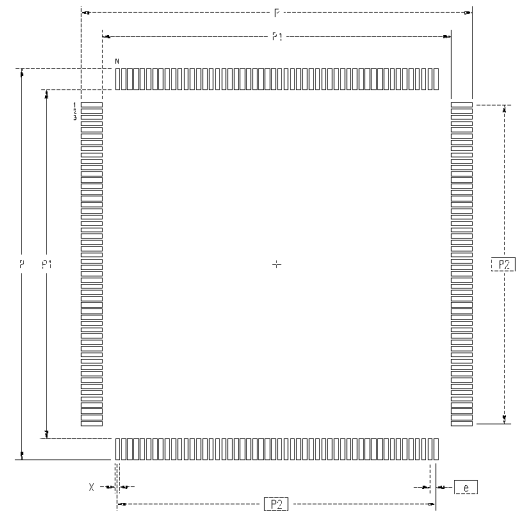


RC64575 208-pin Package Diagram (page2)

DCN	REV	DESCRIPTION	DATE	APPROVED
61478	00	INITIAL RELEASE	09/20/98	

SYMBOL	JEDEC VARIATION FA-1 MIN	NOM	MAX	NOTE
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D		30.60 BSC		4
D1		28.00 BSC		5,2
E		30.60 BSC		4
E1		28.00 BSC		5,2
H		21.00 REF		
N		208		
e		.50 BSC		
b	.17	–	.27	7
b1	.17	.20	.23	
ddd	–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS A–B AND –D– TO BE DETERMINED AT DATUM PLANE –H–
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE –C–
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–143, VARIATION FA–1

UNLESS SPECIFIED TOLERANCES: DECIMAL ANGULAR

Integrated Device Technology, Inc.

APPROVED | DATE: 09/20/98

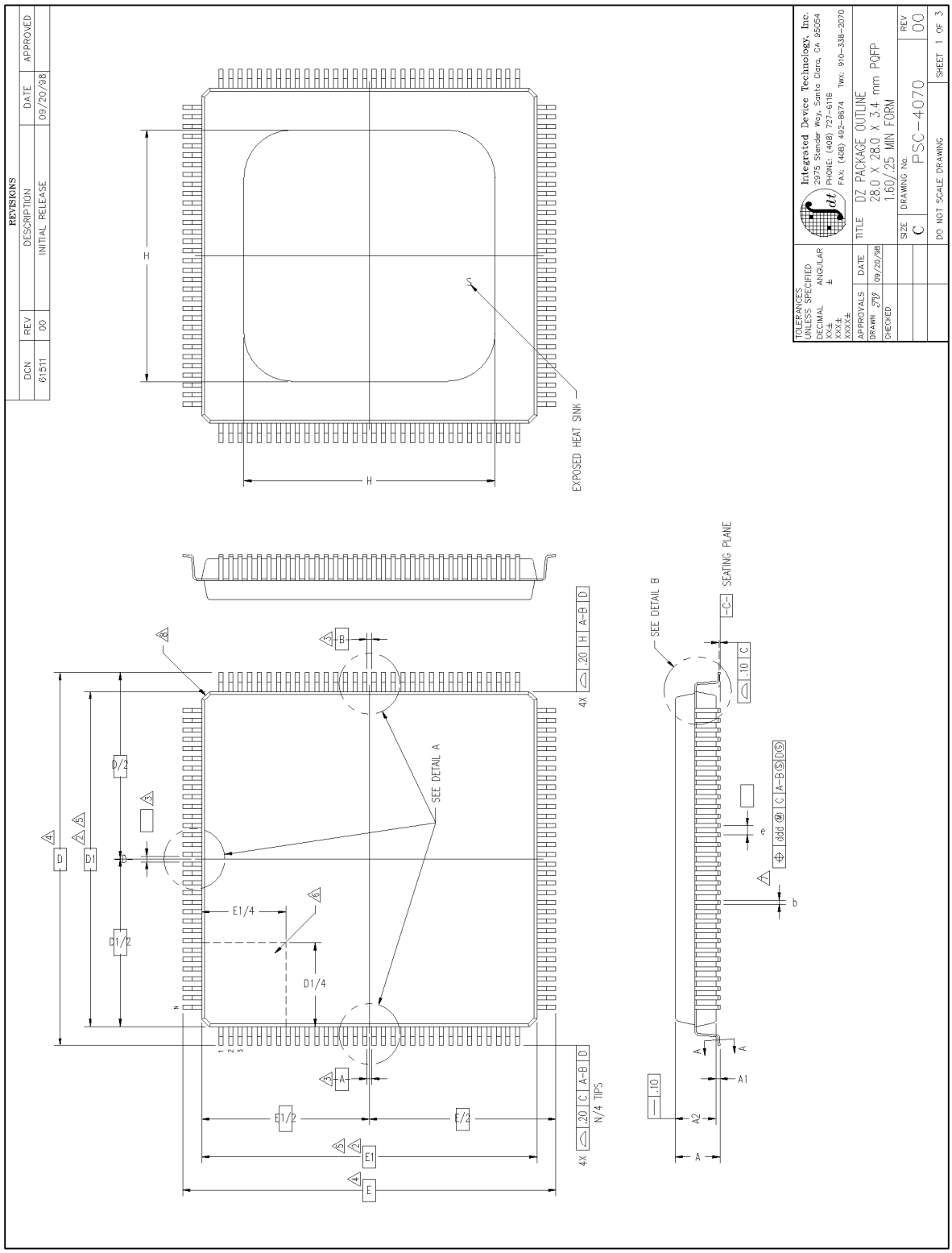
TITLE: DP PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.30/.25 MIN FORM

SIZE: C | DRAWING NO.: PSC–4069 | REV: 00

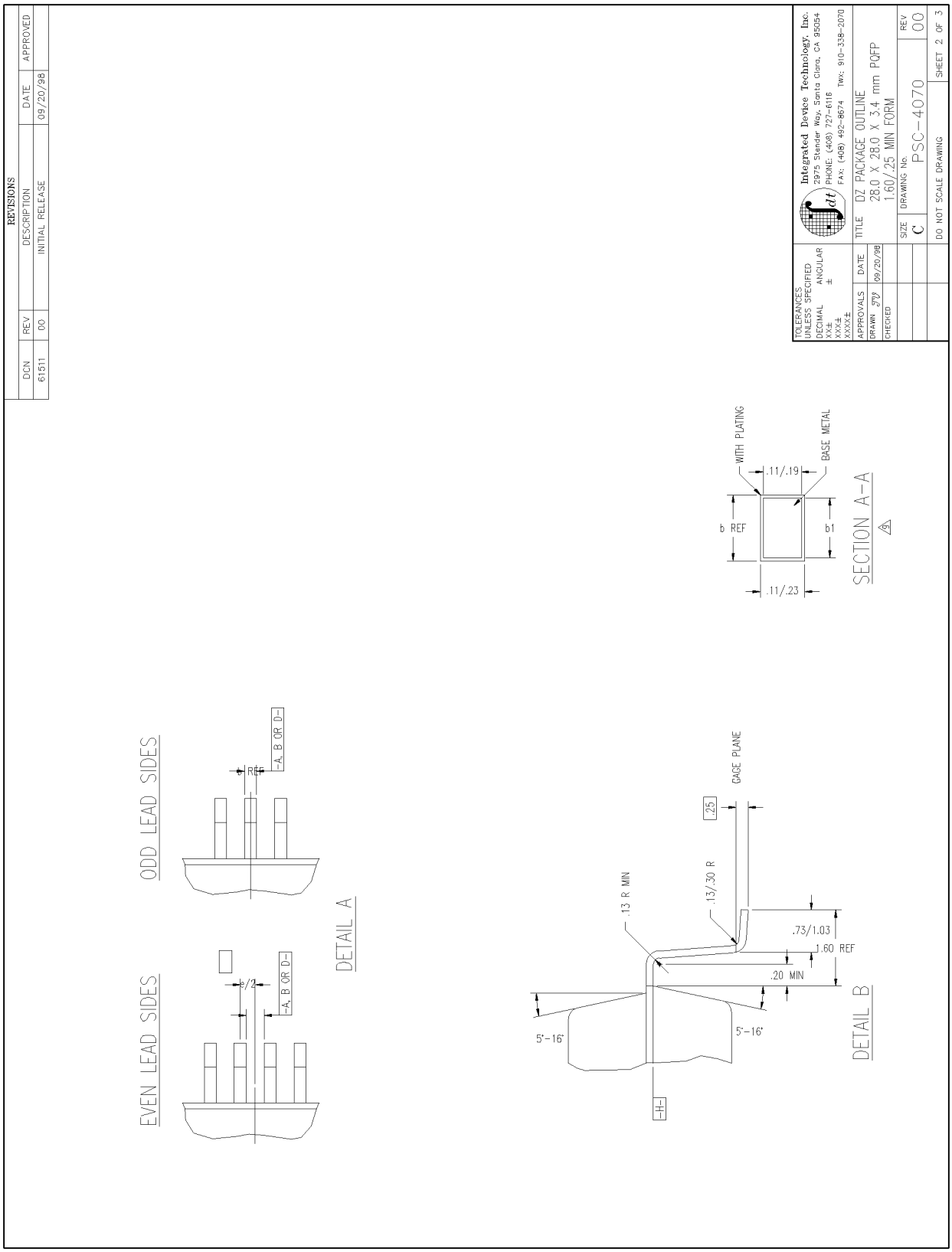
DO NOT SCALE DRAWING | SHEET 2 OF 2

RC64574 128-pin Package Diagram (page 1 of 3)

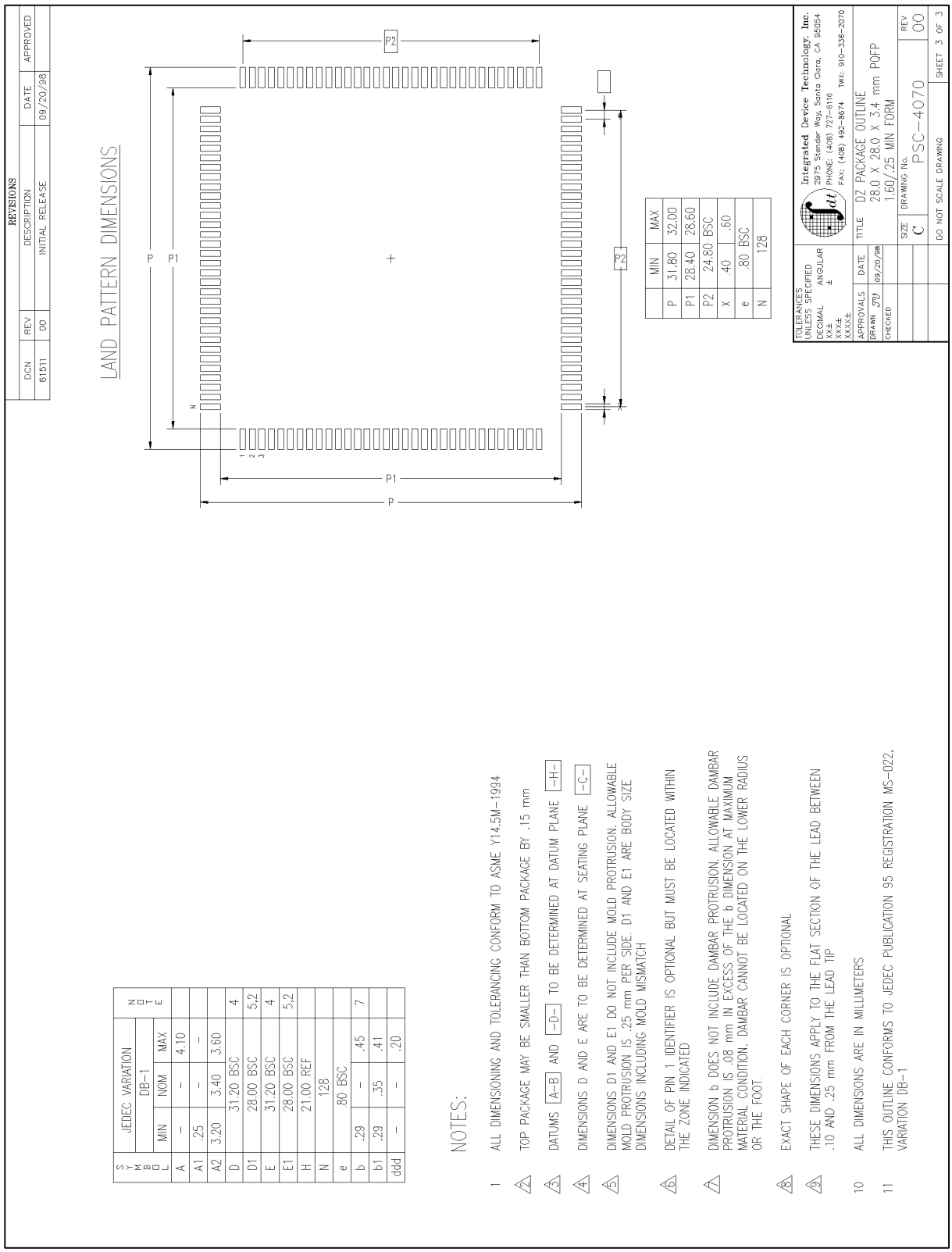
The RC64574 is available in a 128-pin QFP package.



RC64574 128-pin Package Diagram (page 2 of 3)



RC64574 128-pin Diagram (Page 3 of 3)



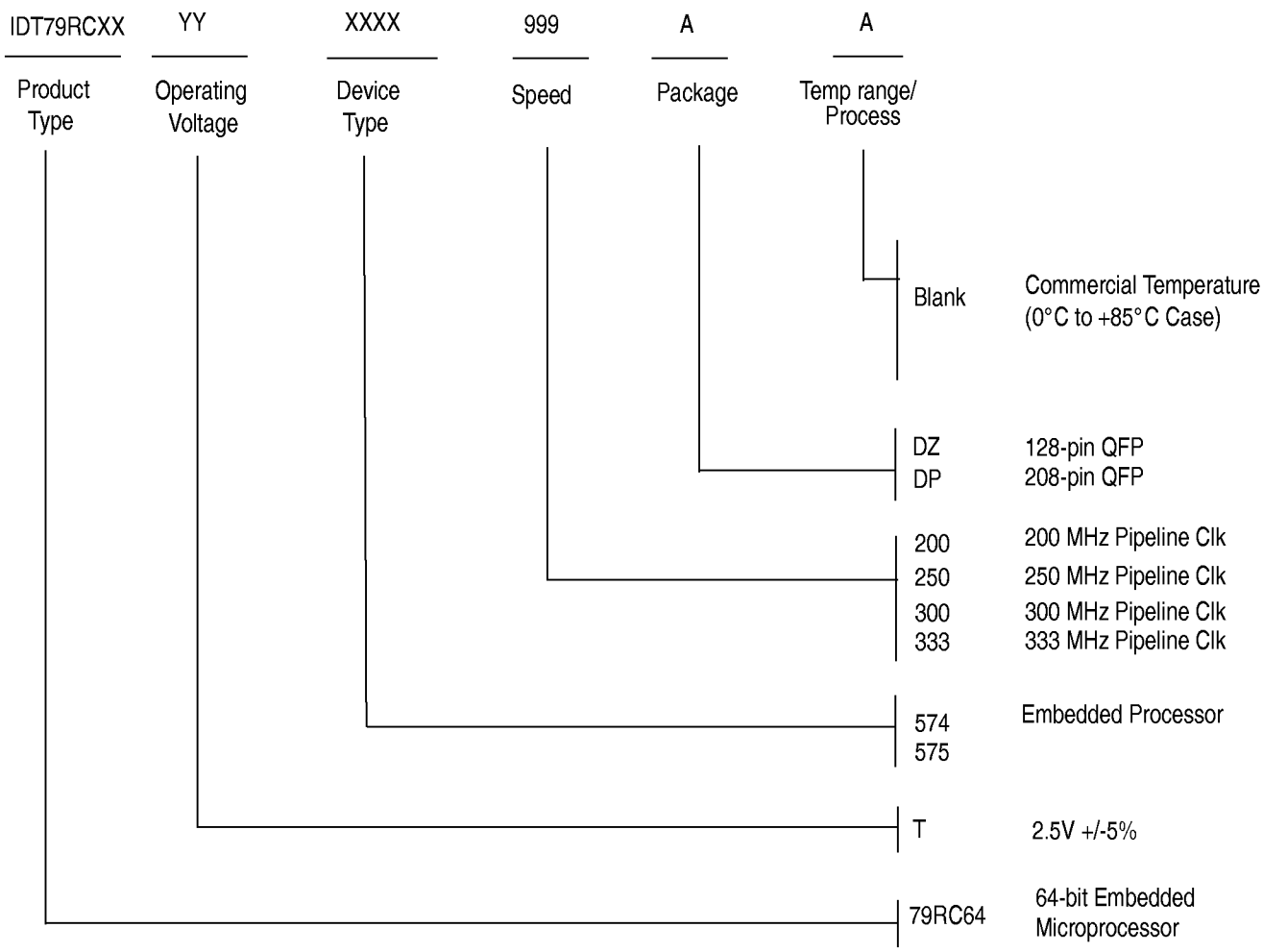
	MIN	MAX
P	31.80	32.00
P1	28.40	28.60
P2	24.80 BSC	
X	.40	.60
e	.80 BSC	
N	128	

SYMBOL	JEDEC VARIATION DB-1 MIN	NOM	MAX	NOTE
A	–	–	4.10	
A1	.25	–	–	
A2	3.20	3.40	3.60	
D		31.20 BSC		4
D1		28.00 BSC		5,2
E		31.20 BSC		4
E1		28.00 BSC		5,2
H		21.00 REF		
N		128		
e		.80 BSC		
b	.29	–	.45	7
b1	.29	.35	.41	
ddd	–	–	.20	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-022, VARIATION DB-1

Ordering Information



Valid Combinations

IDT79RC64T574 - 200, 250, 300, 333 DZ	128-pin QFP package, Commercial Temperature
IDT79RC64T575 - 250, 300, 333 DP	208-pin QFP package, Commercial Temperature

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