



**RISController™ Embedded**  
**64-bit Microprocessor, based on**  
**RISCore4000™**

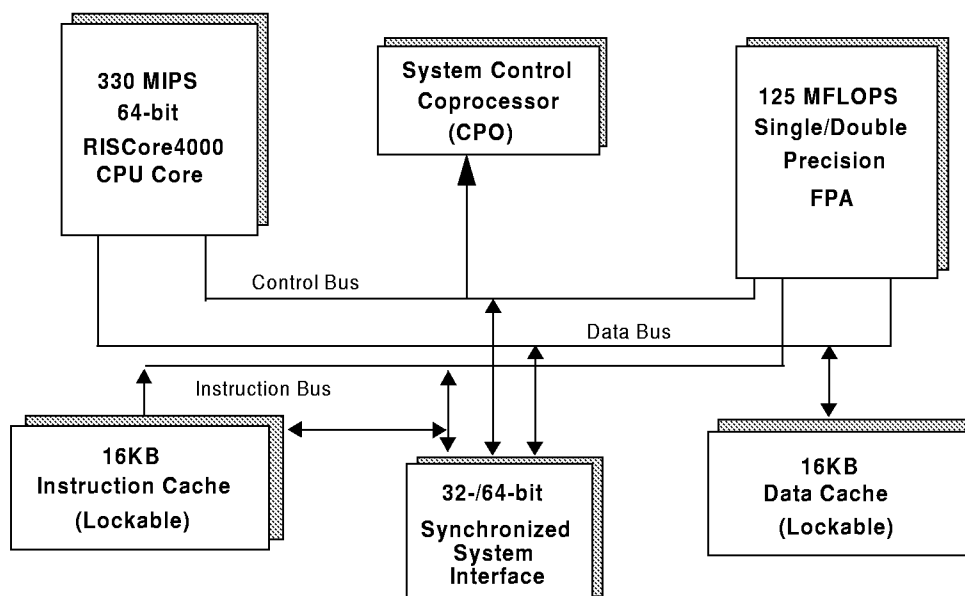
**RC64474™**  
**RC64475™**

**RISController**

## Features

- ♦ High performance 64-bit microprocessor, based on the RISCore4000
    - Minimized branch and load delays, through streamlined 5-stage scalar pipeline.
    - Single and double precision floating-point unit
    - 125 peak MFLOP/s at 250 MHz
    - 330 Dhrystone MIPS at 250 MHz
    - Flexible RC4700-compatible MMU
    - Joint TLB on-chip, for virtual-to-physical address mapping
  - ♦ On-chip two-way set associative caches
    - 16KB instruction cache (I-cache)
    - 16KB data cache (D-cache)
  - ♦ Optional I-cache and D-cache locking (per set), provides improved real-time support
  - ♦ Enhanced, flexible bus interface allows simple, low-cost design
    - 64-bit Bus Interface option, 1000MB/s bandwidth support
    - 32-bit Bus Interface option, 500MB/s bandwidth support
    - SDRAM timing protocol, through delayed data in write cycles
    - RC4000/RC5000 family bus-protocol compatibility
    - Bus runs at fraction of pipeline clock (1/2 to 1/8)
  - ♦ Implements MIPS-III Instruction Set Architecture (ISA)
  - ♦ 3.3V core with 3.3V I/O
- ♦ Software compatible with entire RISController Series of Embedded Microprocessors
  - ♦ Industrial temperature range support
  - ♦ Active power management
    - Powers down inactive units, through sleep-mode feature
  - ♦ 100% pin compatibility between RC64574, RC64474 and RC4640
  - ♦ 100% pin compatibility between RC64575, RC64475 and RC4650
  - ♦ RC64474 available in 128-pin QFP package, for 32-bit only systems
  - ♦ RC64475 available in 208-pin QFP package, for full 64/32 bit systems
  - ♦ Simplified board-level testing, through full Joint Test Action Group (JTAG) boundary scan
  - ♦ Windows® CE compliant

## Block diagram



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## Device overview<sup>1</sup>

Extending Integrated Device Technology's (IDT) RISCore4000 based choices (see Table 1), the RC64474 and RC64475 are high performance 64-bit microprocessors targeted towards applications that require high bandwidth, real-time response and rapid data processing and are ideal for products ranging from internetworking equipment (switches, routers) to multimedia systems such as web browsers, set-top boxes, video games, and Windows®CE based products. These processors are rated at 330 Dhrystone MIPS and 125 Million floating point operations per second, at 250 MHz. The internal cache bandwidth for these devices is over 3GB/second. The 64-bit external bus bandwidth is at more than 1000MB/s, and the 32-bit external bus bandwidth is at 500MB/s.

The RC64474 is packaged in a 128-pin QFP footprint package and uses a 32-bit external bus, offering the ideal combination of 64-bit processing power and 32-bit low-cost memory systems. The RC64475 is packaged in a 208-pin QFP footprint package and uses the full 64-bit external bus. The RC64475 is ideal for applications requiring 64-bit performance and 64-bit external bandwidth.

IDT's **RISCore4000** is a 250MHz 64-bit execution core that uses a 5-stage pipeline, eliminating the "issue restrictions" associated with other more complex pipelines. The RISCore4000 implements the MIPS-III Instruction Set Architecture (ISA) and is upwardly compatible with applications that run on earlier generation parts.

Implementation of the MIPS-III architecture results in 64-bit operations, improved performance for commonly used code sequences in

operating system kernels, and faster execution of floating-point intensive applications.

The **RISCore4000 integer unit** implements a load/store architecture with single cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all of the processor's logical and shift operations. Each unit is highly optimized and can perform an operation in a single pipeline cycle. Both 32- and 64-bit data operations are performed by the RISCore4000, utilizing 32 general purpose 64-bit registers (GPR) that are used for integer operations and address calculation. A complete on-chip floating-point co-processor (CP1), which includes a floating-point register file and execution units, forms a "seamless" interface, decoding and executing instructions in parallel with the integer unit.

**CP1's floating-point execution units** support both single and double precision arithmetic—as specified in the IEEE Standard 754—and are separated into a multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported, and the multiplier is partially pipelined, allowing the initiation of a new multiply instruction every fourth pipeline cycle.

The **floating-point register file** is made up of thirty-two 64-bit registers. The floating-point unit can take advantage of the 64-bit wide data cache and issue a co-processor load or store doubleword instruction in every cycle. The RISCore4000's **system control coprocessor (CP0) registers** are also incorporated on-chip and provide the path through which the virtual memory system's page mapping is examined and changed, exceptions are handled, and any operating mode selections are controlled.

<sup>1</sup> Detailed system operation information is provided in the RC64474/RC64475 user's manual.

## RISCore4000/RISCore5000 Family of Socket Compatible Processors

|                     | 32-bit Processors                               |                                                         |                                                         | 64-bit Processors                                      |                                                           |                                                           |
|---------------------|-------------------------------------------------|---------------------------------------------------------|---------------------------------------------------------|--------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|
|                     | RC4640                                          | RC64474                                                 | RC64574                                                 | RC4650                                                 | RC64475                                                   | RC64575                                                   |
| <b>CPU</b>          | 64-bit RISCore4000 w/ DSP extensions            | 64-bit RISCore4000                                      | 64-bit RISCore5000                                      | 64-bit RISCore4000 w/ DSP extensions                   | 64-bit RISCore4000                                        | 64-bit RISCore5000                                        |
| <b>Performance</b>  | >350MIPS                                        | >330MIPS                                                | >440MIPS                                                | >350MIPS                                               | >330MIPS                                                  | >440MIPS                                                  |
| <b>FPA</b>          | 89 mflops, single precision only                | 125 mflops, single and double precision                 | 666 mflops, single and double precision                 | 89 mflops, single precision only                       | 125 mflops, single and double precision                   | 666 mflops, single and double precision                   |
| <b>Caches</b>       | 8kB/8kB, 2-way, lockable by set                 | 16kB/16kB, 2-way, lockable by set                       | 32kB/32kB, 2-way, lockable by set                       | 8kB/8kB, 2-way, lockable by set                        | 16kB/16kB, 2-way, lockable by set                         | 32kB/32kB, 2-way, lockable by set                         |
| <b>External Bus</b> | 32-bit                                          | 32-bit, Superset pin compatible w/RC4640                | 32-bit, Superset pin compatible w/RC4640, RC64474       | 32- or 64-bit                                          | 32-or 64-bit, Superset pin compatible w/ RC4650           | 32-or 64-bit, Superset pin compatible w/ RC4650, RC64475  |
| <b>Voltage</b>      | 3.3V                                            | 3.3V                                                    | 2.5V                                                    | 3.3V                                                   | 3.3V                                                      | 2.5V                                                      |
| <b>Frequencies</b>  | 100-267 MHz                                     | 180-250 MHz                                             | 200-333 MHz                                             | 100-267 MHz                                            | 180-250 MHz                                               | 200-333 MHz                                               |
| <b>Packages</b>     | 128 PQFP                                        | 128 QFP                                                 | 128 QFP                                                 | 208 QFP                                                | 208 QFP                                                   | 208 QFP                                                   |
| <b>MMU</b>          | Base-Bounds                                     | 96 page TLB                                             | 96 page TLB                                             | Base-Bounds                                            | 96 page TLB                                               | 96 page TLB                                               |
| <b>Key Features</b> | Cache locking, on-chip MAC, 32-bit external bus | Cache locking, JTAG, syncDRAM mode, 32-bit external bus | Cache locking, JTAG, syncDRAM mode, 32-bit external bus | Cache locking, on-chip MAC, 32-bit & 64 bit bus option | Cache locking, JTAG, syncDRAM mode, 32-64- bit bus option | Cache locking, JTAG, syncDRAM mode, 32-64- bit bus option |

Table 1 RISCore4000/RISCore5000 Processor Family

A secure user processing environment is provided through the **user, supervisor, and kernel operating modes** of virtual addressing to system software. Bits in a status register determine which of these modes is used.

If configured for 64-bit **virtual addressing**, the virtual address space layout becomes an upwardly compatible extension of the 32-bit virtual address space layout. Figure 1 is an illustration of the address space layout for the 32-bit virtual address operation.

|            |                                                |
|------------|------------------------------------------------|
| 0xFFFFFFFF | Kernel virtual address space (kseg3)           |
| 0xE0000000 | Mapped, 0.5GB                                  |
| 0xDFFFFFFF | Supervisor virtual address space (sseg)        |
| 0xC0000000 | Mapped, 0.5GB                                  |
| 0xBFFFFFFF | Uncached kernel physical address space (kseg1) |
| 0xA0000000 | Unmapped, 0.5GB                                |
| 0x9FFFFFFF | Cached kernel physical address space (kseg0)   |
| 0x80000000 | Unmapped, 0.5GB                                |
| 0x7FFFFFFF | User virtual address space (useg)              |
| 0x00000000 | Mapped, 2.0GB                                  |

**Figure 1 Kernel Mode Virtual Addressing (32-bit Mode)**

The RC64474/RC64475's **Memory Management Unit (MMU)** controls the virtual memory system's page mapping and consists of a translation lookaside buffer (TLB) used for the virtual memory-mapping subsystem.

This large, **fully associative TLB** maps 96 virtual pages to their corresponding physical addresses. The TLB is organized as 48 pairs of even-odd entries and maps a virtual address and address space identifier into the large, 64GB physical address space. To assist in controlling the amount of mapped space and the replacement characteristics of various memory regions, two mechanisms are provided. First, the page size can be configured on a **per-entry basis**, to map a page size of 4KB to 16MB (in increments of 4x).

The second mechanism controls the replacement algorithm, when a TLB miss occurs. A random replacement algorithm is provided to select a TLB entry to be written with a new mapping; however, the processor provides a mechanism whereby a system specific number of mappings

can be locked into the TLB and avoid being randomly replaced, which facilitates the design of real-time systems, by allowing deterministic access to critical software.

The TLB also contains information to control the cache coherency protocol, and cache management algorithm for each page. However, hardware-based cache coherency is not supported.

The RC64474 and RC64475 enhance IDT's entire RISCore4000 series through the implementation of features such as boundary scan, to facilitate board level testing; enhanced support for SyncDRAM, to simplify system implementation and improve performance.

The RC64474/475 processors offer a **direct migration path** for designs based on IDT's RC4640/RC4650 processors<sup>2</sup>, through full pin and socket compatibility. Also, full 64-bit-family software and bus-protocol compatibility ensures the RC64474/475 access to a robust development tools infrastructure, allowing quicker time to market.

## Development tools

An array of hardware and software tools is available to assist system designers in the rapid development of RC64474/475 based systems. This accessibility allows a wide variety of customers to take full advantage of the device's high-performance features while addressing today's aggressive time-to-market demands.

## Cache memory

To keep the RC64474 and RC64475's high-performance pipeline full and operating efficiently, on-chip instruction and data caches have been incorporated. Each cache has its own data path and can be accessed in the same single pipeline clock cycle.

The 16KB two-way set associative **instruction cache (I-cache)** is virtually indexed, physically tagged, and word parity protected. Because this cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, further increasing performance by allowing both operations to occur simultaneously. The instruction cache provides a peak instruction bandwidth of 1000MB/sec at 250MHz.

The 16KB two-way set associative **data cache (D-cache)** is byte parity protected and has a fixed 32-byte (eight words) line size. Its tag is protected with a single parity bit. To allow simultaneous address translation and data cache access, the D-cache is virtually indexed and physically tagged. The data cache can provide 8 bytes each clock cycle, for a peak bandwidth of 2GB/sec.

To lock critical sections of code and/or data into the caches for quick access, a **"cache locking"** feature has been implemented. Once enabled, a cache is said to be locked when a particular piece of code or data is loaded into the cache and that cache location will not be selected later for refill by other data. This feature locks a set (8KB) of Instructions and/or Data.

Table 2 lists the RC64474/475 Instruction and data cache attributes.

<sup>2</sup> To ensure socket compatibility, refer to Table 8 and Table 9 at back of data sheet.

| Characteristics                 | Instruction                 | Data                                                     |
|---------------------------------|-----------------------------|----------------------------------------------------------|
| Size                            | 16KB                        | 16KB                                                     |
| Organization                    | 2-way set associative       | 2-way set associative                                    |
| Line size                       | 32B                         | 32B                                                      |
| read unit                       | 32-bits                     | 64-bits                                                  |
| write policy                    | na                          | write-back, write-through with or without write-allocate |
| Line transfer order             | sub-block order, for refill | sub-block order, for load sequential order, for store    |
| Miss restart after transfer of: | entire line                 | miss word                                                |
| Parity                          | per-word                    | per-byte                                                 |
| Cache locking                   | per set                     | per set                                                  |

Table 2 RC64474/RC64475 Instruction/Data Cache Attributes

## System interfaces

The RC64475 supports a 64-bit system interface that is bus compatible with the RC4650 and RC64575 system interface. The system interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus that is parity protected.

During 64-bit operation, RC64475 system address/data (SysAD) transfers are protected with an 8-bit parity check bus, SysADC. When initialized for 32-bit operation, the RC64475's SysAD can be viewed as a 32-bit multiplexed bus that is protected by 4 parity check bits.

The RC64474 supports a 32-bit system interface that is bus compatible with the RC4640. During 32-bit operation, SysAD transfers are performed on a 32-bit multiplexed bus (SysAD 31:0) that is protected by 4 parity check bits (SysADC 6:0).

Writes to external memory—whether they are cache miss write-backs, stores to uncached or write-through addresses—use the on-chip **write buffer**. The write buffer holds a maximum of four 64-bit addresses and 64-bit data pairs. The entire buffer is used for a data cache write-back and allows the processor to proceed in parallel with memory updates.

Included in the system interface are **six handshake signals**: RdRdy\*, WrRdy\*, ExtRqst\*, Release\*, ValidOut\*, and ValidIn\*; **six interrupt inputs**, and a **simple timing** specification that is capable of transferring data between the processor and memory at a peak rate of 1000MB/sec. A boot-time selectable option to run the system interface as 32-bits wide—using basically the same protocols as the 64-bit system—is also supported.

A **boot-time mode control interface** initializes fundamental processor modes. The boot-time mode control interface is a serial interface that operates at a very low frequency (MasterClock divided by 256). This low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively, the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL. The boot-time serial stream and configuration options are listed in Table 3.

The **clocking interface** allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock and can be between 25 and 125MHz. An on-chip **phase-locked-loop (PLL)** generates the pipeline clock (PClock) through multiplication of the system interface clock by values of 2,3,4,5,6,7 or 8, as defined at system reset. This allows the pipeline clock to be implemented at a significantly higher frequency than the system interface clock. The RC64474/475 support single data (one to eight bytes) and 8-word block transfers on the SysAD bus.

The RC64474/475 implement additional **write protocols** that **double the effective write bandwidth**. The write re-issue has a repeat rate of 2 cycles per write. Pipelined writes have the same 2-cycle per write repeat rate, but can issue an additional write after WrRdy\* de-asserts.

Choosing a 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles as well as whether a single data transfer—larger than 4 bytes—must be divided into two smaller transfers.

**Board-level testing** during Run-Time mode is facilitated through the full JTAG boundary scan facility. Six pins—TDI, TDO, TMS, TCK, TRST\* and JTAG32\*—have been incorporated to support the standard JTAG interface.

## System enhancement

To facilitate discrete **interface to SDRAM**, the RC64474/475 bus interface is enhanced during write cycles with a programmable delay that is inserted between the write address and the write data (for both block and non-block writes).

The bus delay can be defined as 0 to 7 MasterClock cycles and is activated and controlled through mode bit (17:15) settings selected during the reset initialization sequence. The '000' setting provides the same write operations timing protocol as the RC4640, RC4650, and RC5000 processors.

| Serial Bit | Description                                                                                          | Value & Mode Setting                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                          |
|------------|------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 255:18     | Reserved                                                                                             | Must be 0                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                          |
| 17:15      | WAdrWData_Del<br>Write address to write data delay in Master-Clock cycles. <sup>®</sup>              | 000 → 0 cycles<br>001 → 1 cycle<br>010 → 2 cycles<br>011 → 3 cycles<br>100 → 4 cycles<br>101 → 5 cycles<br>110 → 6 cycles<br>111 → 7 cycles                                           |                                                                                                                                                                                                                                                                                                                                                          |
| 14:13      | Drv_Out<br>output driver slew rate control. <b>Bit 14 is MSB.</b><br>Affects only non-clock outputs. | Output driver strength:<br>10 → 100% strength (fastest)<br>11 → 83% strength<br>00 → 67% strength<br>01 → 50% strength (slowest)                                                      |                                                                                                                                                                                                                                                                                                                                                          |
| 12         | System interface bus width                                                                           | 0 → 64-bit system interface<br>1 → 32-bit system interface                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                          |
| 11         | TmrIntEn<br>Disables the timer interrupt on Int*[5]                                                  | 0 → Enabled Timer Interrupt<br>1 → Disabled Timer Interrupt                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                          |
| 10:9       | Non-block write<br>Selects non-block write type. <b>Bit 10 is MSB.</b>                               | 00 → RC4x00 compatible<br>01 → Reserved<br>10 → Pipelined writes<br>11 → Write re-issue                                                                                               |                                                                                                                                                                                                                                                                                                                                                          |
| 7:5        | Clock Multiplier<br>MasterClock is multiplied internally to generate PClock                          | Clock multiplier:<br>0 Multiply by 2<br>1 Multiply by 3<br>2 Multiply by 4<br>3 Multiply by 5<br>4 Multiply by 6<br>5 Multiply by 7<br>6 Multiply by 8<br>7 Reserved                  |                                                                                                                                                                                                                                                                                                                                                          |
| 8          | EndBit<br>Specifies byte ordering                                                                    | 0 → Little endian<br>1 → Big endian                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                          |
| 4:1        | Writeback data rate<br>System interface data rate for block writes only: <b>bit 4 is MSB</b>         | 64-bit:<br>9:15 Reserved<br>8 → dxxdxxxddxxdxxx<br>7 → ddxxxxxdxxxxxx<br>6 → dxddxxdxxdx<br>5 → ddxxxxddxxx<br>4 → ddxxddxxx<br>3 → dxdxdxdx<br>2 → ddxddxx<br>1 → ddxddx<br>0 → dddd | 32-bit:<br>9:15 Reserved<br>8 → wxxxwxxxwxxxwxxxwxxxwxxxwxxxwxxx<br>7 → wwwxxxxwwxxxxwwxxxxwwxxxxwwxxxx<br>6 → wxwxwxwxwxwxwxwxwxwxwxwxwxwxwx<br>5 → wwxxxxwwwxxxxwwxxxxwwxxxx<br>4 → wwxxwwxxwwxxwwxxwwxxwwxxwwxx<br>3 → wxwxwxwxwxwxwxwxwxwxwxwxwxwxwx<br>2 → wwwxwwwxwwwxwwwxwwwxwwwxwwwx<br>1 → wwxxwxwxwxwxwxwxwxwxwxwxwxwxwxwx<br>0 → ÆE wwwwwwwww |
| 0          | Reserved                                                                                             | Must be zero                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                          |

Table 3 Boot-time Mode Stream

## Power management

Executing the WAIT instruction enables the processor to enter Standby mode. The internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins (Int[5:0]\*, NMI\*, ExtReq\*, Reset\*, and ColdReset\*) will continue to run. Once the CPU is in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

## Thermal considerations

The RC64474/475 come in a QFP with a drop-in heat spreader and are guaranteed in a case temperature range of 0° to +85° C, for commercial temperature devices; - 40° to +85° for industrial temperature devices. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature,  $T_A$ , can be calculated using the thermal resistance from case to ambient ( $\theta_{CA}$ ) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \theta_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum ICC specification for the device.

Typical values for  $\theta_{CA}$  at various airflows are shown in Table 4. Note that the RC64474/475 processors implement advanced power management, which substantially reduces the typical power dissipation of the device.

| Airflow (ft/min) | $\theta_{CA}$ |     |     |     |     |      |
|------------------|---------------|-----|-----|-----|-----|------|
|                  | 0             | 200 | 400 | 600 | 800 | 1000 |
| 128 QFP          | 20            | 12  | 9   | 8   | 7   | 6    |
| 208 QFP          | 20            | 12  | 9   | 8   | 7   | 6    |

Table 4 Thermal Resistance ( $\theta_{CA}$ ) at Various Airflows

## Data sheet revision history

### Data sheet revision history

**December 1998:** Changed ordering code on 128-pin package from DQ / DQI (Industrial) to DZ / DZI (Industrial).

**January 1999:** Removed 5V tolerance capability and deleted 5V tolerant pin.

**February 1999:** Changed the package drawings to reflect the new 208-pin DP (DPI) and 128-pin DZ (DZI) packages.

**May 1999:**

Removed "Preliminary" status from data sheet.

Changes in DC Electrical Characteristics table.

Changes in Pin Description table.

Changes in Clock Parameters table.

Changes in System Interface Parameters table.

**September 1999:** Updated Revision History section.

## Pin description table

The following is a list of system interface pins available on the RC64474/475. Pin names ending with an asterisk (\*) are active when low.

| Pin Name                | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>System Interface</b> |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| ExtRqst*                | I    | <b>External request</b><br>An external agent asserts ExtRqst* to request use of the System interface. The processor grants the request by asserting Release*.                                                                                                                                                                                                                                                                                                                                                                          |
| Release*                | O    | <b>Release interface</b><br>In response to the assertion of ExtRqst* or a CPU read request, the processor asserts Release* and signals to the requesting device that the system interface is available.                                                                                                                                                                                                                                                                                                                                |
| RdRdy*                  | I    | <b>Read Ready</b><br>The external agent asserts RdRdy* to indicate that it can accept a processor read request.                                                                                                                                                                                                                                                                                                                                                                                                                        |
| WrRdy*                  | I    | <b>Write Ready</b><br>An external agent asserts WrRdy* when it can now accept a processor write request.                                                                                                                                                                                                                                                                                                                                                                                                                               |
| ValidIn*                | I    | <b>Valid Input</b><br>Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.                                                                                                                                                                                                                                                                                                                                                                 |
| ValidOut*               | O    | <b>Valid output</b><br>Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.                                                                                                                                                                                                                                                                                                                                                                    |
| SysAD(63:0)             | I/O  | <b>System address/data bus</b><br>A 64-bit address and data bus for communication between the processor and an external agent. During address phases only, SysAd(35:0) contains valid address information. The remaining SysAD(63:36) pins are not used. The whole 64-bit SysAD(63:0) may be used during the data transfer phase.<br>In 32-bit mode and in the RC64474, SysAD(63:32) is not used, regardless of Endianness. A 32-bit address and data communication between processor and external agent is performed via SysAD(31:0). |
| SysADC(7:0)             | I/O  | <b>System address/data check bus</b><br>An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.<br>In 32-bit mode and in the RC64474, SysADC(7:4) is not used. The SysADC(3:0) contains check bits for SysAD(31:0).                                                                                                                                                                                                                                                                                        |
| SysCmd(8:0)             | I/O  | <b>System command/data identifier bus</b><br>A 9-bit bus for command and data identifier transmission between the processor and an external agent.                                                                                                                                                                                                                                                                                                                                                                                     |
| SysCmdP                 | I/O  | <b>System Command Parity</b><br>A single, even-parity bit for the Syscmd bus. This signal is always driven low.                                                                                                                                                                                                                                                                                                                                                                                                                        |

Table 5 Pin Descriptions (Page 1 of 3)

| Pin Name                        | Type | Description                                                                                                                                                                                                                                                                              |
|---------------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Clock/Control Interface</b>  |      |                                                                                                                                                                                                                                                                                          |
| MasterClock                     | I    | <b>Master Clock</b><br>Master clock input establishes the processor and bus operating frequency. It is multiplied internally by 2,3,4,5,6,7,8 to generate the pipeline clock (PClock). This clock must be driven by 3.3V (Vcc) clock signals, regardless of the 5V tolerant pin setting. |
| VccP                            | I    | <b>Quiet VCC for PLL</b><br>Quiet Vcc for the internal phase locked loop.                                                                                                                                                                                                                |
| VssP                            | I    | <b>Quiet Vss for PLL</b><br>Quiet Vss for the internal phase locked loop.                                                                                                                                                                                                                |
| <b>Interrupt Interface</b>      |      |                                                                                                                                                                                                                                                                                          |
| Int*(5:0)                       | I    | <b>Interrupt</b><br>Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.                                                                                                                                                                             |
| NMI*                            | I    | <b>Non-maskable interrupt</b><br>Non-maskable interrupt, ORed with bit 6 of the interrupt register.                                                                                                                                                                                      |
| <b>Initialization Interface</b> |      |                                                                                                                                                                                                                                                                                          |
| VccOk                           | I    | <b>Vcc is OK</b><br>When asserted, this signal indicates to the processor that the power supply has been above the Vcc minimum for more than 100 milliseconds and will remain stable. The assertion of VccOk initiates the initialization sequence.                                      |
| ColdReset*                      | I    | <b>Cold reset</b><br>This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with MasterClock.                                                                                                                                    |
| Reset*                          | I    | <b>Reset</b><br>This signal must be asserted for any reset sequence. It can be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterClock.                                           |
| ModeClock                       | O    | <b>Boot-mode clock</b><br>Serial boot-mode data clock output at the system clock frequency divided by two hundred fifty-six.                                                                                                                                                             |
| ModeIn                          | I    | <b>Boot-mode data in</b><br>Serial boot-mode data input.                                                                                                                                                                                                                                 |

Table 5 Pin Descriptions (Page 2 of 3)



| Pin Name              | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>JTAG Interface</b> |      |                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| TDI                   | I    | <b>JTAG Data In</b><br>On the rising edge of TCK, serial input data are shifted into either the Instruction register or Data register, depending on the TAP controller state.                                                                                                                                                                                                                                                            |
| TDO                   | O    | <b>JTAG Data Out</b><br>On the falling edge of TCK, the TDO is serial data shifted out from either the instruction or data register. When no data is shifted out, the TDO is tri-stated (high impedance).                                                                                                                                                                                                                                |
| TCK                   | I    | <b>JTAG Clock Input</b><br>An input test clock used to shift into or out of the boundary-scan register cells. TCK is independent of the system and processor clock with nominal 40-60% duty cycle.                                                                                                                                                                                                                                       |
| TMS                   | I    | <b>JTAG Command Select</b><br>The logic signal received at the TMS input is decoded by the TAP controller to control test operation. TMS is sampled on the rising edge of TCK.                                                                                                                                                                                                                                                           |
| TRST*                 | I    | <b>JTAG Reset</b><br>The TRST* pin is an active-low signal used for asynchronous reset of the debug unit, independent of the processor logic. During normal CPU operation, the JTAG controller will be held in the reset mode, asserting this active low pin.<br>When asserted low, this pin will also tristate the TDO pin.                                                                                                             |
| JTAG32*               | I    | <b>JTAG 32-bit scan</b><br>This pin is used to control length of the scan chain for SYsAD (32-bit or 64-bit) for the JTAG mode. When set to Vss, 32-bit bus mode is selected. In this mode, only SysAD(31:0) are part of the scan chain. When set to Vcc, 64-bit bus mode is selected. In this mode, SysAD(63:0) are part of the scan chain. This pin has a built-in pull-down device to guarantee 32-bit scan, if it is left uncovered. |
| JR_Vcc                | I    | <b>JTAG VCC</b><br>This pin has an internal pull-down to continuously reset the JTAG controller (if left unconnected) bypassing the TRst* pin. When supplied with Vcc, the TRst* pin will be the primary control for the JTAG reset.                                                                                                                                                                                                     |

Table 5 Pin Descriptions (Page 3 of 3)

## Logic diagram — RC64474/RC64475

Figure 2 illustrates the direction and functional groupings for the processor signals.

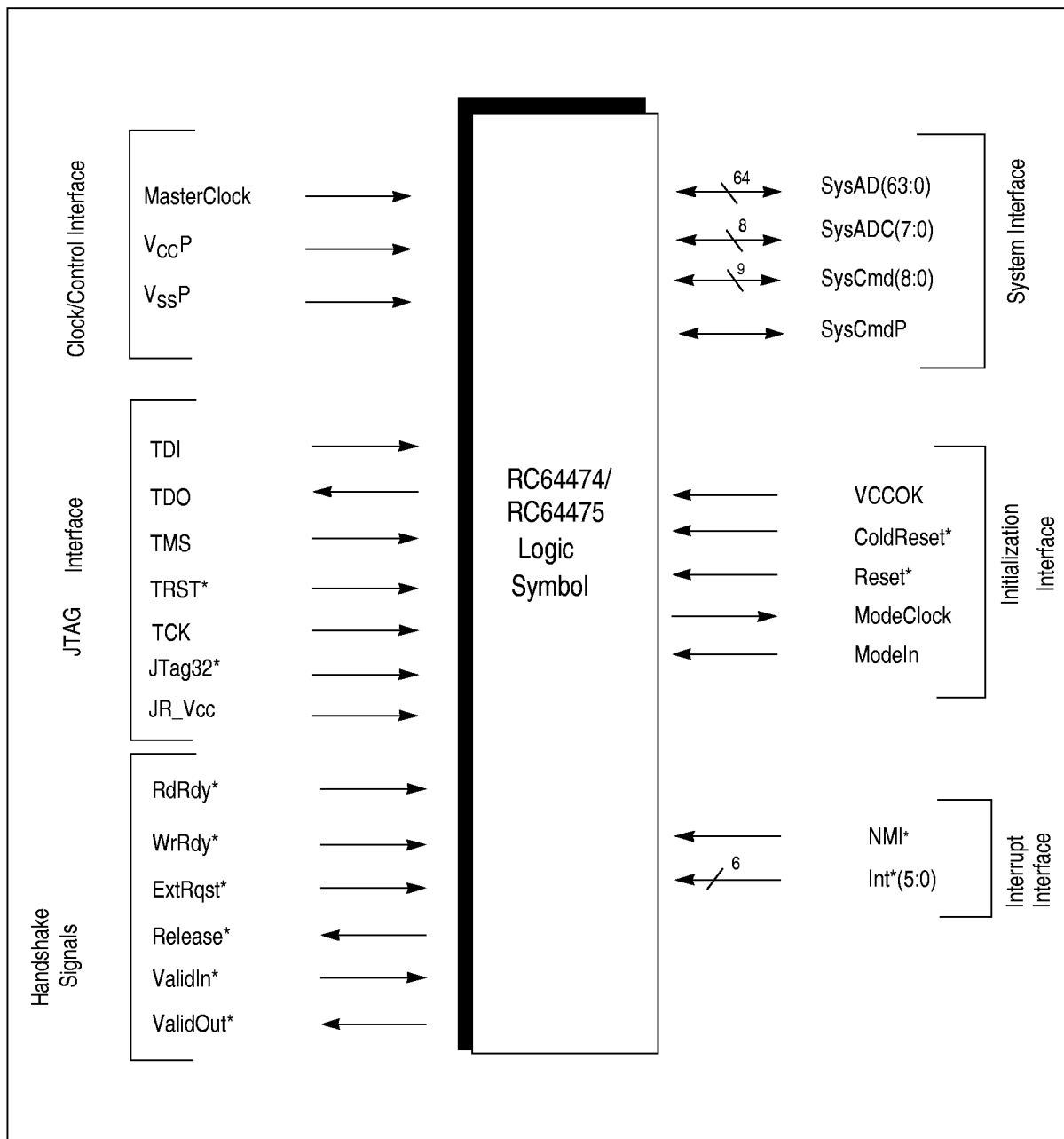


Figure 2 Logic Diagram for RC64474/RC64475

**RC64475 208-pin QFP package pin-out**

Pin names followed by an asterisk (\*) are active when low. For maximum flexibility and compatibility with future designs, N.C. pins should be left floating.

| Pin | Function        | Pin | Function        | Pin | Function        | Pin | Function           |
|-----|-----------------|-----|-----------------|-----|-----------------|-----|--------------------|
| 1   | N.C.            | 53  | JTAG32*         | 105 | N.C.            | 157 | N.C.               |
| 2   | N.C.            | 54  | N.C.            | 106 | N.C.            | 158 | N.C.               |
| 3   | N.C.            | 55  | N.C.            | 107 | N.C.            | 159 | SysAD59            |
| 4   | N.C.            | 56  | N.C.            | 108 | N.C.            | 160 | ColdReset*         |
| 5   | N.C.            | 57  | SysCmd2         | 109 | N.C.            | 161 | SysAD28            |
| 6   | N.C.            | 58  | SysAD36         | 110 | N.C.            | 162 | VCC                |
| 7   | N.C.            | 59  | SysAD4          | 111 | N.C.            | 163 | V <sub>SS</sub>    |
| 8   | N.C.            | 60  | SysCmd1         | 112 | N.C.            | 164 | SysAD60            |
| 9   | N.C.            | 61  | V <sub>SS</sub> | 113 | N.C.            | 165 | Reset*             |
| 10  | SysAD11         | 62  | V <sub>cc</sub> | 114 | SysAD52         | 166 | SysAD29            |
| 11  | V <sub>SS</sub> | 63  | SysAD35         | 115 | ExtRqst*        | 167 | SysAD61            |
| 12  | V <sub>cc</sub> | 64  | SysAD3          | 116 | V <sub>cc</sub> | 168 | SysAD30            |
| 13  | SysCmd8         | 65  | SysCmd0         | 117 | V <sub>SS</sub> | 169 | V <sub>cc</sub>    |
| 14  | SysAD42         | 66  | SysAD34         | 118 | SysAD21         | 170 | V <sub>SS</sub>    |
| 15  | SysAD10         | 67  | V <sub>SS</sub> | 119 | SysAD53         | 171 | SysAD62            |
| 16  | SysCmd7         | 68  | V <sub>cc</sub> | 120 | RdRdy*          | 172 | SysAD31            |
| 17  | V <sub>SS</sub> | 69  | SysAD2          | 121 | Modein          | 173 | SysAD63            |
| 18  | V <sub>cc</sub> | 70  | Int5*           | 122 | SysAD22         | 174 | V <sub>cc</sub>    |
| 19  | SysAD41         | 71  | SysAD33         | 123 | SysAD54         | 175 | V <sub>SS</sub>    |
| 20  | SysAD9          | 72  | SysAD1          | 124 | V <sub>cc</sub> | 176 | V <sub>cc</sub> OK |
| 21  | SysCmd6         | 73  | V <sub>SS</sub> | 125 | V <sub>SS</sub> | 177 | SysADC3            |
| 22  | SysAD40         | 74  | V <sub>cc</sub> | 126 | Release*        | 178 | SysADC7            |
| 23  | V <sub>SS</sub> | 75  | Int4*           | 127 | SysAD23         | 179 | N.C.               |
| 24  | V <sub>cc</sub> | 76  | SysAD32         | 128 | SysAD55         | 180 | TDI                |
| 25  | SysAD8          | 77  | SysAD0          | 129 | NMI*            | 181 | TRst*              |
| 26  | SysCmd5         | 78  | Int3*           | 130 | V <sub>cc</sub> | 182 | TCK                |
| 27  | SysADC4         | 79  | V <sub>SS</sub> | 131 | V <sub>SS</sub> | 183 | TMS                |
| 28  | SysADC0         | 80  | V <sub>cc</sub> | 132 | SysADC2         | 184 | TDO                |
| 29  | V <sub>SS</sub> | 81  | Int2*           | 133 | SysADC6         | 185 | V <sub>cc</sub> P  |
| 30  | V <sub>cc</sub> | 82  | SysAD16         | 134 | SysAD24         | 186 | V <sub>SS</sub> P  |
| 31  | SysCmd4         | 83  | SysAD48         | 135 | V <sub>cc</sub> | 187 | MasterClock        |
| 32  | SysAD39         | 84  | Int1*           | 136 | V <sub>SS</sub> | 188 | V <sub>cc</sub>    |
| 33  | SysAD7          | 85  | V <sub>SS</sub> | 137 | SysAD56         | 189 | V <sub>SS</sub>    |

Table 6 RC64475 208-pin QFP Package Pin-Out (Page 1 of 2)

| Pin | Function        | Pin | Function        | Pin | Function           | Pin | Function        |
|-----|-----------------|-----|-----------------|-----|--------------------|-----|-----------------|
| 34  | SysCmd3         | 86  | V <sub>cc</sub> | 138 | SysAD25            | 190 | SysADC5         |
| 35  | V <sub>ss</sub> | 87  | SysAD17         | 139 | SysAD57            | 191 | SysADC1         |
| 36  | V <sub>cc</sub> | 88  | SysAD49         | 140 | N.C.               | 192 | V <sub>cc</sub> |
| 37  | SysAD38         | 89  | Int0*           | 141 | V <sub>ss</sub>    | 193 | V <sub>ss</sub> |
| 38  | SysAD6          | 90  | SysAD18         | 142 | N.C                | 194 | SysAD47         |
| 39  | ModeClock       | 91  | V <sub>ss</sub> | 143 | SysAD26            | 195 | SysAD15         |
| 40  | WrRdy*          | 92  | V <sub>cc</sub> | 144 | SysAD58            | 196 | SysAD46         |
| 41  | SysAD37         | 93  | SysAD50         | 145 | N.C.               | 197 | V <sub>cc</sub> |
| 42  | SysAD5          | 94  | ValidIn*        | 146 | V <sub>cc</sub>    | 198 | V <sub>ss</sub> |
| 43  | V <sub>ss</sub> | 95  | SysAD19         | 147 | V <sub>ss</sub>    | 199 | SysAD14         |
| 44  | V <sub>cc</sub> | 96  | SysAD51         | 148 | SysAD27            | 200 | SysAD45         |
| 45  | N.C.            | 97  | V <sub>ss</sub> | 149 | N.C.               | 201 | SysAD13         |
| 46  | N.C.            | 98  | V <sub>cc</sub> | 150 | JR_V <sub>cc</sub> | 202 | SysAD44         |
| 47  | N.C.            | 99  | ValidOut*       | 151 | N.C.               | 203 | V <sub>ss</sub> |
| 48  | N.C.            | 100 | SysAD20         | 152 | N.C.               | 204 | V <sub>cc</sub> |
| 49  | N.C.            | 101 | N.C.            | 153 | N.C.               | 205 | SysAD12         |
| 50  | N.C.            | 102 | N.C.            | 154 | N.C.               | 206 | SysCmdP         |
| 51  | N.C.            | 103 | N.C.            | 155 | N.C.               | 207 | SysAD43         |
| 52  | N.C.            | 104 | N.C.            | 156 | N.C.               | 208 | N.C.            |

Table 6 RC64475 208-pin QFP Package Pin-Out (Page 2 of 2)

## RC64474 128-pin QFP package pin-out

| Pin | Function        | Pin | Function        | Pin | Function           | Pin | Function        |
|-----|-----------------|-----|-----------------|-----|--------------------|-----|-----------------|
| 1   | JTAG32*         | 33  | V <sub>cc</sub> | 65  | V <sub>cc</sub>    | 97  | V <sub>cc</sub> |
| 2   | SysCmd2         | 34  | V <sub>ss</sub> | 66  | SysAD28            | 98  | V <sub>ss</sub> |
| 3   | V <sub>cc</sub> | 35  | SysAD13         | 67  | ColdReset*         | 99  | SysAD19         |
| 4   | V <sub>ss</sub> | 36  | SysAD14         | 68  | SysAD27            | 100 | ValidIn*        |
| 5   | SysAD5          | 37  | V <sub>ss</sub> | 69  | V <sub>ss</sub>    | 101 | V <sub>cc</sub> |
| 6   | WrRdy*          | 38  | V <sub>cc</sub> | 70  | V <sub>cc</sub>    | 102 | V <sub>ss</sub> |
| 7   | ModeClock       | 39  | SysAD15         | 71  | JR_V <sub>cc</sub> | 103 | SysAD18         |
| 8   | SysAD6          | 40  | V <sub>ss</sub> | 72  | SysAD26            | 104 | Int0*           |
| 9   | V <sub>cc</sub> | 41  | V <sub>cc</sub> | 73  | N.C.               | 105 | SysAD17         |
| 10  | V <sub>ss</sub> | 42  | SysADC1         | 74  | V <sub>ss</sub>    | 106 | V <sub>cc</sub> |
| 11  | SysCmd3         | 43  | V <sub>ss</sub> | 75  | N.C.               | 107 | V <sub>ss</sub> |
| 12  | SysAd7          | 44  | V <sub>cc</sub> | 76  | SysAD25            | 108 | Int1*           |

Table 7 RC64474 128-pin QFP Package Pin-out (Page 1 of 2)

| Pin | Function | Pin | Function    | Pin | Function  | Pin | Function |
|-----|----------|-----|-------------|-----|-----------|-----|----------|
| 13  | SysCmd4  | 45  | MasterClock | 77  | Vss       | 109 | SysAD16  |
| 14  | Vcc      | 46  | VssP        | 78  | Vcc       | 110 | Int2*    |
| 15  | Vss      | 47  | VccP        | 79  | SysAD24   | 111 | Vcc      |
| 16  | SysAdC0  | 48  | TDO         | 80  | SysADC2   | 112 | Vss      |
| 17  | SysCmd5  | 49  | TMS         | 81  | Vss       | 113 | Int3*    |
| 18  | SysAD8   | 50  | TCK         | 82  | Vcc       | 114 | SysAD0   |
| 19  | Vcc      | 51  | TRst*       | 83  | NMI*      | 115 | Int4*    |
| 20  | Vss      | 52  | TDI         | 84  | SysAD23   | 116 | Vcc      |
| 21  | SysCmd6  | 53  | Vss         | 85  | Release*  | 117 | Vss      |
| 22  | SysAD9   | 54  | SysADC3     | 86  | Vss       | 118 | SysAD1   |
| 23  | Vcc      | 55  | VccOK       | 87  | Vcc       | 119 | Int5*    |
| 24  | Vss      | 56  | Vss         | 88  | SysAD22   | 120 | SysAD2   |
| 25  | SysCCmd7 | 57  | Vcc         | 89  | Modein    | 121 | Vcc      |
| 26  | SysAD10  | 58  | SysAD31     | 90  | RdRdy*    | 122 | Vss      |
| 27  | SysCmd8  | 59  | Vss         | 91  | SysAD21   | 123 | SysCmd0  |
| 28  | Vcc      | 60  | Vcc         | 92  | Vss       | 124 | SysAd3   |
| 29  | Vss      | 61  | SysAD30     | 93  | Vcc       | 125 | Vcc      |
| 30  | SysAD11  | 62  | SysAD29     | 94  | ExtRqst*  | 126 | Vss      |
| 31  | SysCmdP  | 63  | Reset*      | 95  | SysAD20   | 127 | SysCmd1  |
| 32  | SysAD12  | 64  | Vss         | 96  | ValidOut* | 128 | SysAD4   |

Table 7 RC64474 128-pin QFP Package Pin-out (Page 2 of 2)

## Socket compatibility—RC64474 & RC4640

To ensure socket compatibility between the RC4640 and the RC64474 devices, several pin changes are required, as shown below.

| Pin | RC4640          | RC64574/<br>RC64474 | Compatible to<br>RV4640? | Comments                                                                                                    |
|-----|-----------------|---------------------|--------------------------|-------------------------------------------------------------------------------------------------------------|
| 1   | N.C             | JTAG32*             | Yes.                     | Pin has an internal pull-down, to enable 32-bit scan.<br>Can also be left a N.C.                            |
| 48  | V <sub>ss</sub> | TDO                 | Yes.                     | Can be driven with V <sub>ss</sub> , if JTAG is not needed. Is tristated when TRst* is low.                 |
| 49  | V <sub>ss</sub> | TMS                 | Yes.                     | Can be driven with V <sub>ss</sub> if JTAG is not needed.                                                   |
| 50  | V <sub>ss</sub> | TCK                 | Yes.                     | Can be driven with V <sub>ss</sub> if JTAG is not needed.                                                   |
| 51  | V <sub>ss</sub> | TRst*               | Yes.                     | Can be driven with V <sub>ss</sub> if JTAG is not needed.                                                   |
| 52  | V <sub>ss</sub> | TDI                 | Yes.                     | Can be driven with V <sub>ss</sub> if JTAG is not needed.                                                   |
| 71  | N.C.            | JR_V <sub>cc</sub>  | Yes.                     | Can be left N.C. in RC64474, if JTAG is not need. If JTAG is needed, it must be driven to V <sub>cc</sub> . |

Table 8 RC64574 Socket Compatibility to RC64474 and R4640

## Socket compatibility—RC64475 & RC4650

| Pin | RV4650<br>32-bit | RC64575<br>32-bit<br>RC64475<br>32-bit | RV4650<br>64-bit | RC64575<br>64-bit<br>RC64475<br>64-bit | Compatible<br>to RV4650? | Comments                                                                                                                                                                        |
|-----|------------------|----------------------------------------|------------------|----------------------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 53  | N.C.             | JTAG32*                                | No Connect       | JTAG32*                                | Yes                      | In 32-bit, this pin can be left unconnected because of internal pull-down.<br>In 64-bit, this assumes that JTAG will not be used. If using JTAG, this pin must be at $V_{CC}$ . |
| 150 | N.C.             | JR_ $V_{CC}$                           | No Connect       | JR_ $V_{CC}$                           | Yes                      | In RC64475, can be left a N.C. if JTAG is not need. If JTAG is needed, it must be driven to $V_{CC}$ .                                                                          |
| 180 | N.C.             | TDI                                    | No Connect       | TDO                                    | Yes                      | If JTAG is not needed, can be left a N.C.                                                                                                                                       |
| 181 | N.C.             | TRsT*                                  | No Connect       | TRsT*                                  | Yes                      | If JTAG is not needed, can be left a N.C.                                                                                                                                       |
| 182 | N.C.             | TCK                                    | No Connect       | TCK                                    | Yes                      | If JTAG is not needed, can be left a N.C.                                                                                                                                       |
| 183 | N.C.             | TMS                                    | No Connect       | TMS                                    | Yes                      | If JTAG is not needed, can be left a N.C.                                                                                                                                       |
| 184 | N.C.             | TDO                                    | No Connect       | TDIO                                   | Yes                      | If JTAG is not needed, can be left a N.C.                                                                                                                                       |

Table 9 RC64575 Socket Compatibility to RC64475 &amp; RC4650

### Absolute maximum ratings

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

| Symbol     | Rating                               | RC64474/475<br>3.3V±5%    | RC64474/475<br>3.3V±5%    | Unit |
|------------|--------------------------------------|---------------------------|---------------------------|------|
|            |                                      | Commercial                | Industrial                |      |
| $V_{TERM}$ | Terminal Voltage with respect to GND | −0.5 <sup>1</sup> to +4.6 | −0.5 <sup>1</sup> to +4.6 | V    |
| $T_C$      | Operating Temperature(case)          | 0 to +85                  | −40 to +85                | °C   |
| $T_{BIAS}$ | Case Temperature Under Bias          | −55 to +125               | −55 to +125               | °C   |
| $T_{STG}$  | Storage Temperature                  | −55 to +125               | −55 to +125               | °C   |
| $I_{IN}$   | DC Input Current                     | 20 <sup>2</sup>           | 20 <sup>2</sup>           | mA   |
| $I_{OUT}$  | DC Output Current                    | 50 <sup>3</sup>           | 50 <sup>3</sup>           | mA   |

<sup>1</sup>.  $V_{IN}$  minimum = −2.0V for pulse width less than 15ns.  $V_{IN}$  should not exceed  $V_{CC}$  +0.5 Volts.

<sup>2</sup>. When  $V_{IN} < 0V$  or  $V_{IN} > V_{CC}$

<sup>3</sup>. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

**Recommended operation temperature and supply voltage**

| Grade      | Temperature         | Gnd | RC64474/475     |
|------------|---------------------|-----|-----------------|
|            |                     |     | V <sub>CC</sub> |
| Commercial | 0°C to +85°C (Case) | 0V  | 3.3V±5%         |
| Industrial | -40 + 85°C (Case)   | 0V  | 3.3V±5%         |

**DC electrical characteristics**

Commercial Temperature Range—RC64474/64475

(V<sub>CC</sub> = 3.3±5%, T<sub>CASE</sub> = 0°C to +85°C)

| Parameter           | RC64474/RC64475<br>180MHz |                        | RC64474/RC64475<br>200MHz |                        | RC64474/RC64475<br>250MHz |                        | Conditions                            |
|---------------------|---------------------------|------------------------|---------------------------|------------------------|---------------------------|------------------------|---------------------------------------|
|                     | Minimum                   | Maximum                | Minimum                   | Maximum                | Minimum                   | Maximum                |                                       |
| V <sub>OL</sub>     | —                         | 0.1V                   | —                         | 0.1V                   | —                         | 0.1V                   | I <sub>OUT</sub>   = 20uA             |
| V <sub>OH</sub>     | V <sub>CC</sub> - 0.1V    | —                      | V <sub>CC</sub> - 0.1V    | —                      | V <sub>CC</sub> - 0.1V    | —                      |                                       |
| V <sub>OL</sub>     | —                         | 0.4V                   | —                         | 0.4V                   | —                         | 0.4V                   | I <sub>OUT</sub>   = 4mA              |
| V <sub>OH</sub>     | 2.4V                      | —                      | 2.4V                      | —                      | 2.4V                      | —                      |                                       |
| V <sub>IL</sub>     | -0.5V                     | 0.2V <sub>CC</sub>     | -0.5V                     | 0.2V <sub>CC</sub>     | -0.5V                     | 0.2V <sub>CC</sub>     | —                                     |
| V <sub>IH</sub>     | 2.0V                      | V <sub>CC</sub> + 0.5V | 2.0V                      | V <sub>CC</sub> + 0.5V | 2.0V                      | V <sub>CC</sub> + 0.5V | —                                     |
| I <sub>IN</sub>     | —                         | ±10uA                  | —                         | ±10uA                  | —                         | ±10uA                  | 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> |
| C <sub>IN</sub>     | —                         | 10pF                   | —                         | 10pF                   | —                         | 10pF                   | —                                     |
| C <sub>OUT</sub>    | —                         | 10pF                   | —                         | 10pF                   | —                         | 10pF                   | —                                     |
| I/O <sub>LEAK</sub> | —                         | 20uA                   | —                         | 20uA                   | —                         | 20uA                   | Input/Output Leakage                  |

**Power consumption—RC64474**

| Parameter         |         | RC64474 180MHz       |                      | RC64474 200MHz       |                      | RC64474 250MHz       |                     | Conditions                                                                                            |
|-------------------|---------|----------------------|----------------------|----------------------|----------------------|----------------------|---------------------|-------------------------------------------------------------------------------------------------------|
|                   |         | Typical <sup>1</sup> | Max                  | Typical <sup>1</sup> | Max                  | Typical <sup>1</sup> | Max                 |                                                                                                       |
| System Condition: |         | 180/90MHz            |                      | 200/100MHz           |                      | 250/125MHz           |                     | —                                                                                                     |
| I <sub>CC</sub>   | standby | —                    | 60 mA <sup>2</sup>   | —                    | 60 mA <sup>2</sup>   | —                    | 100 mA <sup>2</sup> | C <sub>L</sub> = 0pF <sup>3</sup>                                                                     |
|                   |         | —                    | 110 mA <sup>2</sup>  | —                    | 110 mA <sup>2</sup>  | —                    | 110 mA <sup>2</sup> | C <sub>L</sub> = 50pF                                                                                 |
|                   | active  | 530 mA <sup>2</sup>  | 630 mA <sup>2</sup>  | 600mA <sup>2</sup>   | 700 mA <sup>2</sup>  | 700 mA <sup>2</sup>  | 850mA <sup>2</sup>  | C <sub>L</sub> = 0pF<br>No SysAd activity <sup>3</sup>                                                |
|                   |         | 630mA <sup>2</sup>   | 750 mA <sup>2</sup>  | 700 mA <sup>2</sup>  | 850 mA <sup>2</sup>  | 850mA <sup>2</sup>   | 1000mA <sup>2</sup> | C <sub>L</sub> = 50pF<br>R4x00 compatible writes,<br>T <sub>C</sub> = 25°C                            |
|                   |         | 750 mA <sup>2</sup>  | 1050 mA <sup>4</sup> | 850 mA <sup>2</sup>  | 1200 mA <sup>4</sup> | 1000mA <sup>2</sup>  | 1400mA <sup>2</sup> | C <sub>L</sub> = 50pF<br>Pipelined writes or write<br>re-issue,<br>T <sub>C</sub> = 25°C <sup>3</sup> |

<sup>1</sup>. Typical integer instruction mix and cache miss rates

<sup>2</sup>. These are not tested. They are the results of engineering analysis and are provided for reference only

<sup>3</sup>. Guaranteed by design.

<sup>4</sup>. These are the specifications IDT tests to insure compliance.

**Power consumption—RC64475**

| Parameter         |                                              | RC64475 180MHz       |                      | RC64475 200MHz       |                      | RC64475 250MHz       |                      | Conditions                                                                                            |
|-------------------|----------------------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|-------------------------------------------------------------------------------------------------------|
|                   |                                              | Typical <sup>1</sup> | Max                  | Typical <sup>1</sup> | Max                  | Typical <sup>1</sup> | Max                  |                                                                                                       |
| System Condition: |                                              | 180/90MHz            |                      | 200/100MHz           |                      | 250/125MHz           |                      | —                                                                                                     |
| I <sub>CC</sub>   | standby                                      | —                    | 60 mA <sup>2</sup>   | —                    | 60 mA <sup>2</sup>   | —                    | 100 mA <sup>2</sup>  | C <sub>L</sub> = 0pF <sup>3</sup>                                                                     |
|                   |                                              | —                    | 110 m <sup>2</sup> A | —                    | 110 mA <sup>2</sup>  | —                    | 110 mA <sup>2</sup>  | C <sub>L</sub> = 50pF                                                                                 |
|                   | active,<br>64-bit bus<br>option <sup>4</sup> | 720 mA <sup>2</sup>  | 850 mA <sup>2</sup>  | 850 mA <sup>2</sup>  | 1000 mA <sup>2</sup> | 935 mA <sup>2</sup>  | 1100 mA <sup>2</sup> | C <sub>L</sub> = 0pF<br>No SysAd activity <sup>3</sup>                                                |
|                   |                                              | 850 mA <sup>2</sup>  | 1000 mA <sup>2</sup> | 1000 mA <sup>2</sup> | 1200 mA <sup>2</sup> | 1100mA <sup>2</sup>  | 1360mA <sup>2</sup>  | C <sub>L</sub> = 50pF<br>R4x00 compatible writes,<br>T <sub>C</sub> = 25°C                            |
|                   |                                              | 1000 mA <sup>2</sup> | 1200 mA <sup>5</sup> | 1200 mA <sup>2</sup> | 1400 mA <sup>5</sup> | 1360 mA <sup>2</sup> | 1600 mA <sup>2</sup> | C <sub>L</sub> = 50pF<br>Pipelined writes or write<br>re-issue,<br>T <sub>C</sub> = 25°C <sup>3</sup> |

<sup>1</sup>. Typical integer instruction mix and cache miss rates

<sup>2</sup>. These are not tested. They are the results of engineering analysis and are provided for reference only.

<sup>3</sup>. Guaranteed by design.

<sup>4</sup>. In 32-bit bus option, use RC64474 power consumption values.

<sup>5</sup>. These are the specifications IDT tests to insure compliance.



## Timing characteristics—RC64474/RC64475

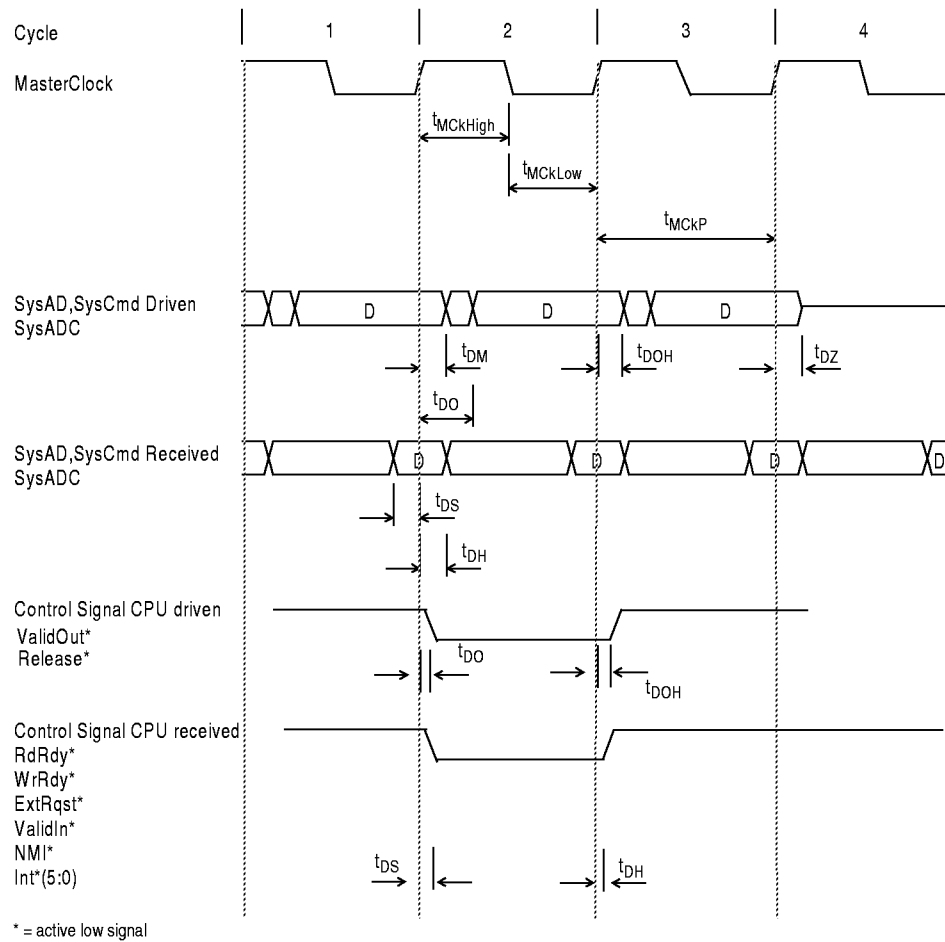


Figure 3 System Clocks Data Setup, Output, and Hold timing

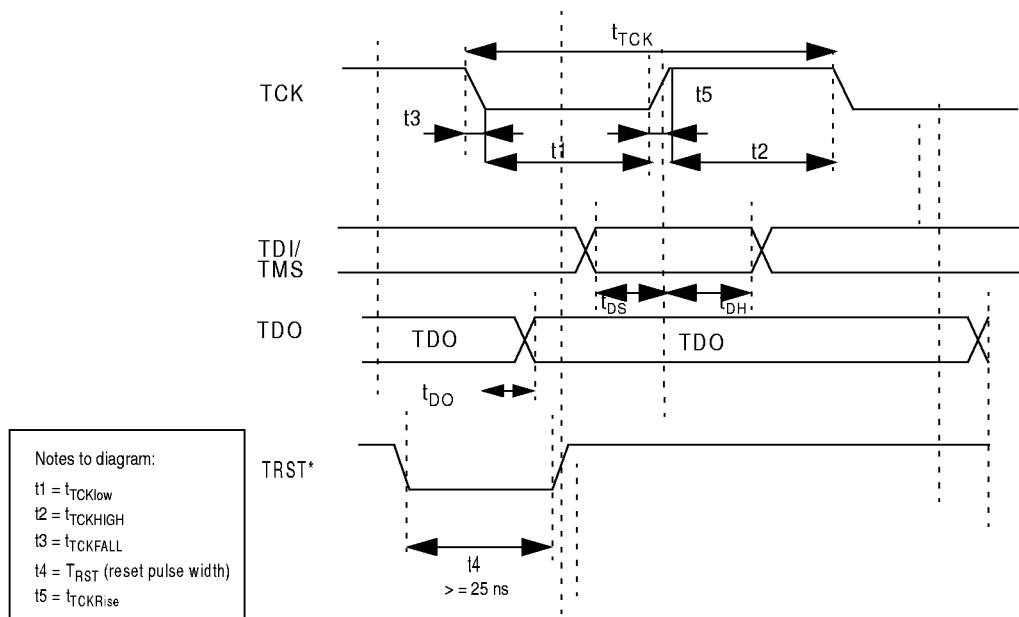


Figure 4 Standard JTAG timing

## AC electrical characteristics

Commercial Temperature Range RC64474/RC64475

( $V_{CC}=3.3V \pm 5\%$ ;  $T_{CASE} = 0^{\circ}C$  to  $+85^{\circ}C$ )

### Clock Parameters

| Parameter <sup>1</sup>       | Symbol                | Test Conditions  | RC64474/<br>RC64475<br>180MHz |                          | RC64474/<br>RC64475<br>200MHz |                          | RC64474/<br>RC64475<br>250MHz |                          | Units |
|------------------------------|-----------------------|------------------|-------------------------------|--------------------------|-------------------------------|--------------------------|-------------------------------|--------------------------|-------|
|                              |                       |                  | Min                           | Max                      | Min                           | Max                      | Min                           | Max                      |       |
| Pipeline clock Frequency     | PClk                  |                  | 80                            | 180                      | 80                            | 200                      | 80                            | 250                      | MHz   |
| MasterClock HIGH             | t <sub>MCHIGH</sub>   | Transition ≤ 3ns | 3                             | —                        | 3                             | —                        | 2.5                           | —                        | ns    |
| MasterClock LOW              | t <sub>MLOW</sub>     | Transition ≤ 3ns | 3                             | —                        | 3                             | —                        | 2.5                           | —                        | ns    |
| MasterClock Frequency        | —                     | —                | 10                            | 90                       | 10                            | 100                      | 10                            | 125                      | MHz   |
| MasterClock Period           | t <sub>MCP</sub>      | —                | 11.1                          | 100                      | 10                            | 100                      | 8                             | 100                      | ns    |
| Clock Jitter for MasterClock | t <sub>JitterIn</sub> | —                | —                             | ±250                     | —                             | ±250                     | —                             | ±250                     | ps    |
| MasterClock Rise Time        | t <sub>MCRise</sub>   | —                | —                             | 2.5                      | —                             | 2                        | —                             | 2                        | ns    |
| MasterClock Fall Time        | t <sub>MCFall</sub>   | —                | —                             | 2.5                      | —                             | 2                        | —                             | 2                        | ns    |
| ModeClock Period             | t <sub>ModeCKP</sub>  | —                | —                             | 256*<br>t <sub>MCP</sub> | —                             | 256*<br>t <sub>MCP</sub> | —                             | 256*<br>t <sub>MCP</sub> | ns    |
| JTAG Clock Input             | t <sub>TCK</sub>      | —                | 100                           | —                        | 100                           | —                        | 100                           | —                        | ns    |
| JTAG Clock HIGH              | t <sub>TCKHIGH</sub>  | —                | 40                            | —                        | 40                            | —                        | 40                            | —                        | ns    |
| JTAG Clock Low               | t <sub>TCKLOW</sub>   | —                | 40                            | —                        | 40                            | —                        | 40                            | —                        | ns    |
| JTAG Clock Rise Time         | t <sub>TCKRise</sub>  | —                | —                             | 5                        | —                             | 5                        | —                             | 5                        | ns    |
| JTAG Clock Fall Time         | t <sub>TCKFall</sub>  | —                | —                             | 5                        | —                             | 5                        | —                             | 5                        | ns    |

<sup>1</sup>. Timings are measured from 1.5V of the clock to 1.5V of the signal.

### Capacitive load deration—RC64474/RC64475

| Parameter   | Symbol          | Test Conditions | 180MHz |     | 200MHz† |     | 250MHz† |     | Units   |
|-------------|-----------------|-----------------|--------|-----|---------|-----|---------|-----|---------|
|             |                 |                 | Min    | Max | Min     | Max | Min     | Max |         |
| Load Derate | C <sub>LD</sub> | —               | —      | 2   | —       | 2   | —       | 2   | ns/25pF |

**System interface parameters**

**Note:** Operation of the RC64474/RC64475 is only guaranteed with the Phase Lock Loop enabled.

| Parameter <sup>1</sup>   | Symbol                                         | Test Conditions                       | RC64474/<br>RC64475<br>180MHz |     | RC64474/<br>RC64475<br>200MHz |     | RC64474/<br>RC64475<br>250MHz |     | Units |
|--------------------------|------------------------------------------------|---------------------------------------|-------------------------------|-----|-------------------------------|-----|-------------------------------|-----|-------|
|                          |                                                |                                       | Min                           | Max | Min                           | Max | Min                           | Max |       |
| Data Output <sup>2</sup> | $t_{DM} = \text{Min}$<br>$t_{DO} = \text{Max}$ | mode <sub>14..13</sub> = 10 (fastest) | 1.0 <sup>3</sup>              | 6   | 1.0 <sup>3</sup>              | 5   | 1.0 <sup>3</sup>              | 4.7 | ns    |
|                          |                                                | mode <sub>14..13</sub> = 01 (slowest) | —                             | 9   | —                             | 9   | —                             | 7   | ns    |
| Data Output Hold         | $t_{DOH}$ <sup>4</sup>                         | mode <sub>14..13</sub> = 10 (fastest) | 1.0 <sup>3</sup>              | —   | 1.0 <sup>3</sup>              | —   | 1.0 <sup>3</sup>              | —   | ns    |
| Data Setup               | $t_{DS}$                                       | $t_{rise} = 5\text{ns}$               | 2                             | —   | 2                             | —   | 2                             | —   | ns    |
| Data Hold                | $t_{DH}$                                       | $t_{fall} = 5\text{ns}$               | 1.0                           | —   | 1.0                           | —   | 1.0                           | —   | ns    |

<sup>1</sup> Timings are measured from 1.5V of the clock to 1.5V of the signal.

<sup>2</sup> Capacitive load for all output timings is 50pF.

<sup>3</sup> Guaranteed by design.

<sup>4</sup> 50pf loading on external output signals, fastest settings. Also applies to JTAG signals (TRST\*,TDO,TDI,TMS)

**Boot-Time interface parameters**

| Parameter       | Symbol   | RC64474/<br>RC64475<br>180 MHz |     | RC64474/<br>RC64475<br>200 MHz |     | RC64474/<br>RC64475<br>250MHz |     | Units              |
|-----------------|----------|--------------------------------|-----|--------------------------------|-----|-------------------------------|-----|--------------------|
|                 |          | Min                            | Max | Min                            | Max | Min                           | Max |                    |
| Mode Data Setup | $t_{DS}$ | 3                              | —   | 3                              | —   | 3                             | —   | Master Clock Cycle |
| Mode Data Hold  | $t_{DH}$ | 0                              | —   | 0                              | —   | 0                             | —   | Master Clock Cycle |

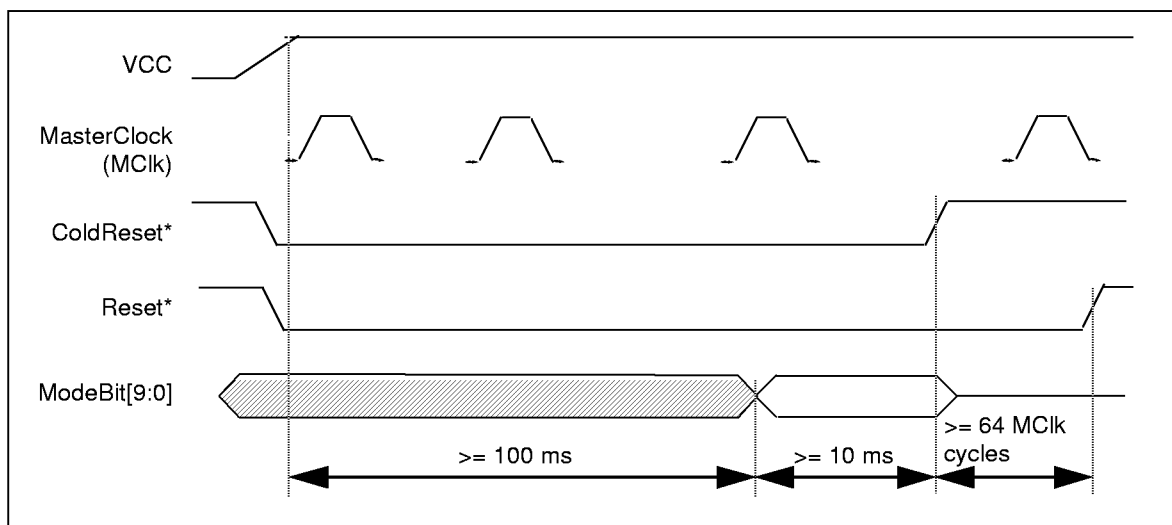
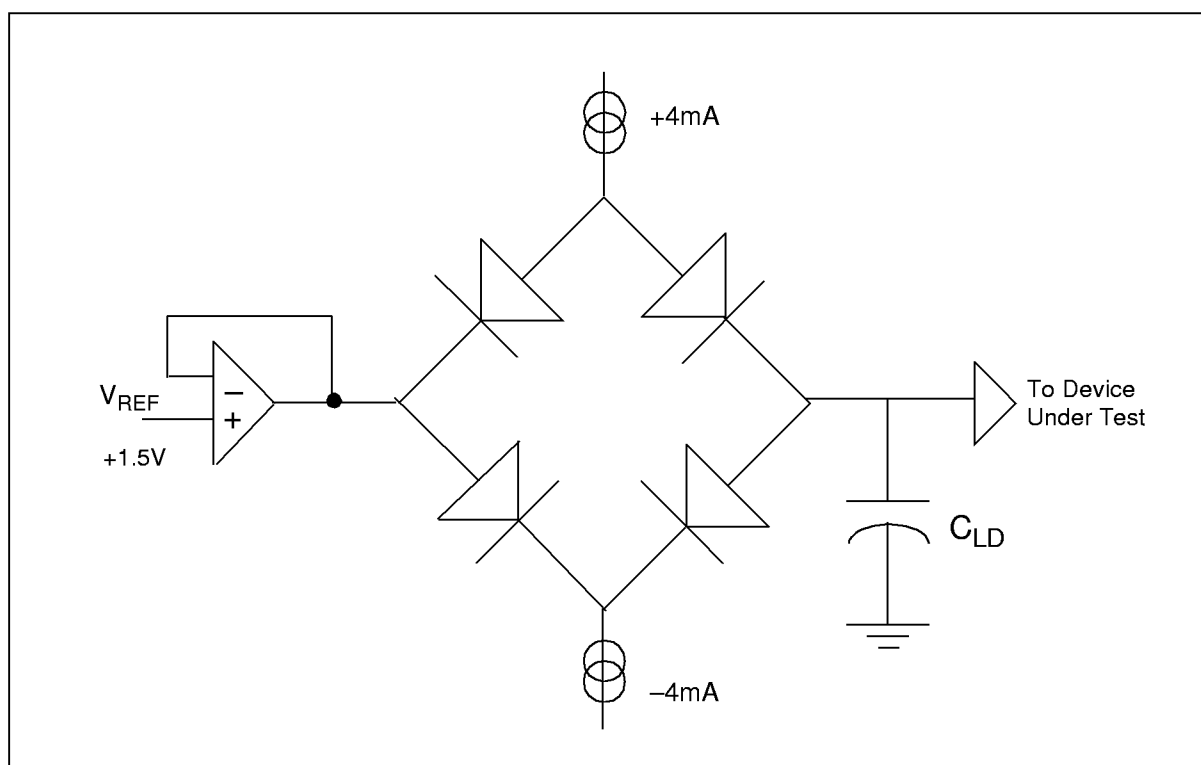
**Mode configuration interface reset sequence**

Figure 5 Mode Configuration Interface Reset Sequence

**Output loading for AC testing**

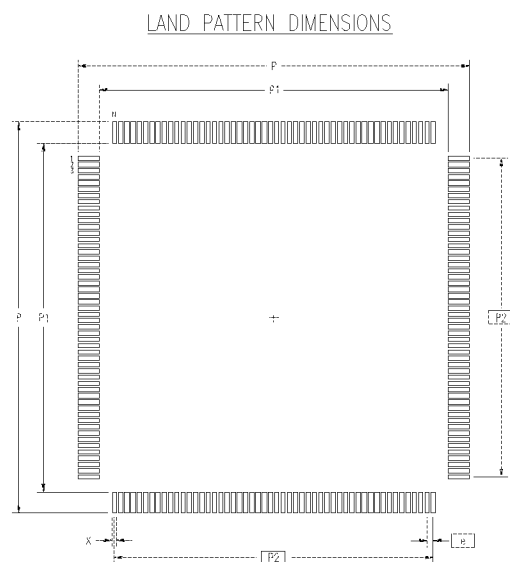
| Signal      | Cld   |
|-------------|-------|
| All Signals | 50 pF |



| S<br>M<br>B<br>D<br>L | JEDEC VARIATION |           |      | N<br>O<br>T<br>E |
|-----------------------|-----------------|-----------|------|------------------|
|                       | FA-1            |           |      |                  |
|                       | MIN             | NOM       | MAX  |                  |
| A                     | --              | --        | 4.13 |                  |
| A1                    | .25             | --        | --   |                  |
| A2                    | 3.26            | 3.43      | 3.60 |                  |
| D                     |                 | 39.60 BSC |      | 4                |
| D1                    |                 | 28.00 BSC |      | 5.2              |
| E                     |                 | 39.60 BSC |      | 4                |
| E1                    |                 | 28.00 BSC |      | 5.2              |
| H                     |                 | 21.00 REF |      |                  |
| N                     |                 | .208      |      |                  |
| e                     |                 | .50 BSC   |      |                  |
| b                     | .17             | --        | .27  | 7                |
| b1                    | .17             | .26       | .23  |                  |
| ddd                   | --              | --        | .08  |                  |

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

- TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
- DATUMS  $\overline{A-B}$  AND  $\overline{D-E}$  TO BE DETERMINED AT DATUM PLANE  $\overline{C-H}$
- DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE  $\overline{C-G}$
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OR THE FOOT.
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS CARRIER CONFORMS TO JEDEC PUBLICATION 65 REGISTRATION MO-143, VARIATION: FA-1



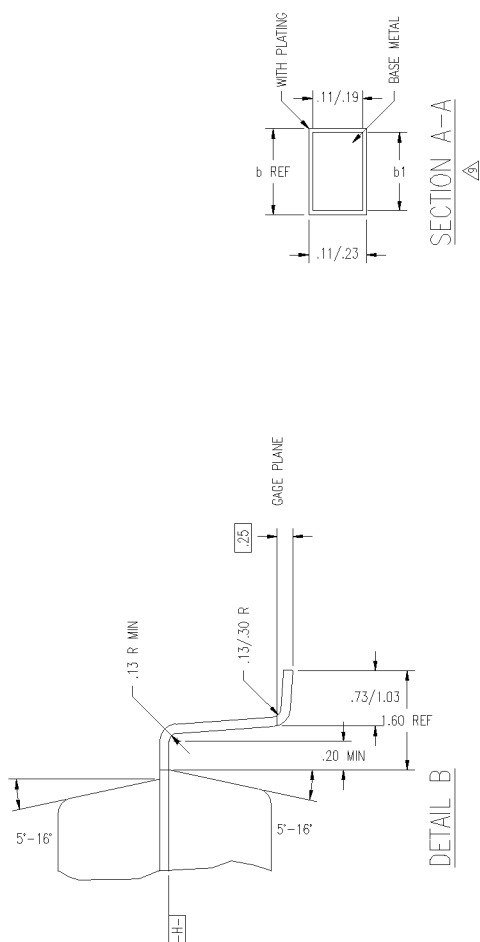
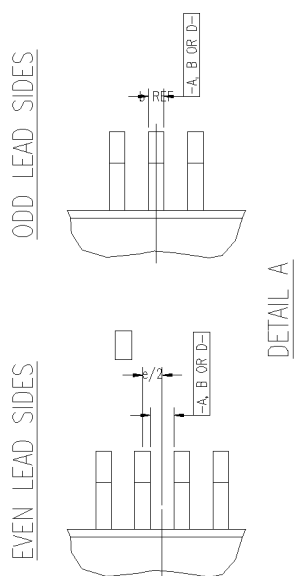
|    | MIN   | MAX   |
|----|-------|-------|
| P  | 31.20 | 31.40 |
| P1 | 27.80 | 28.60 |
| P2 | 25.50 | BSC   |
| X  | .30   | .40   |
| e  | .50   | BSC   |
| N  | 200   |       |

|                                 |                                                                                       |                                                                                                                                         |           |
|---------------------------------|---------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----------|
| TELEPHONE NO.<br>1-800-368-5821 |  | Integrating Device Technology, Inc.<br>2992 Sunny Way, Santa Clara, CA 95050<br>1990S 1990 227-274<br>FAX 1990 860-896 Doc 260-330-2670 |           |
| FACSIMILE NO.<br>227-274        |                                                                                       |                                                                                                                                         |           |
| DATE<br>10/20/90                | TYPE<br>DP PACKAGE OUTLINE<br>28.0 X 28.0 X 3.4 mm PQFP<br>1.30/.25 MIN FORM          |                                                                                                                                         |           |
| QUANTITY<br>10000               | DATE<br>10/20/90                                                                      | PRICE<br>\$3.400000                                                                                                                     | NEW<br>00 |
| C<br>10000 28.00 1.30/0.25      |                                                                                       | PSC-4069 00                                                                                                                             |           |

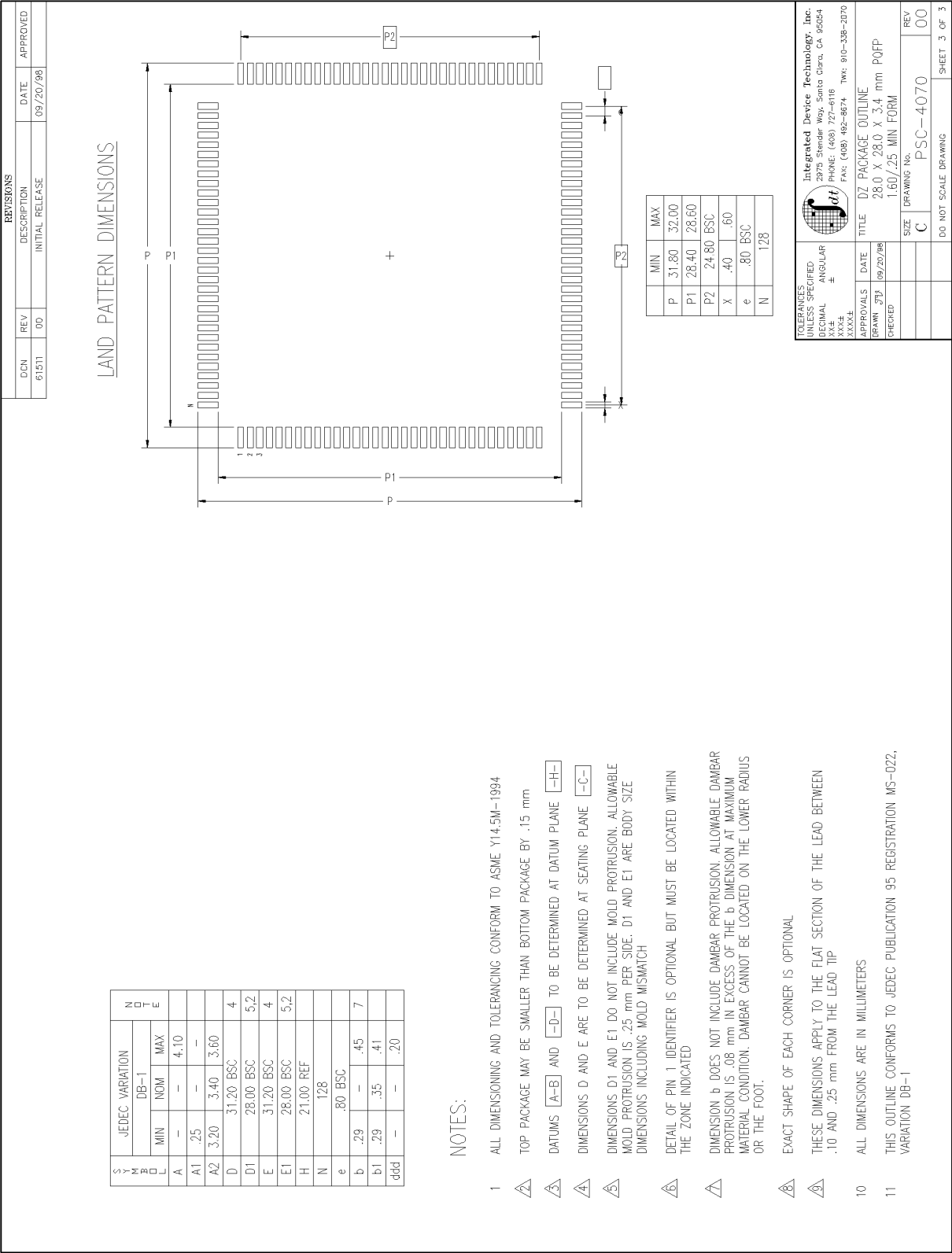




| REVISIONS |     |                 |          |
|-----------|-----|-----------------|----------|
| DCN       | REV | DESCRIPTION     | DATE     |
| 61511     | 00  | INITIAL RELEASE | 09/20/98 |



|                                                                                               |  |                                       |                                                                                                                                                                                                                                                                                 |                                                                                    |                                                           |              |
|-----------------------------------------------------------------------------------------------|--|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----------------------------------------------------------|--------------|
| TOLERANCES UNLESS SPECIFIED<br>FRACTIONAL DECIMAL ANGULAR<br>±<br>XXX.XX ± .01<br>XXXX ± .005 |  | DATE<br>DRAWN 279 09/20/86<br>CHECKED |  <p><b>Integrated Device Technology, Inc.</b><br/>         2737 Stender Way, Santa Clara, CA 95054<br/>         PHONE: (408) 727-4116<br/>         FAX: (408) 482-8674 TWR: 910-338-2070</p> | <b>TITLE</b><br>DZ PACKAGE OUTLINE<br>28.0 X 28.0 X 3.4 mm PQFP<br>1.60mm MIN FORM | <b>SIZE</b><br>DRAWING NO.<br><b>C</b> PSC-4070<br>REV 00 | SHEET 2 OF 3 |
|-----------------------------------------------------------------------------------------------|--|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|-----------------------------------------------------------|--------------|



## Ordering information

| IDT79RCXX    | YY                | XXXX        | 999               | A        | A                   |                                                 |
|--------------|-------------------|-------------|-------------------|----------|---------------------|-------------------------------------------------|
| Product Type | Operating Voltage | Device Type | Speed             | Package  | Temp range/ Process |                                                 |
|              |                   |             |                   |          | Blank               | Commercial Temperature<br>(0°C to +85°C Case)   |
|              |                   |             |                   |          | I                   | Industrial Temperature<br>(-40°C to +85°C Case) |
|              |                   |             |                   | DZ<br>DP |                     | 128-pin QFP<br>208-pin QFP                      |
|              |                   |             | 180<br>200<br>250 |          |                     | 180 MHz PClk<br>200 MHz PClk<br>250 MHz PClk    |
|              |                   | 474<br>475  |                   |          |                     | Embedded Processor                              |
|              | V                 |             |                   |          |                     | 3.3V +/-5%                                      |
|              |                   | 79RC64      |                   |          |                     | 64-bit Embedded<br>Microprocessor               |

### Valid combinations

|                                   |                                             |
|-----------------------------------|---------------------------------------------|
| IDT79RC64V474 - 180, 200, 250 DZ  | 128-pin QFP package, Commercial Temperature |
| IDT79RC64V475 - 180, 200, 250 DP  | 208-pin QFP package, Commercial Temperature |
| IDT79RC64V474 - 180, 200, 250 DZI | 128-pin QFP package, Industrial Temperature |
| IDT79RC64V475 - 180, 200, 250 DPI | 208-pin QFP package, Industrial Temperature |



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