Integrated Device Technology, Inc.

8K x 8
16K x 8
CMOS DUAL-PORT STATIC RAM MODULE (SLAVE)

IDT7M144S
IDT7M145S

FEATURES:

- High-density 64K/128K CMOS SLAVE Dual-Port static RAM modules
- 16K x 8 (IDT7M145) or 8K x 8 (IDT7M144) option
- Easily expands data bus width to 16-or-more-bits when used with MASTER IDT7M134 or IDT7M135 modules
- Fully asynchronous read/write operation from either port
- Fast access time
  - commercial: 30ns (max.)
  - military: 40ns (max.)
- Low-power consumption
- $\overline{BUSY}$ output flags
- Dual Vcc and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply

DESCRIPTION:

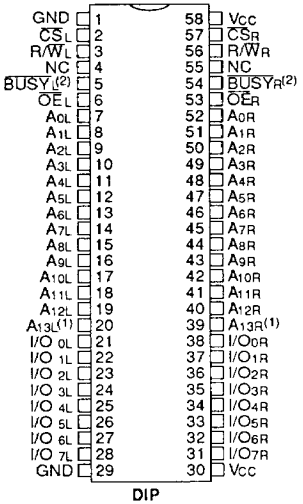
The IDT7M144/IDT7M145 are 64K/128K high-speed CEMOS™ SLAVE Dual-Port static RAM modules constructed on a multi-layered, co-fired, ceramic substrate using four IDT7142 2K x 8 SLAVE dual-port static RAMs (IDT7M144) or eight IDT7142 SLAVE dual-port static RAMs (IDT7M145) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/IDT74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port static RAMs. (On IDT7M144 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port static RAMs).

The IDT7M144/IDT7M145 are designed as "SLAVE" dual-port static RAM modules to be used together with the IDT7M135/IDT7M135 "MASTER" dual-port RAM modules in 16-or-more-bit systems, whereas the IDT7M134/IDT7M135 are designed to be used as stand-alone 8-bit dual-port static RAM modules. Using the IDT MASTER/SLAVE dual-port static RAM module approach in 16-or-more-bit memory system applications results in full speed operation without the need for additional discrete logic.

Both SLAVE IDT7M144/IDT7M145 and MASTER IDT7M134/IDT7M135 modules provide two ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive). The $\overline{BUSY}$ pins are outputs on the MASTER and inputs on the SLAVE.

All military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

PIN CONFIGURATION (3)



DIP
TOP VIEW

2687 dwg 01

PIN NAMES

Left Port	Right Port	Names
A_{0L}-A_{13L}	A_{0R}-A_{13R}	Address Input
I/O_{0L}-IO_{7L}	I/O_{0R}-I/O_{7R}	Data Input/Output
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{BUSY}$ Input
Vcc	Vcc	Power
GND	GND	Ground

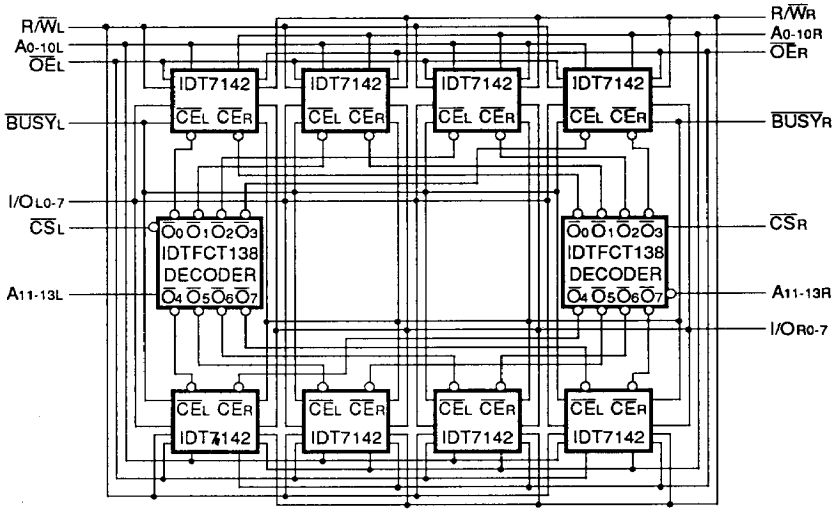
NOTES:
1. On 8K x 8 IDT7M144 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
2. IDT7M134/IDT7M135 (MASTER): $\overline{BUSY}$ is open drain output and requires pull up resistor. IDT7M144/IDT7M145 (SLAVE): $\overline{BUSY}$ is input.
3. For module dimensions, please refer to module drawing M12 in the packaging section.

8

CEMOS is a trademark of Integrated Device Technology, Inc.

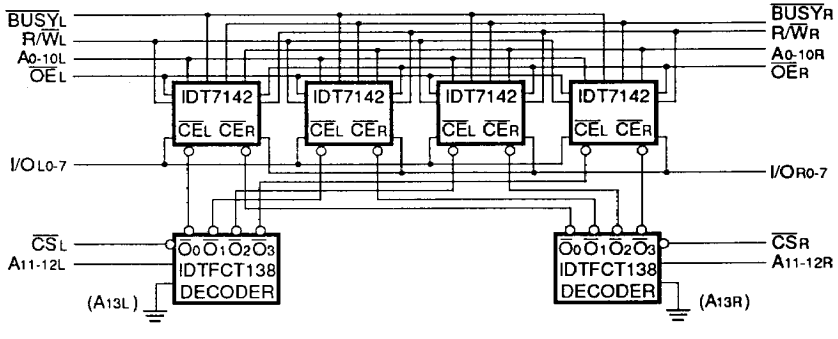
FUNCTIONAL BLOCK DIAGRAMS

IDT7M145 (16K x 8)



2687 dwg 02

IDT7M144 (8K x 8)



2687 dwg 03

(GROUND A_{13L} AND A_{13R} EXTERNALLY)

DC ELECTRICAL CHARACTERISTICS
OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(DC electricals for the IDT7M144/IDT7M145 SLAVE module are identical to the IDT7M134/IDT7M135 MASTER module. Reference the IDT7M134/IDT7M135 CMOS Dual-Port static RAM data sheet.)

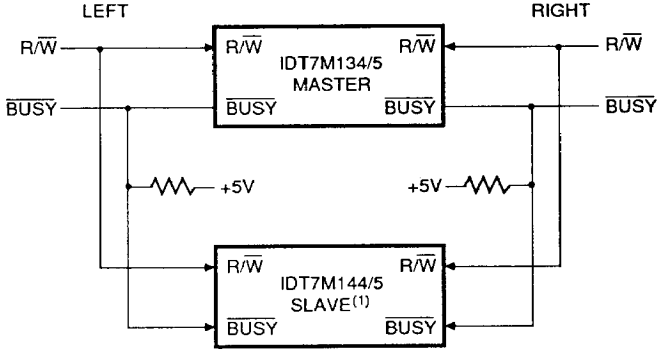
AC ELECTRICAL CHARACTERISTICS
OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(AC electricals for the IDT7M144/IDT7M145 SLAVE module are identical to the IDT7M134/IDT7M135 MASTER module except where noted below.)

Symbol	Parameter	IDTM144S30 IDTM145S30 (Com'l. Only) Min.	Max.	IDTM144S35 IDTM145S35 (Com'l. Only) Min.	Max.	IDTM144S40 IDTM145S40 Min.	Max.	IDTM144S45 IDTM145S45 Min.	Max.	Unit
t_{WB}	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$	20	—	20	—	20	—	20	—	ns

Symbol	Parameter	IDTM144S50 IDTM145S50 Min.	Max.	IDTM144S60 IDTM145S60 Min.	Max.	IDTM144S70 IDTM145S70 (Mil. Only) Min.	Max.	IDTM144S90 IDTM145S90 (Mil. Only) Min.	Max.	IDTM144S100 IDTM145S100 (Mil. Only) Min.	Max.	Unit
t_{WB}	Write to $\overline{BUSY}$	0	—	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$	20	—	20	—	20	—	20	—	20	—	ns

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEM



2687 dwg 04

NOTE:
1. No arbitration in IDT7M144/IDT7M145 (SLAVE): $\overline{BUSY}$ in inhibits write in IDT7M144/IDT7M145.

8

ORDERING INFORMATION