Integrated Device Technology, Inc.

SUBSYSTEMS FLEXI-PAK™ FAMILY
32K x 32
128K x 32
CMOS STATIC RAM MODULES

IDT7M4003
IDT7M4013

T-46-23-14

FEATURES:

- High-density 1 megabit/4 megabit CEMOS™ static RAM modules
- Member of the Subsystems "Flexi-Pak" Family of inter-changeable modules, with equivalent pin-outs, supporting a wide range of applications
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
  - 7M4003 - 15ns (max.) commercial
  - 7M4003 - 20ns (max.) military
  - 7M4013 - 15ns (max.) commercial
  - 7M4013 - 20ns (max.) military
- Low power CMOS operation
- Surface mounted LCC or SO components on a multi-layered co-fired ceramic substrate
- Offered in a 66-pin "PGA-type" HIP (Hex In-line Package), occupying only 1 sq. inch of board space
- Single 5V (±10%) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7M4003/4013 are high-speed, high-density 1megabit/4 megabit CMOS static RAM modules constructed on a multi-layer co-fired ceramic substrate using either 32K x 8 or 128K x 8 SRAM components.

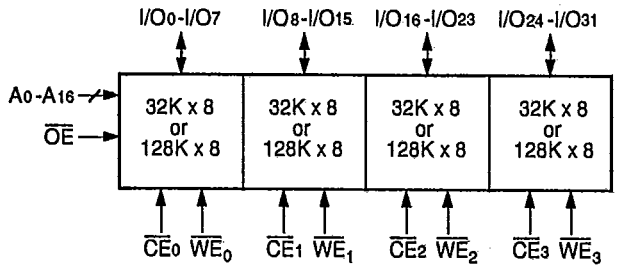
These modules are part of the IDT Subsytems "Flexi-Pak" Family. This family of SRAM/EEPROM/EPROM memory modules support applications requiring stand alone static or programmable memory or those applications needing a combination of both. All three module configurations have equivalent pin-outs, making these "plug-in compatible" with each other (i.e. inter-changeable) suitable for a wide range of applications.

The IDT7M4003/4013 is available with access times as fast as 15ns over the commercial temperature range and 20ns over the military temperature range.

This family of IDT modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit 1 megabit/4 megabit of memory into 1 sq. inch of board space.

All IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2711 drw 01

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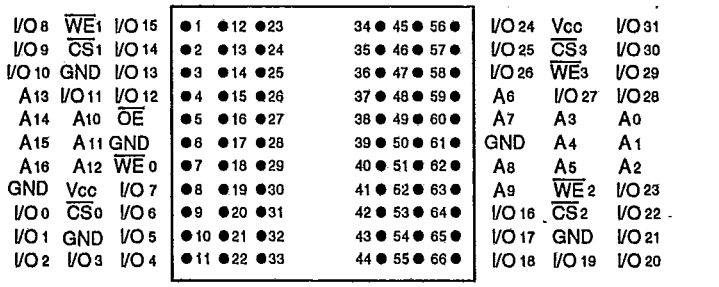
PIN CONFIGURATION[1]



HIP
TOP VIEW

2711 drw 02

NOTE:
1. For the IDT7M4003 (32K x 32) version, pins 6 and 7 are no connects.

PIN NAMES

Name	Description
I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}_{0-3}$	Write Enables
$\overline{CS}_{0-3}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2711 tbl 01

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
$C_{IN(1)}$	Input Capacitance (DATA, $\overline{CS}$, $\overline{WE}$)	V_{IN} = 0V	50	pF
$C_{IN(2)}$	Input Capacitance (ADDRESS, $\overline{OE}$)	V_{IN} = 0V	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2711 tbl 02
1. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Read	L	H	H	High Z	Active
Write	L	X	L	$DATA_{IN}$	Active

2711 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2711 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2711 tbl 05
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2711 tbl 06

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.(1)	Max.(2)	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, $\overline{OE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	10	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{CS}$, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	40	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	10	µA
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$ f = f_{MAX}, Output Open	—	800	880	mA
I_{SB}	Standby Supply Curent	V_{CC} = Max., $\overline{CS} \geq V_{IH}$ f = f_{MAX}, Output Open	—	80	280	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} > V_{CC}$ -0.2V or < 0.2V	—	80	80	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA(3)	—	0.4	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA(4)	2.4	—	—	V

2711 tbl 07

NOTES:
1. For TA = 0°C to +70°C versions only.
2. For TA = -55°C to +125°C versions only.
3. I_{OL} = 2mA for 70ns – 100ns versions of the IDT7M4013.
4. I_{OH} = -1mA for 70ns – 100ns versions of the IDT7M4013.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2711 tbl 07

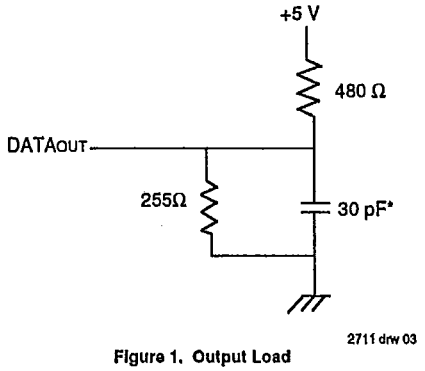

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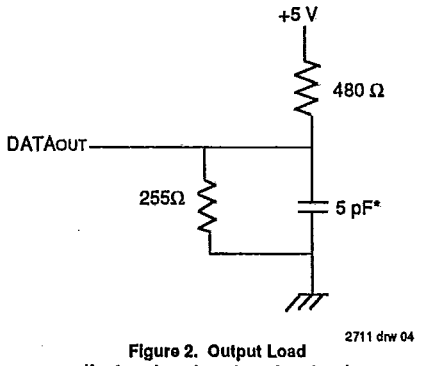
Figure 1. Output Load



2711 drw 04

Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

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AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-15[2]		-17[2]		-20[2]		-25		-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	—	30	ns
tACS	Chip Select Access Time	—	15	—	17	—	20	—	25	—	30	ns
tCLZ[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	12	—	13	—	15	ns
tOLZ[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	2	—	2	—	ns
tCHZ[1]	Chip Deselect to Output in High Z	—	6	—	7	—	8	—	12	—	15	ns
tOHZ[1]	Output Disable to Output In High Z	—	6	—	7	—	7	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
WRITE CYCLE												
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tCW	Chip Select to End of Write	12	—	13	—	15	—	20	—	25	—	ns
tAW	Address Valid to End of Write	12	—	13	—	15	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	13	—	15	—	20	—	23	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ[1]	Write Enable to Ouput In High Z	—	6	—	8	—	9	—	12	—	13	ns
tDW	Data to Write Time Overlap	8	—	8	—	9	—	13	—	15	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	3	—	3	—	ns
tOW[1]	Output Active from End of Write	0	—	0	—	0	—	5	—	5	—	ns

2711 tbl 09

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specification only.

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AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-35		-40		-50		-60 (Mil. Only)		-70 (Mil. Only)		-85 (Mil. Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	35	—	40	—	50	—	60	—	70	—	85	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	25	—	30	—	30	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	2	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	15	—	20	—	20	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	35	—	40	—	50	—	60	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	30	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Set-up Time	0	—	2	—	2	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	40	—	45	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Ouput in High Z	—	17	—	20	—	20	—	25	—	30	—	35	ns
t_{DW}	Data to Write Time Overlap	16	—	16	—	25	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time	3	—	3	—	5	—	5	—	5	—	5	—	ns
t_{OW}[1]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2711 tbl 10

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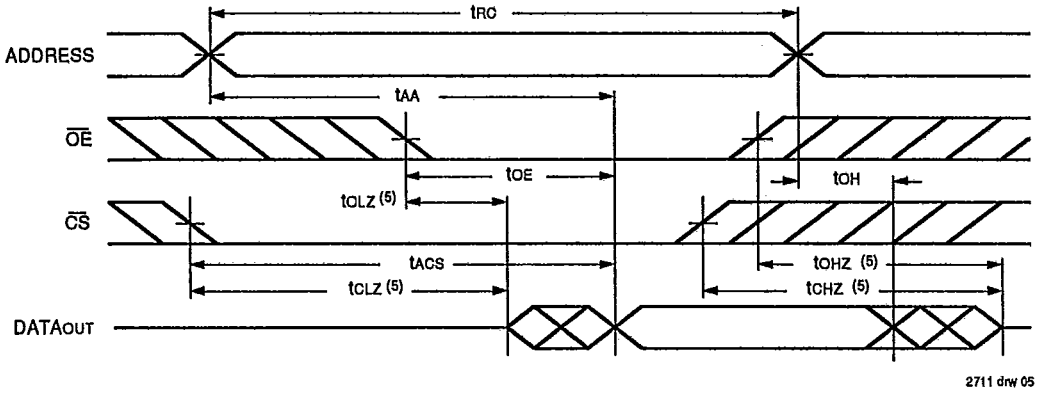
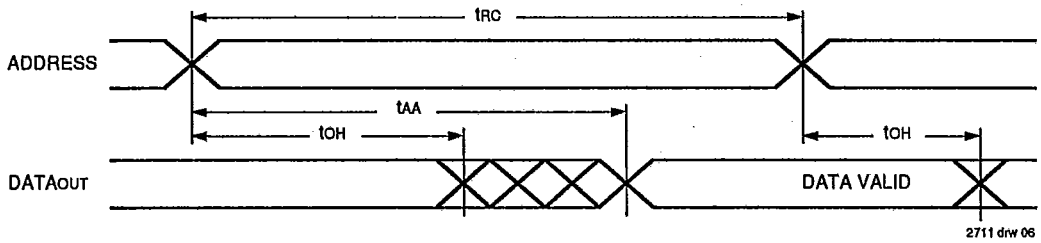
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



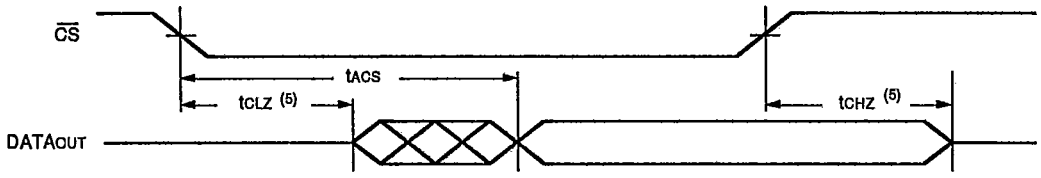
2711 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2711 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2711 drw 07

NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1, 2, 3, 7)

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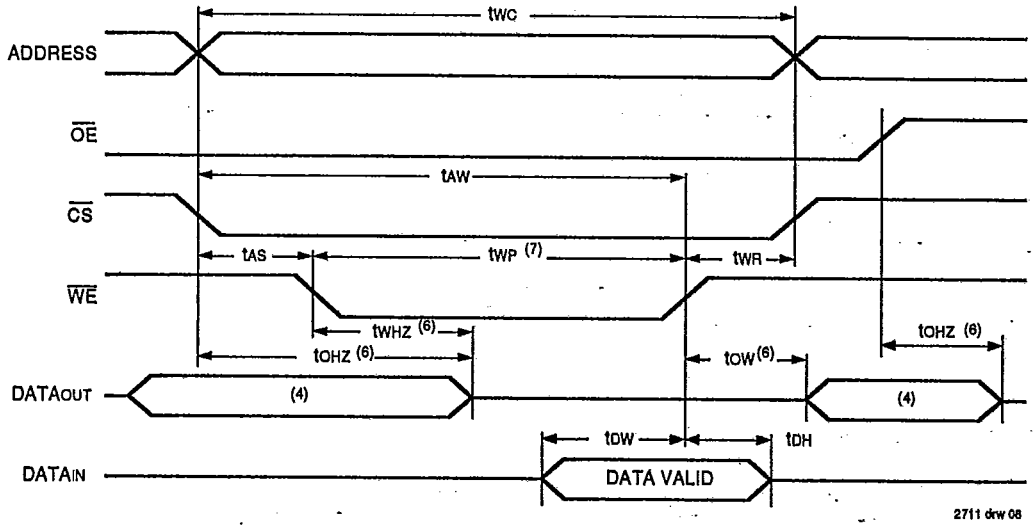
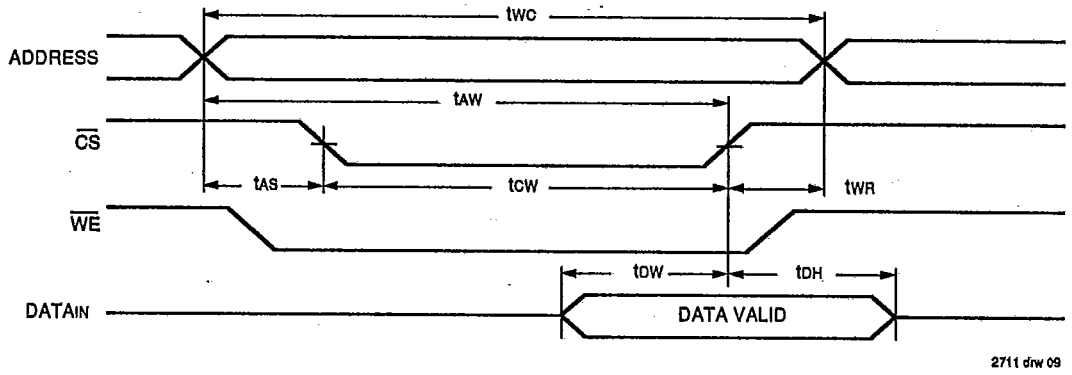


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going High to the end of write cycle.
4. During this period, I/O pins are in the output state, input signals must not be applied.
5. If the $\overline{CS}$ Low transition occurs simultaneously with or after the $\overline{WE}$ Low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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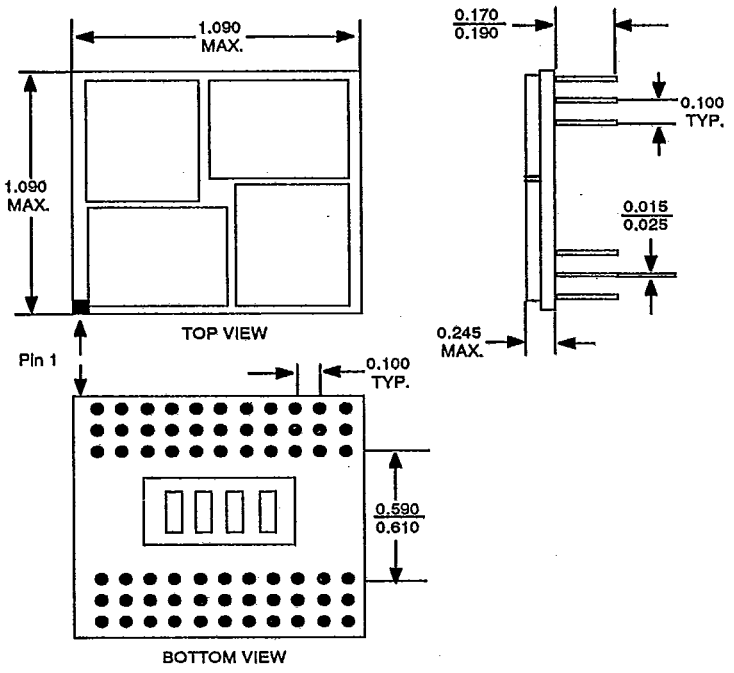
PACKAGE DIMENSIONS

7M4003SxxCHx



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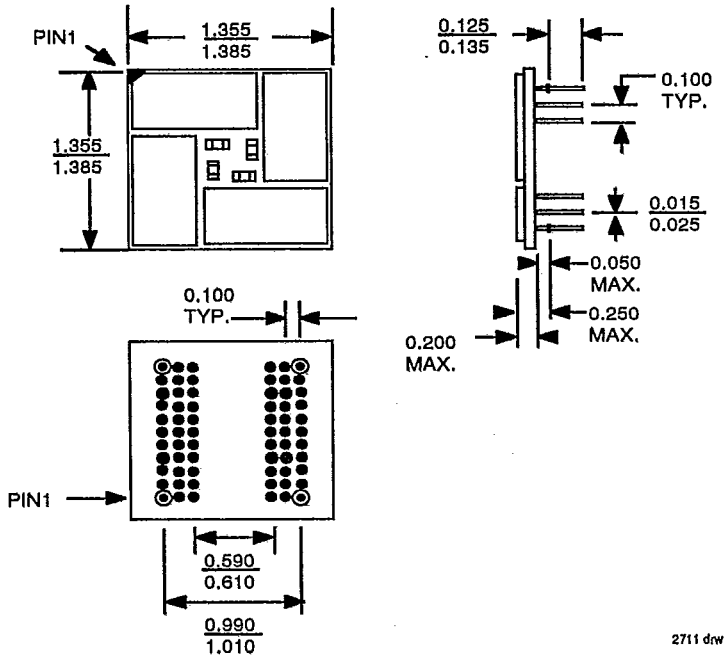
7M4013SxxCHx



2711 drw 11

7M4013SxxNH

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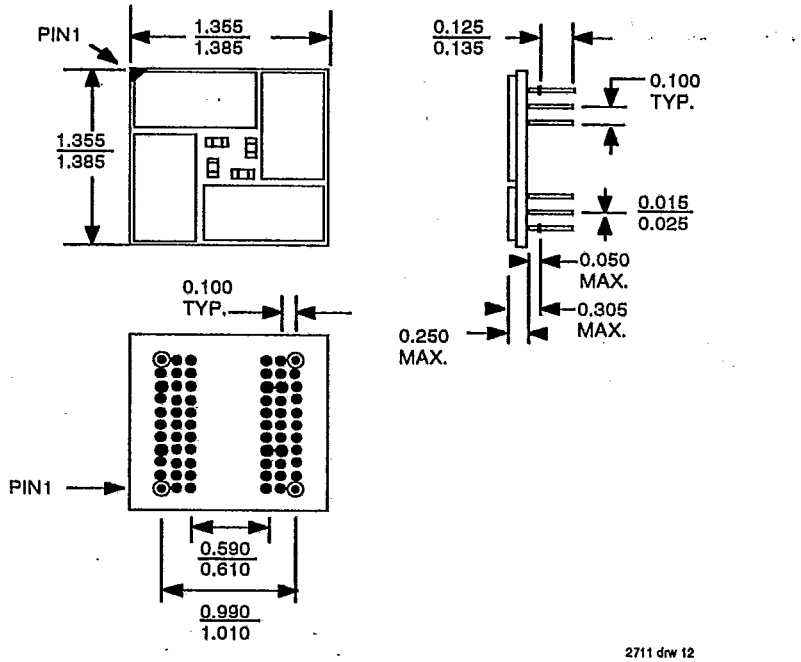

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