



Integrated Device Technology, Inc.

32K x 32
128K x 32
CMOS STATIC RAM MODULES

IDT7M4003
IDT7M4013

FEATURES

- High-density 1Mb/4Mb CMOS Static RAM modules
- Footprint compatible module upgrades to the next higher density with relative ease
- Fast access times:
 - 7M4003 — 30ns (max.) commercial
 - 7M4003 — 30ns (max.) military
 - 7M4013 — 15ns (max.) commercial
 - 7M4013 — 25ns (max.) military
- Low-power CMOS operation
- Surface mounted LCC or SOJ components on a multilayered cofired ceramic substrate
- Offered in a 66-pin "PGA-type" HIP (Hex In-line Package)
- Single 5V ($\pm 10\%$) power supply
- Multiple ground pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION

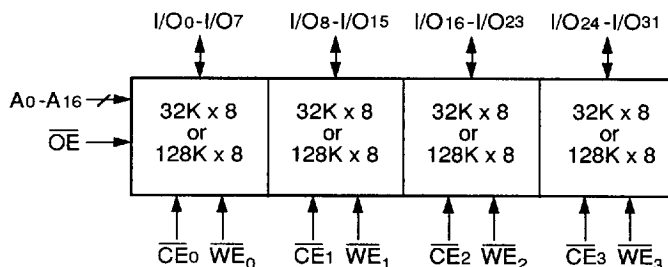
The IDT7M4003/4013 are high-speed, high-density 1Mb/4Mb CMOS Static RAM modules constructed on a multilayer cofired ceramic substrate using either 32K x 8 or 128K x 8 SRAM components.

The IDT7M4003/4013 is available with access times as fast as 15ns over the commercial temperature range and 25ns over the military temperature range.

This family of IDT modules are offered in a 66-pin, ceramic HIP (Hex In-line Package). This HIP package is similar to a PGA and allows the designer to fit 1Mb/4Mb of memory into a minimum amount of board space.

All IDT military modules are assembled with semiconductor components compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2711 drw 01

The IDT logo is a registered trademark and Flexi-Pak is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES
SEPTEMBER 1993

©1993 Integrated Device Technology, Inc.

DSC-7069/4

7.8

1

7

INTEGRATED DEVICE

PIN CONFIGURATION⁽¹⁾

I/O 8 $\overline{WE}$ 1	I/O 15	●1 ●12 ●23	34 ●45 ●56 ●	I/O 24 Vcc	I/O 31
I/O 9 $\overline{CS}$ 1	I/O 14	●2 ●13 ●24	35 ●46 ●57 ●	I/O 25 $\overline{CS}$ 3	I/O 30
I/O 10 GND	I/O 13	●3 ●14 ●25	36 ●47 ●58 ●	I/O 26 $\overline{WE}$ 3	I/O 29
A13 I/O 11	I/O 12	●4 ●15 ●26	37 ●48 ●59 ●	A6 I/O 27	I/O 28
A14 A10	$\overline{OE}$	●5 ●16 ●27	38 ●49 ●60 ●	A7 A3	A0
A15 A11	GND	●6 ●17 ●28	39 ●50 ●61 ●	GND A4	A1
A16 A12	$\overline{WE}$ 0	●7 ●18 ●29	40 ●51 ●62 ●	A8 A5	A2
GND Vcc	I/O 7	●8 ●19 ●30	41 ●52 ●63 ●	A9 $\overline{WE}$ 2	I/O 23
I/O 0 $\overline{CS}$ 0	I/O 6	●9 ●20 ●31	42 ●53 ●64 ●	I/O 16 $\overline{CS}$ 2	I/O 22
I/O 1 GND	I/O 5	●10 ●21 ●32	43 ●54 ●65 ●	I/O 17 GND	I/O 21
I/O 2 I/O 3	I/O 4	●11 ●22 ●33	44 ●55 ●66 ●	I/O 18 I/O 19	I/O 20

HIP
TOP VIEW

2711 drw 02

NOTE:

1. For the IDT7M4003 (32K x 32) version, pins 6 and 7 are no connects

PIN NAMES

Name	Description
I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$ 0-3	Write Enables
$\overline{CS}$ 0-3	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground

2711 tbi 01

CAPACITANCE⁽¹⁾ ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter	Conditions	Max.	Unit
$C_{IN}^{(1)}$	Input Capacitance (DATA, CS, WE)	$V_{IN} = 0V$	12	pF
$C_{IN}^{(2)}$	Input Capacitance (ADDRESS, OE)	$V_{IN} = 0V$	50	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	pF

2711 tbi 02

NOTE:

1. This parameter is guaranteed by design, but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DATA _{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DATA _{IN}	Active

2711 tbi 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2711 tbi 04

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input HIGH Voltage	2.2	—	6.0	V
V _{IL}	Input LOW Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

2711 tbi 05

1. V_{IL} = -3.0V for pulse width less than 20ns

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2711 tbi 06

DC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$ and $0^\circ C$ to $+70^\circ C$)

Symbol	Parameter	Test Conditions	Min.	Max. ⁽¹⁾	Max. ⁽²⁾	Unit
I _{LI}	Input Leakage Current (Address, OE)	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	20	40	μA
I _{LI}	Input Leakage Current (Data, CS, WE)	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	—	5	10	μA
I _{LO}	Output Leakage Current	$V_{CC} = \text{Max.}$ $\overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	—	5	10	μA
I _{CC}	Dynamic Operating Current	$V_{CC} = \text{Max.}, \overline{CS} \leq V_{IL}$ $f = f_{MAX}, \text{Output Open}$	—	720	800	mA
I _{SB}	Standby Supply Current	$V_{CC} = \text{Max.}, \overline{CS} \geq V_{IH}$ $f = f_{MAX}, \text{Output Open}$	—	160	240	mA
I _{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} > V_{CC} - 0.2V$ or $< 0.2V$	—	60	80	mA
V _{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8mA$	—	0.4	0.4	V
V _{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4mA$	2.4	—	—	V

NOTES:

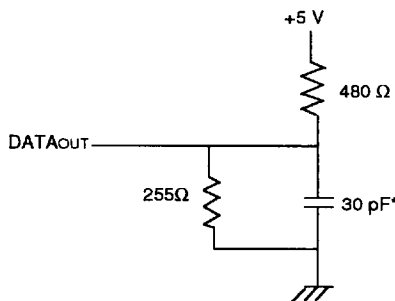
- 1 For $T_A = 0^\circ C$ to $+70^\circ C$ versions only
- 2 For $T_A = -55^\circ C$ to $+125^\circ C$ versions only

2711 tbi 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

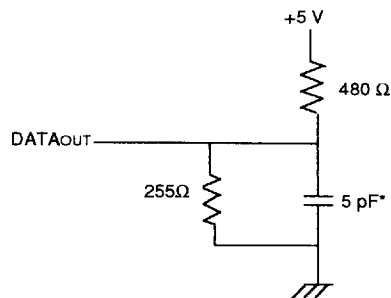
2711 tbi 07



2711 drw 03

*Including scope and jig

Figure 1. Output Load



2711 drw 04

*Including scope and jig

Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

AC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-15 ⁽²⁾		-17 ⁽²⁾		-20 ⁽²⁾		-25		-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	—	30	ns
tACS	Chip Select Access Time	—	15	—	17	—	20	—	25	—	30	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	12	—	13	—	15	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	2	—	2	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	—	6	—	7	—	8	—	12	—	15	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	—	6	—	7	—	7	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
WRITE CYCLE												
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	30	—	ns
tCW	Chip Select to End-of-Write	12	—	13	—	15	—	20	—	25	—	ns
tAW	Address Valid to End-of-Write	12	—	13	—	15	—	20	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	13	—	15	—	20	—	23	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Ouput in High-Z	—	6	—	8	—	9	—	12	—	13	ns
tDW	Data to Write Time Overlap	8	—	8	—	9	—	13	—	15	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	3	—	3	—	ns
tOW ⁽¹⁾	Output Active from End-of-Write	0	—	0	—	0	—	5	—	5	—	ns

NOTES:

1. This parameter is guaranteed by design, but not tested
2. Preliminary specification only.

2711 tbi 09

AC ELECTRICAL CHARACTERISTICS

68E D 4825771 0014460 635 IDT

INTEGRATED DEVICE

(Vcc = 5.0V ± 10%, TA = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameters	-35		-40		-50		-60		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	35	—	40	—	50	—	60	—	ns
tAA	Address Access Time	—	35	—	40	—	50	—	60	ns
tACS	Chip Select Access Time	—	35	—	40	—	50	—	60	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	20	—	25	—	30	—	30	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	2	—	5	—	5	—	5	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	—	17	—	20	—	20	—	25	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	—	15	—	20	—	20	—	25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
WRITE CYCLE										
tWC	Write Cycle Time	35	—	40	—	50	—	60	—	ns
tCW	Chip Select to End-of-Write	30	—	35	—	45	—	55	—	ns
tAW	Address Valid to End-of-Write	30	—	35	—	45	—	55	—	ns
tAS	Address Set-up Time	0	—	2	—	2	—	5	—	ns
tWP	Write Pulse Width	25	—	30	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	—	17	—	20	—	20	—	25	ns
tDW	Data to Write Time Overlap	16	—	16	—	25	—	30	—	ns
tDH	Data Hold from Write Time	3	—	3	—	5	—	5	—	ns
tOW ⁽¹⁾	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

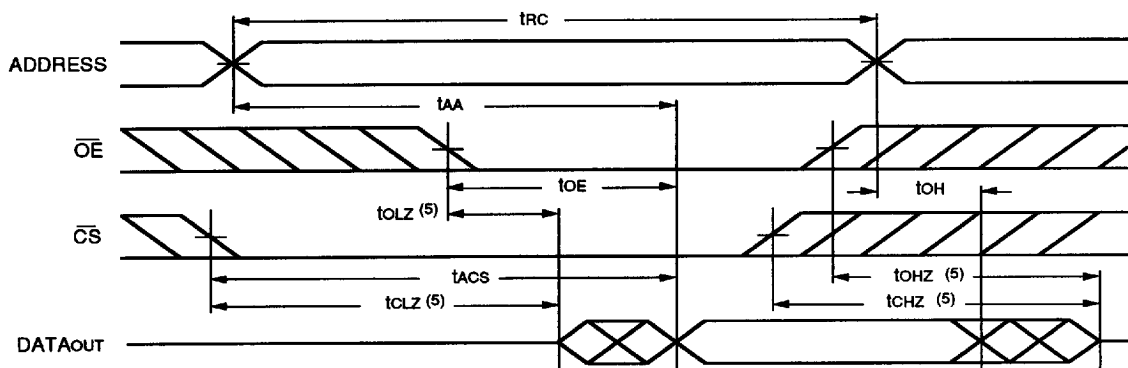
NOTE:

1 This parameter is guaranteed by design, but not tested

2711 tbl 10

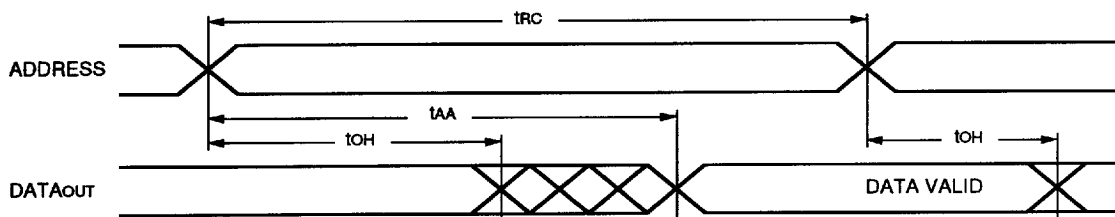
TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾

INTEGRATED DEVICE



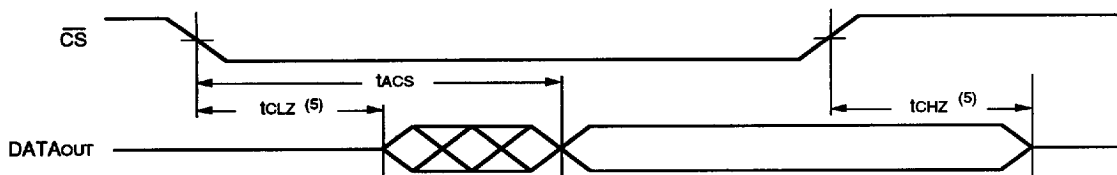
2711 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



2711 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)

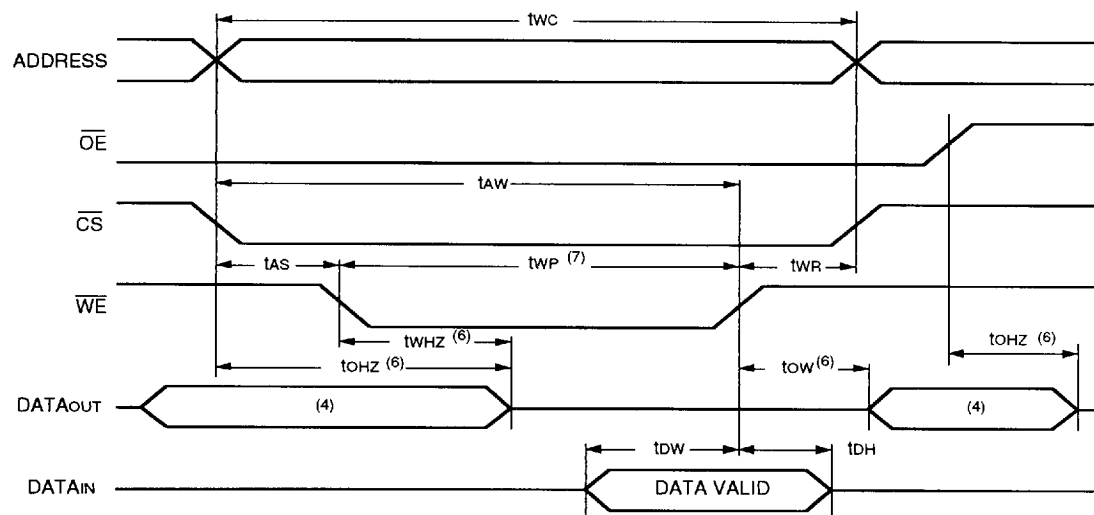


2711 drw 07

NOTES:

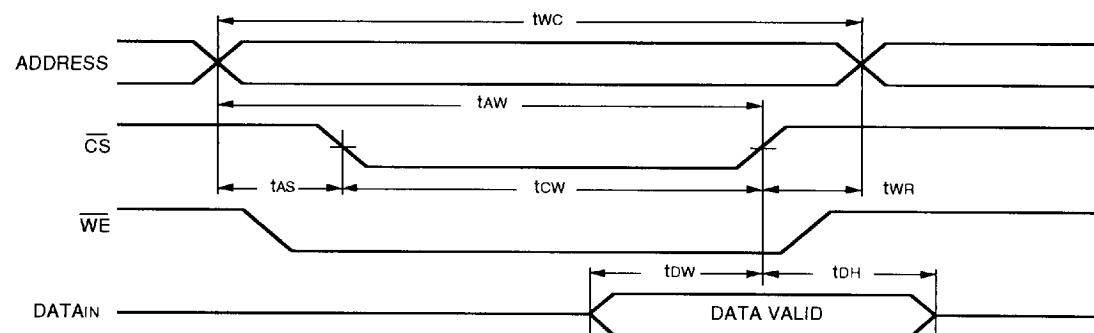
1. WE is HIGH for Read Cycle.
2. Device is continuously selected, CS = V_L.
3. Address valid prior to or coincident with CS transition LOW.
4. OE = V_L.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)^(1, 2, 3, 7)



2711 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)^(1, 2, 3, 5)



2711 drw 09

NOTES:

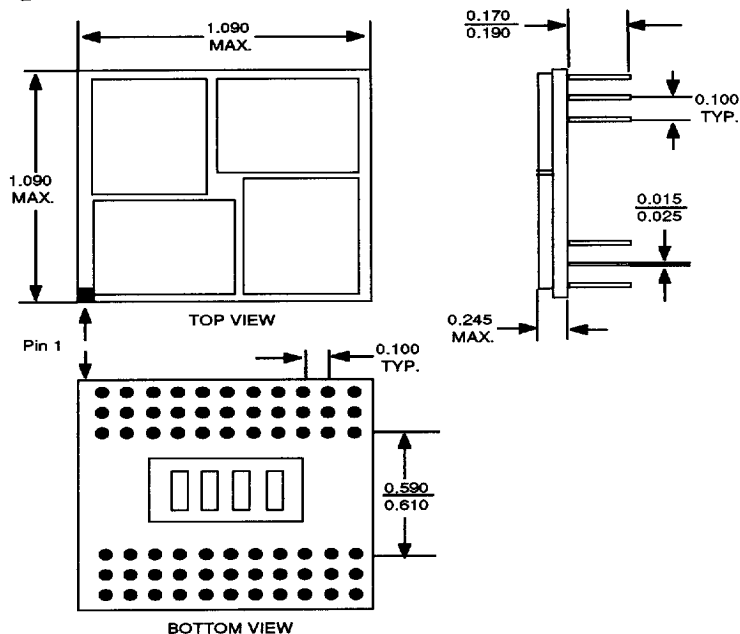
- 1 $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions
- 2 A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$
- 3 tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle
- 4 During this period, I/O pins are in the output state, input signals must not be applied
- 5 If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state
- 6 Transition is measured $\pm 200\text{mV}$ from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested
- 7 If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tOW) to allow the I/O drivers to turn off data and to be placed on the bus for the required tOW. If $\overline{OE}$ is HIGH during an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

68E D 4825771 0014463 344 IDT

PACKAGE DIMENSIONS

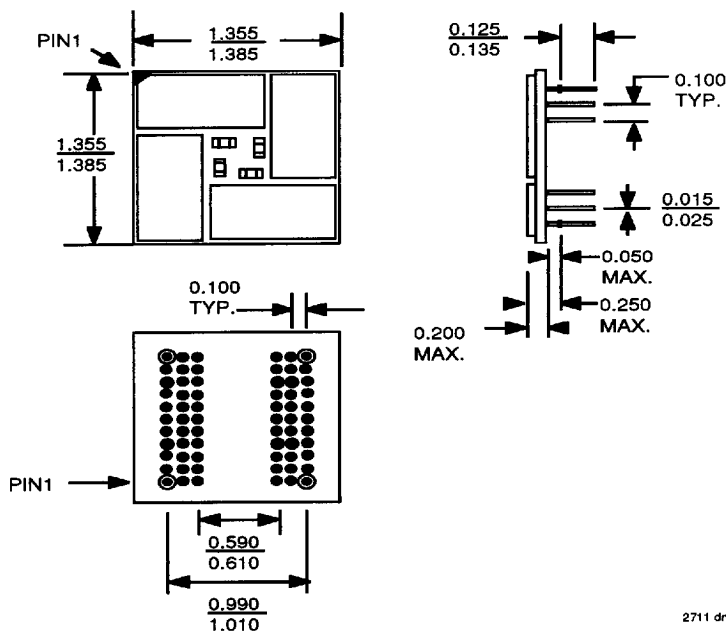
7M4003SxxCHx

INTEGRATED DEVICE



2711 drw 10

7M4013SxxCHx

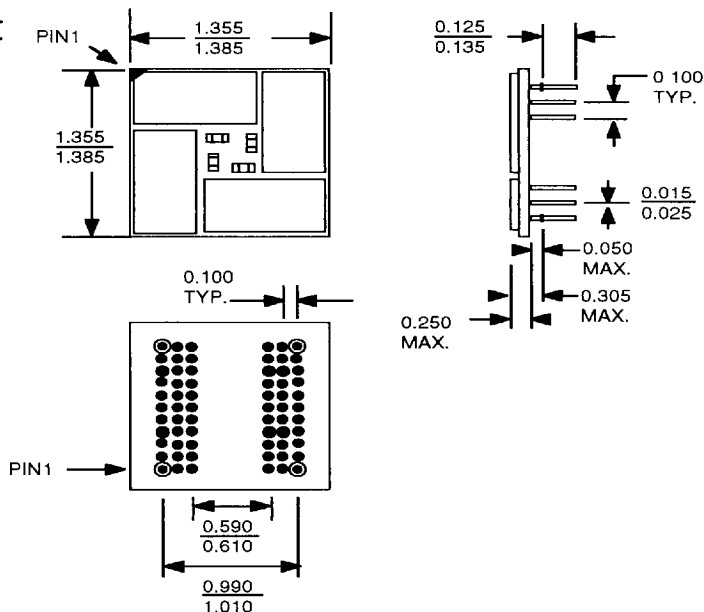


2711 drw 11

7M4013SxxNH

INTEGRATED DEVICE

68E D 4825771 0014464 280 IDT



2711 drw 12

ORDERING INFORMATION

IDT	XXXX	XX	XXX	X	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank B	Commercial (0°C to +70°C) Military (-55°C to +125°C) Semiconductor components compliant to MIL-STD-883, Class B
					CH NH*	LCCs on a Sidebrazed HIP (Hex In-line Package) SOJs on a Sidebrazed HIP (Hex In-line Package)
					15	(commercial only)
					17	(commercial only)
					20	
					25	
					30	
					35	
					40	
					45	
					50	
					60	
					S	Standard Power
					7M4003	32K x 32 CMOS Static RAM Module
					7M4013	128K x 32 CMOS Static RAM Module

Speed in Nanoseconds

* NH - This package option is only available on the IDT7M4013 version

2711 drw 13