Integrated Device Technology, Inc.

64K X 16 CMOS STATIC RAM MODULE

IDT7M624S

FEATURES:

- High-density 1 Megabit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - — Military: 30ns (max.)
  - — Commercial: 25ns (max.)
- Low power consumption
  - — Active: 4.8W (typ. in 64K x 16 organization)
  - — Standby: 1.6mW (typ.)
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT7M624 is a 1 Megabit high-speed CMOS static RAM module constructed on a multi-layered ceramic substrate using sixteen 64K x 1 static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds can be achieved by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS™.

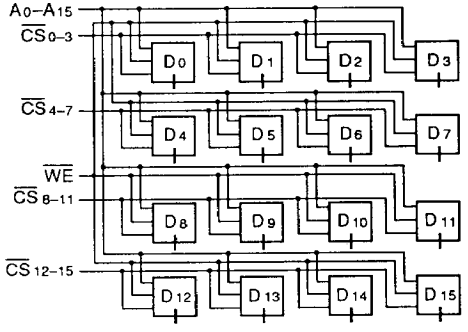
The IDT7M624 is available with access times as fast as 25ns (max.) commercial and 30ns (max.) military temperature range, with maximum operating power consumption of only 12.3W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 5.7W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

All IDT military module semiconductor components are compliant with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

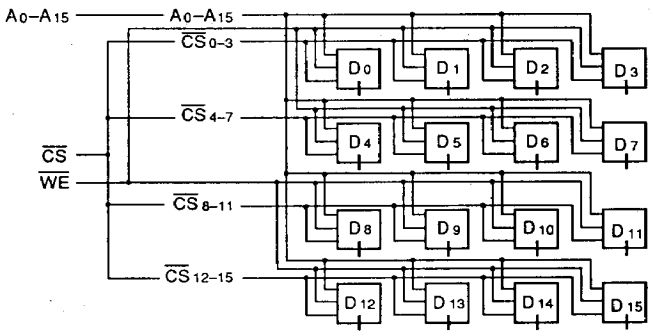
FUNCTIONAL BLOCK DIAGRAM



2663 drw 01

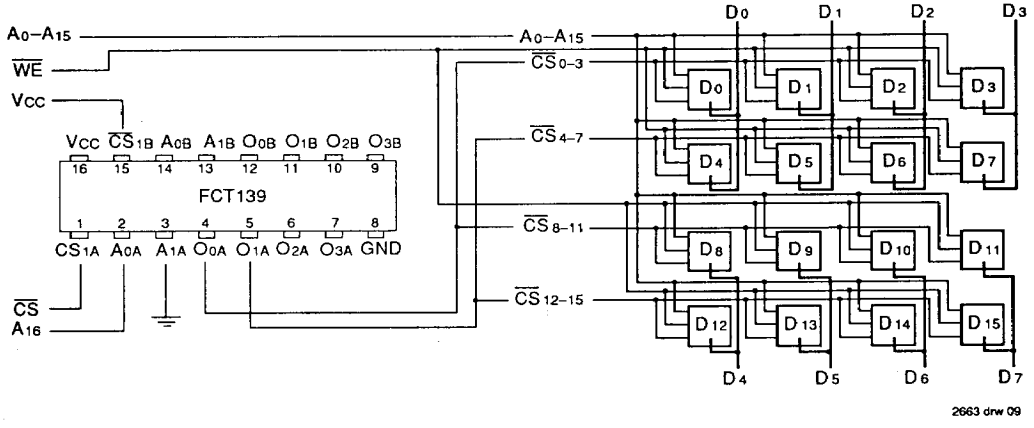
CEMOS is a trademark of Integrated Device Technology, Inc.

IDT7M624
64K x 16 CONFIGURATION



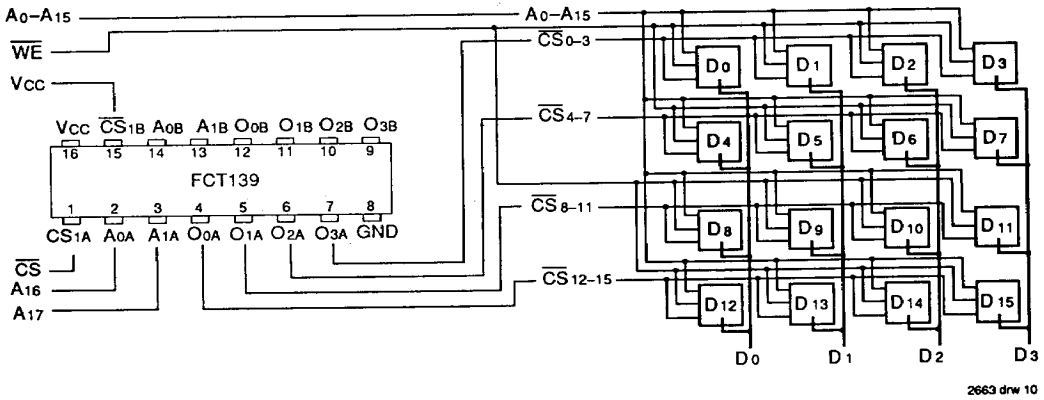
NOTE:
1. All chip selects tied together since, in a by 16 configuration, all chips are either on or off.

IDT7M624
128K x 8 CONFIGURATION



NOTE:
1. The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{16}) to determine which of the two banks of memory are enabled.

IDT7M624
256K x 4 CONFIGURATION

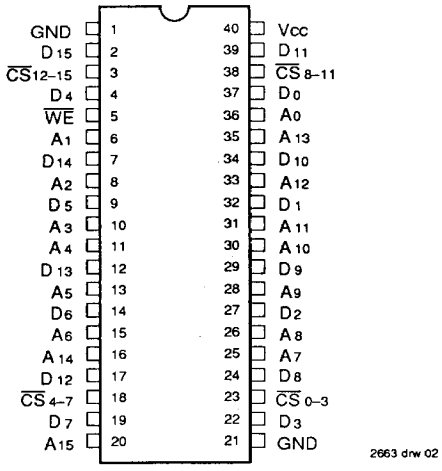


2663 drw 10

NOTE:
1. Each chip is now controlled by the two higher order address pins A16 and A17.

8

PIN CONFIGURATION[1]



2663 drw 02

DIP
TOP VIEW

NOTE:
1. For module dimensions, please refer to module drawing M8 in the packaging section

TRUTH TABLE

Mode	$\overline{CS}$xx	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

2663 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to + 125°C	0V	5.0V ± 10%
Commercial	0°C to + 70°C	0V	5.0V ± 10%

2663 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

2663 tbl 03

PIN NAMES

A0-15	Address
D0-15	Data Input/Output
$\overline{CS}$xx	Chip Selects
$\overline{WE}$	Write Enable
Vcc	Power
GND	Ground

2663 tbl 04

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	° C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	° C
TSTG	Storage Temperature	-55 to + 125	-65 to +155	° C
bUT	DC Output Current	50	50	mA

2663 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = + 25° C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Units
CIN	Input Capacitance	VIN= 0V	130	pF
COUT	Output Capacitance	VOUT= 0V	35	pF

2663 tbl 06

NOTE:
1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55° C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7M624S Min.	Typ(1)	Max.(3)	Max.(4)	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}$xx = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	20	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}$xx = V_{IL}, Output Open, V_{CC} = 5.5V, f = fMAX	—	960	1950	2240	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}$xx = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	720	1380	1640	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}$xx = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	600	1100	1340	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$xx ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	480	820	1040	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$xx ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V (CMOS Level)	—	0.32	320(2)	320	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V	—	—	0.5	0.5	V
		I_{OL} = 8mA, V_{CC} = 4.5V	—	—	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC}= 4.5V	2.4	—	—	—	V

2663 tbl 07

NOTES:
1. Typical limits are at V_{CC} = 5.0V, + 25° C.
2. I_{SB1} max. at commercial temperature = 240mA.
2. t_{AA} = 30, 35, 45, 55, 65ns.
3. t_{AA} = 25ns.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2663 tbl 08

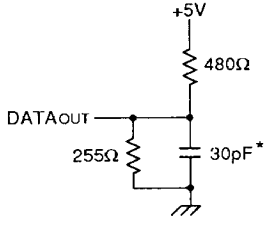


Figure 1. Output Load

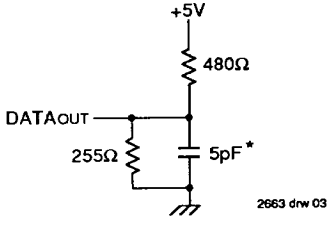


Figure 2. Output Load (for t_{CHZ}, t_{CLZ}, t_{WHZ} and t_{OW})

*Including scope and jig.

8

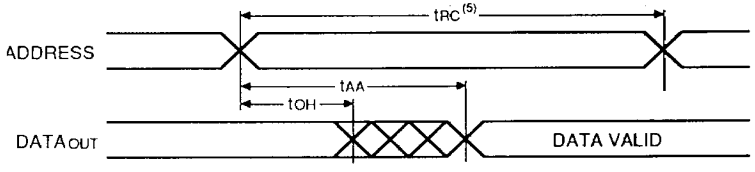
AC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, TA = -55° C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M624S25 Com'l. Only		7M624S30		7M624S35		7M624S45		7M624S55		7M624S65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t RC	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	65	—	ns
t AA	Address Access Time	—	25	—	30	—	35	—	45	—	55	—	65	ns
t ACS	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	—	65	ns
t OH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t CLZ	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t CHZ	Chip Deselection to Output in High Z	—	20	—	25	—	30	—	30	—	30	—	30	ns
t PU	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t PD	Chip Selection to Power Down Time	—	25	—	30	—	35	—	35	—	35	—	35	ns
Write Cycle														
t WC	Write Cycle Time	25	—	30	—	35	—	45	—	55	—	65	—	ns
t CW	Chip Selection to End of Write	22	—	25	—	30	—	40	—	50	—	55	—	ns
t AW	Address Valid to End of Write	22	—	25	—	30	—	40	—	50	—	55	—	ns
t AS	Address Set-up Time	2	—	3	—	5	—	5	—	5	—	10	—	ns
t WP	Write Pulse Width	20	—	20	—	25	—	30	—	35	—	40	—	ns
t WR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t DW	Data Valid to End of Write	15	—	20	—	20	—	25	—	25	—	30	—	ns
t DH	Data Hold Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
t WHZ	Write Enable to Output in High Z	0	20	0	25	0	30	0	30	0	30	0	35	ns
t OW	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

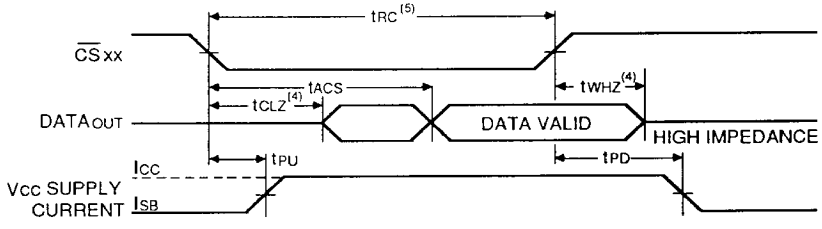
2663 tbl 09

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 2)



2663 drw 04

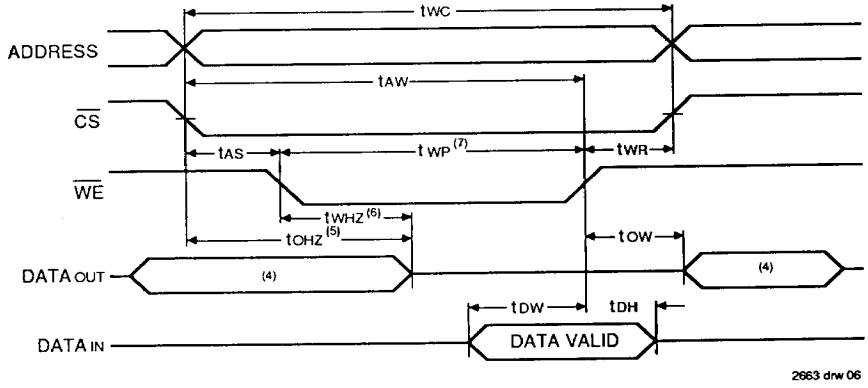
TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 3)



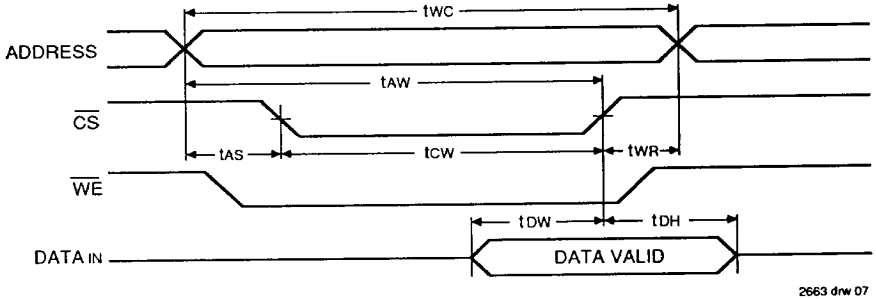
2663 drw 05

NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$xx is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$xx transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is guaranteed by design but not tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design but not tested.

8

ORDERING INFORMATION