

MAXIM INTEGRATED PRODUCTS

MAXIM

CMOS, TTL-Compatible Analog Switches

IH5140-IH5145/883B

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1.0 SCOPE

- 1.1** This specification covers the detail requirements for six CMOS switches with three switch configurations (SPST, SPDT, and DPST). These circuits are processed in accordance with MIL-STD-883 and are fully compliant to paragraph 1.2.1.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace source control drawings.

For typical applications and operating characteristics, consult Maxim's data books.

1.2 Part Numbers

Device	Part Number
-1	IH5140M(X)/883B
-2	IH5141M(X)/883B
-3	IH5142M(X)/883B
-4	IH5143M(X)/883B
-5	IH5144M(X)/883B
-6	IH5145M(X)/883B

1.3 Package

(X)	Package	Description
JE	J-16	16-Pin Ceramic Dual-In-Line Package (CERDIP)

Note: See *Package Information* section for package drawing and dimensions.

1.4 Absolute Maximum Ratings

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_+ to V_-	44V
V_+ to V_D	30V
V_D to V_-	$\pm 22\text{V}$
V_L to V_-	33V
V_L to V_{IN}	30V
V_L	20V
V_{IN}	20V
Current, Any Terminal	30mA
Power Dissipation ($T_j = +150^\circ\text{C}$)	
up to $+70^\circ\text{C}$	800mW
derate above $+70^\circ\text{C}$	10mW/ $^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (soldering, 10 sec)	$+300^\circ\text{C}$

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- 1.5 Thermal Resistance $\Theta_{JC} = 50^{\circ}\text{C/W}$
 $\Theta_{JA} = 100^{\circ}\text{C/W}$

2.0 REQUIREMENTS

- 2.1 Electrical performance characteristics are specified in Table 1 and apply over the full ambient operating temperature range, unless otherwise specified.

TABLE 1. ELECTRICAL PERFORMANCE CHARACTERISTICS (Note 1)

CHARACTERISTICS	SYMBOL	CONDITIONS	DEVICE TYPES	GROUP A SUB-GROUPS	LIMITS		UNITS
					MIN	MAX	
Input Logic Current	I_{INH}	$V_{IN} = 0.8\text{V or } 2.4\text{V (Note 2)}$	All	1, 3	± 1		μA
				2		± 10	
Input Logic Current	I_{INL}	$V_{IN} = 0.8\text{V or } 2.4\text{V (Note 2)}$	All	1, 3	± 1		μA
				2		± 10	
Drain-Source On Resistance	$r_{DS(ON)}$	$I_S = -10\text{mA}, V_{ANALOG} = \pm 10\text{V}$	All	1, 3	50		Ω
				2	75		
Switch-Off Leakage Current	$I_{D(OFF)} + I_{S(OFF)}$	$V_D = \pm 10\text{V}, V_S = \mp 10\text{V}$	All	1	± 0.5		nA
				2	100		
Switch-On Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_D = V_S = \pm 10\text{V}$	All	1	± 1		nA
				2	200		
Positive Power-Supply Quiescent Current	I_+	$V_+ = 15\text{V}, V_- = -15\text{V}, V_L = 5\text{V}$	All	1, 3	1		μA
				2	10		
Negative Power-Supply Quiescent Current	I_-	$V_+ = 15\text{V}, V_- = -15\text{V}, V_L = 5\text{V}$	All	1, 3	1		μA
				2	10		
+5V Power-Supply Quiescent Current	I_L	$V_+ = 15\text{V}, V_- = -15\text{V}, V_L = 5\text{V}$	All	1, 3	1		μA
				2	10		
Ground-Supply Quiescent Current	I_{GND}	$V_+ = 15\text{V}, V_- = -15\text{V}, V_L = 5\text{V}$	All	1, 3	1		μA
				2	10		
Switch-On Time	t_{ON}	Figure 1	-1, -2	9	150		ns
			-3	9	200		
Switch-Off Time	t_{OFF}	Figure 1	-1 to -6	9	125		ns

Note 1: $V_+ = 15\text{V}, V_- = -15\text{V}, V_L = +5\text{V}$, unless otherwise noted.

Note 2: Some channels are turned off by high (1) logic inputs and other channels by low (0) inputs; however, 0.8V and 2.4V describe the minimum range for proper switching. Refer to logic diagrams for logical input value for on or off states.

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3.0 QUALITY ASSURANCE

- 3.1** Sampling and inspection procedures shall be in accordance with MIL-M-38510 and, to the extent specified, with MIL-STD-883.
- 3.2** Screening shall be in accordance with Method 5004 of MIL-STD-883. Burn-in test (Method 1015):
- (1) Test condition A, B, C, or D.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Interim and final electrical test requirements shall be as specified in Table 2.
- 3.3** Quality conformance inspection shall be in accordance with Method 5005 of MIL-STD-883 including Groups A, B, C, and D inspection.
- Group A inspection:
- (1) Tests as specified in Table 2.
 - (2) Selected subgroups in Table 1, Method 5005 of MIL-STD-883 shall be omitted.
- 3.4** Groups C and D inspections:
- a. End-point electrical parameters shall be specified in Table 1.
 - b. Steady-state life test (Method 1005 of MIL-STD-883):
- (1) Test condition A, B, C, or D.
 - (2) $T_A = +125^\circ\text{C}$, minimum.
 - (3) Test duration, 1000 hours, except as permitted by Method 1005 of MIL-STD-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

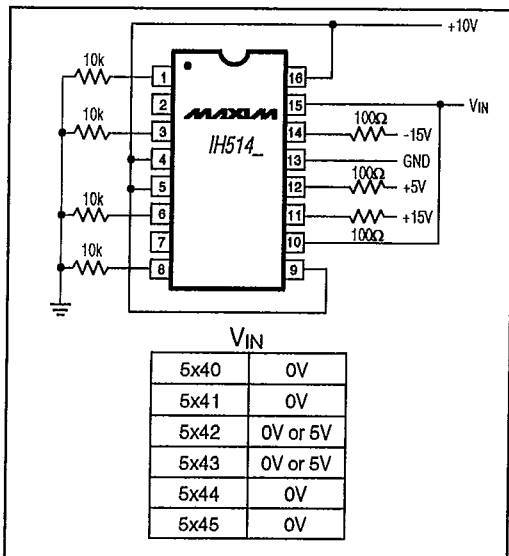
MIL-STD-883 Test Requirements	Subgroups (per Method 5005, Table 1)
Interim Electrical Parameters (Method 5004)	1
Final Electrical Parameters (Method 5004)	1, * 2, 3, 9
Group A Test Requirements (Method 5005)	1, 2, 3, 9, 10, ** 11**
Groups C and D End-Point Electrical Parameters (Method 5005)	1

* PDA applies to Subgroup 1 only.

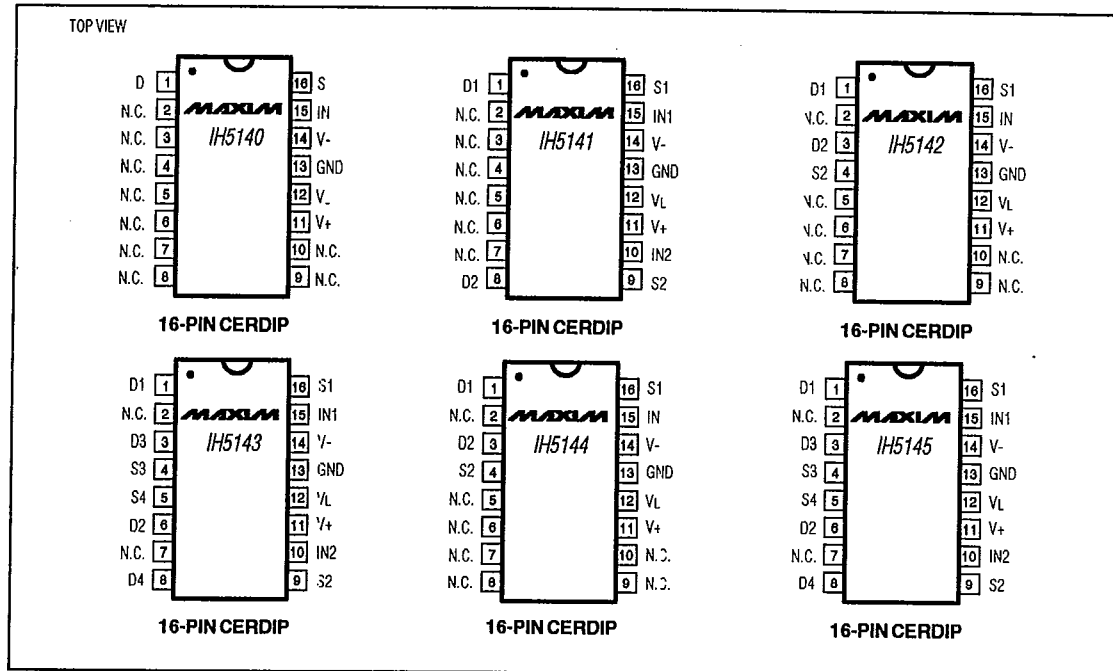
** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits in Table 1.

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4.0 Life Test/Burn-In Circuits

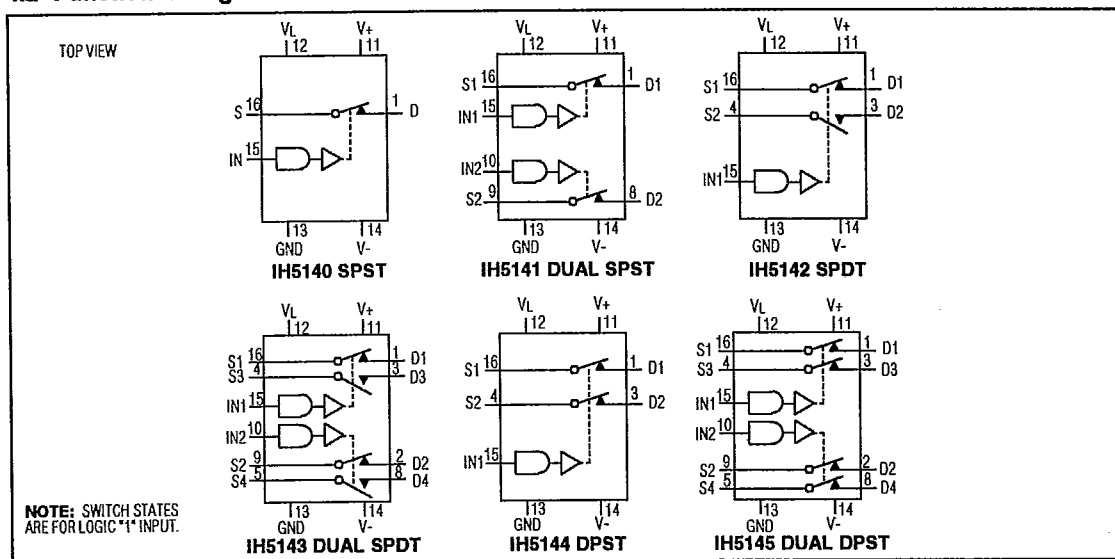


4.1 Pin Configurations



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4.2 Functional Diagrams



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4.3 Test Circuit/Timing Diagram

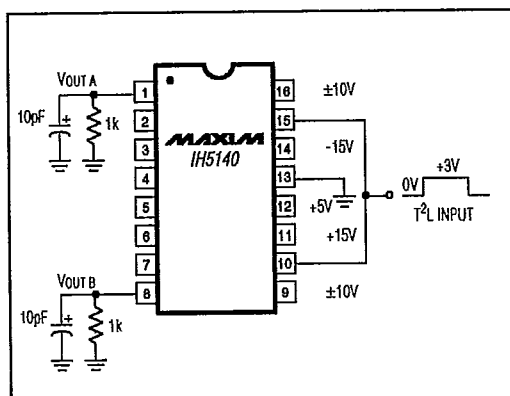


Figure 1. Switching-Time Test Circuit