ISO 9001 Registered

IMP5241/42

9-Line Multimode LVD/SE SCSI Terminator

DESCRIPTION

The IMP5241/42 is a multimode SCSI terminator that conforms to the SCSI Parallel Interconnect-2 (SPI-2) specification developed by the T10 standards committee for low voltage differential (LVD) termination, while providing backwards compatibility to the SCSI, SCSI-2, and SPI single-ended specifications. Multimode compatibility permits the use of legacy devices on the bus without hardware alterations. Automatic mode selection is achieved through voltage detection on the diffsense line.

The IMP5241/42 utilizes IMP's adaptive non-linear technology for the ultimate in SCSI bus performance while saving component cost and board area. Elimination of the external capacitors also mitigates the need for a lengthy capacitor selection process. The individual high bandwidth drivers also maximize channel separation and reduce channel to channel noise and cross talk. The high bandwidth architecture insures ULTRA2 performance while providing a clear migration path to ULTRA3 and beyond.

When the IMP5241/42 is enabled, the differential sense (DIFFSENSE) pin supplies a voltage between 1.2V and 1.4V. In application, this pin is tied to the DIFFSENSE input of the corresponding LVD transceivers. This action enables the LVD transceiver function. DIFFSENSE is capable of supplying a maximum of 15mA. Tying the DIFFSENSE pin high places the IMP5241/42 in a HI Z state indicating the presence of an HVD device. Tying the pin low places the part in a single-ended mode while also signaling the multimode transceiver to operate in a single-ended mode.

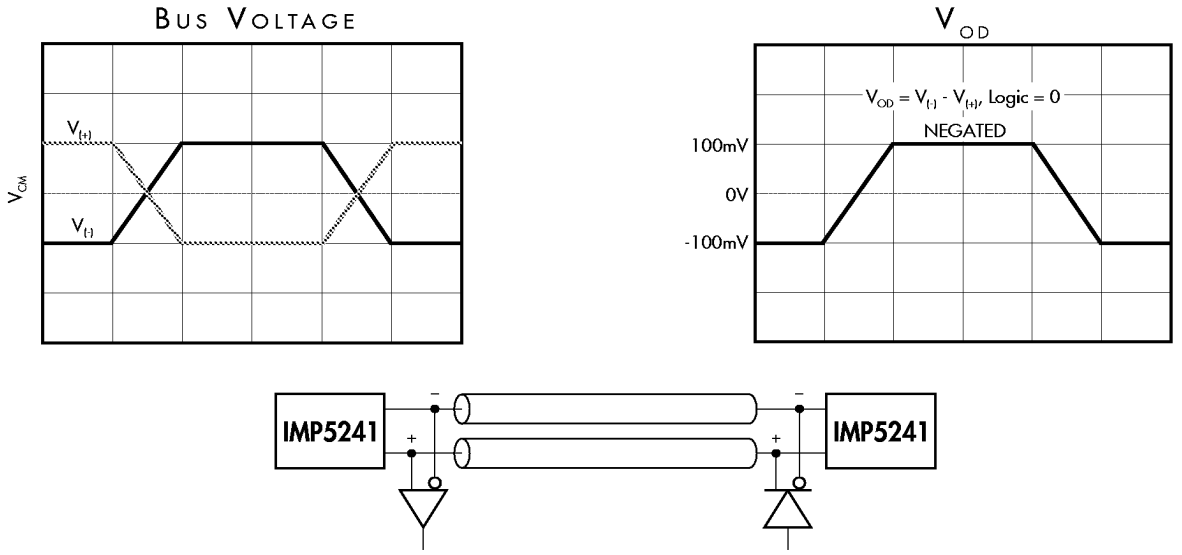
Recognizing the needs of portable and configurable peripherals, the IMP5241/42 have a TTL compatible sleep/disable mode. During this sleep/disable mode, power dissipation is reduced to a meager 5µA while also placing all outputs in a HI Z state. Also during sleep/disable mode, the DIFFSENSE function is disabled and is placed in a HI Z state.

Another key feature of the IMP5241/42 is the master / slave function. Driving this pin high or floating the pin enables the 1.3V DIFFSENSE reference. Driving the pin low disables the on board DIFFSENSE reference and enables use of an external master reference device.

KEY FEATURES

- AUTO-SELECTABLE LVD OR SINGLE-ENDED TERMINATION
- 3.0pF MAXIMUM DISABLED OUTPUT CAPACITANCE
- FAST RESPONSE, NO EXTERNAL CAPACITORS REQUIRED
- COMPATIBLE WITH ACTIVE NEGATION DRIVERS
- 5µA SUPPLY CURRENT IN DISCONNECT MODE
- LOGIC COMMAND DISCONNECTS ALL TERMINATION LINES
- DIFFSENSE LINE DRIVER
- GROUND DRIVER INTEGRATED FOR SINGLE-ENDED OPERATION
- CURRENT LIMIT AND THERMAL PROTECTION
- HOT-SWAP COMPATIBLE (SINGLE-ENDED)
- COMPATIBLE WITH SCSI 1, 2, 3, FAST-20, AND THE PENDING SPI-2 LVD
- SEE IMP5244 FOR LVD TERMINATION ONLY

PRODUCT HIGHLIGHT



PACKAGE ORDER INFORMATION

T_A (°C)	DB Plastic SSOP 36-pin	PW Plastic TSSOP 24-pin
0 to 70	IMP5241CDB	IMP5241CPW
	IMP5242CDB	IMP5242CPW

Note: All surface-mount packages are available in Tape & Reel. Append the letter "T" to part number. (i.e. IMP5241/42CDBT)

ABSOLUTE MAXIMUM RATINGS (Note 1)

TermPwr Voltage ..... +7V
Operating Junction Temperature
Plastic (DB, PW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

THERMAL DATA

DB PACKAGE:

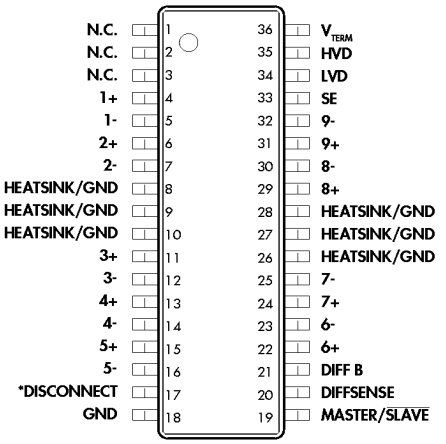
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Θ_{JA} ..... 50°C/W

PW PACKAGE:

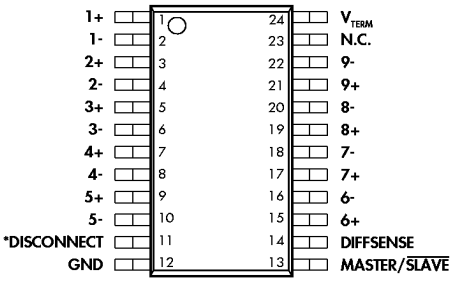
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Θ_{JA} ..... 144°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUTS



DB PACKAGE
(Top View)



PW PACKAGE
(Top View)

$\overline{\text{*DISCONNECT}}$ for the IMP5242

MASTER / $\overline{\text{SLAVE}}$ FUNCTION TABLE

MASTER / SLAVE	DIFFSENSE Status	Output Current
L*	HI Z	0mA
H	1.3V	15mA Source
Open (Pull-up)	1.3V	15mA Source

* When in LOW state, terminator will detect state of DIFFSENSE line.

DIFFSENSE / POWER UP / POWER DOWN FUNCTION TABLE

IMP5241 DISCONNECT	IMP5242 $\overline{\text{DISCONNECT}}$	DIFF SENSE	Outputs Status	Outputs Type
L	H	L < 0.5V	Enable	S.E.
L	H	0.7 to 1.9V	Enable	LVD
L	H	H > 2.4V	Disable	HI Z
H Open	L Open	X	Disable	HI Z

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Termpwr Voltage LVD	V_{TERM}	3.0		5.25	V
SE		4.0		5.25	V
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		V_{TERM}	V
Operating Virtual Junction Temperature Range					
IMP5241 / 5242C		0		70	°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply over the operating ambient temperature range of $0°C \le T_A \le 70°C$, TermPwr = 4.75V. For the IMP5241 DISCONNECT = L, for the IMP5242 $\overline{\text{DISCONNECT}}$ = H. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

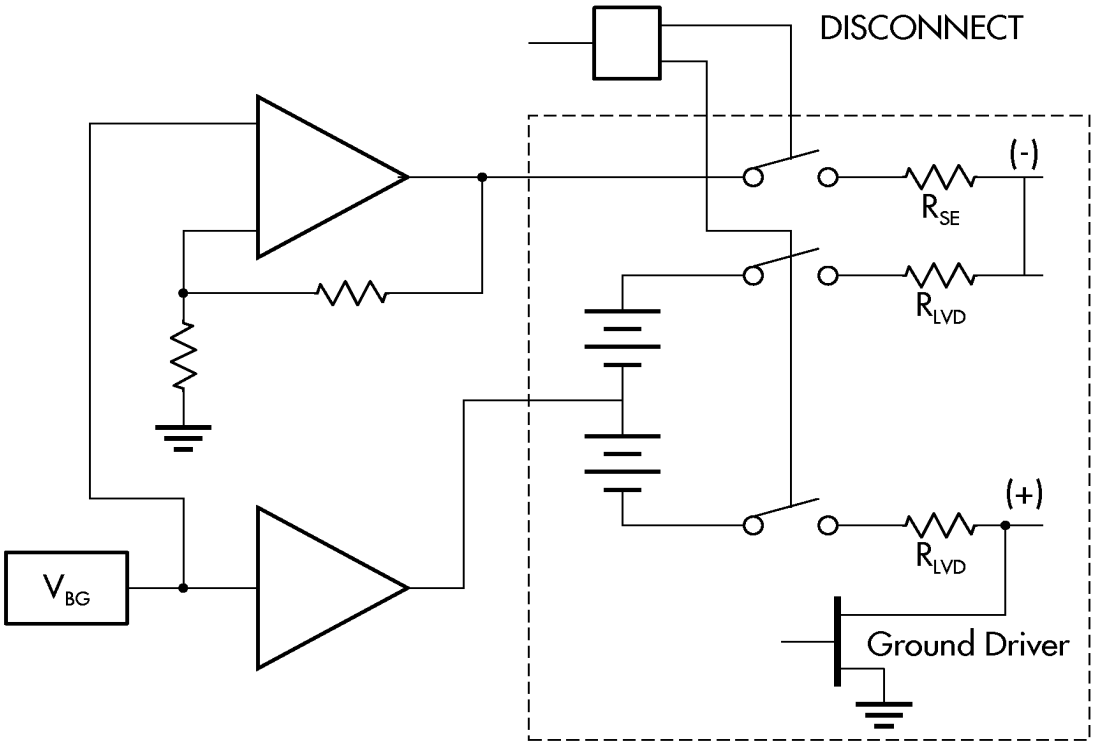
Parameter	Symbol	Test Conditions	IMP5241 / 5242			Units
			Min.	Typ.	Max.	
LVD Terminator Section						
TermPwr Supply Current		All term lines = Open		25	32	mA
		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V		5	25	µA
Common Mode Voltage			1.125	1.25	1.375	V
Offset Voltage		Open circuit between - and + (see Note 3)	100	112	125	mV
Differential Terminator Impedance			100	105	110	Ω
Common Mode Impedance			100	200	300	Ω
Output Capacitance		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V		2.5		pF
Output Leakage		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V, V_{LINE} = 0 to 4V, T_A = 25°C			2	µA
		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V, V_{TERM} = 0V, V_{LINE} = 0V to 4V, T_A = 25°C		1		µA
Channel Bandwidth				40		MHz
Mode Change Delay		DIFFSENSE = 1.4V to 0V		115		ms
DIFFSENSE Section						
DIFFSENSE Output Voltage			1.2	1.3	1.4	V
DIFFSENSE Output Source Current		V_{DIFF} = 0V	5.0		15.0	mA
DIFFSENSE Sink Current		V_{DIFF} = 2.75V			200	µA
DIFFSENSE Output Leakage		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V, T_A = 25°C			10	µA
Single-Ended Termination Section						
Termpwr Supply Current		All term lines = Open, Master/Slave = 0V		9	18	mA
		All term lines = 0.2V, Master/Slave = 0V		214	245	mA
		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V			25	µA
Terminator Output High Volt			2.6	2.85		V
Output Current		V_{OUT} = 0.2V	21	23	25	mA
Sink Current		V_{OUT} = 4V, All lines	35	65		mA
Output Capacitance		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V		2.5		pF
Leakage Current		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V, V_{OUT} = 0 to 4V, T_A = 25°C			2	µA
		IMP5241: DISCONNECT > 2.0V, IMP5242: $\overline{\text{DISCONNECT}}$ < 0.8V, V_{TERM} = 0V, V_{LINE} = 2.7V		1		µA

Note 3. Open circuit failsafe voltage.

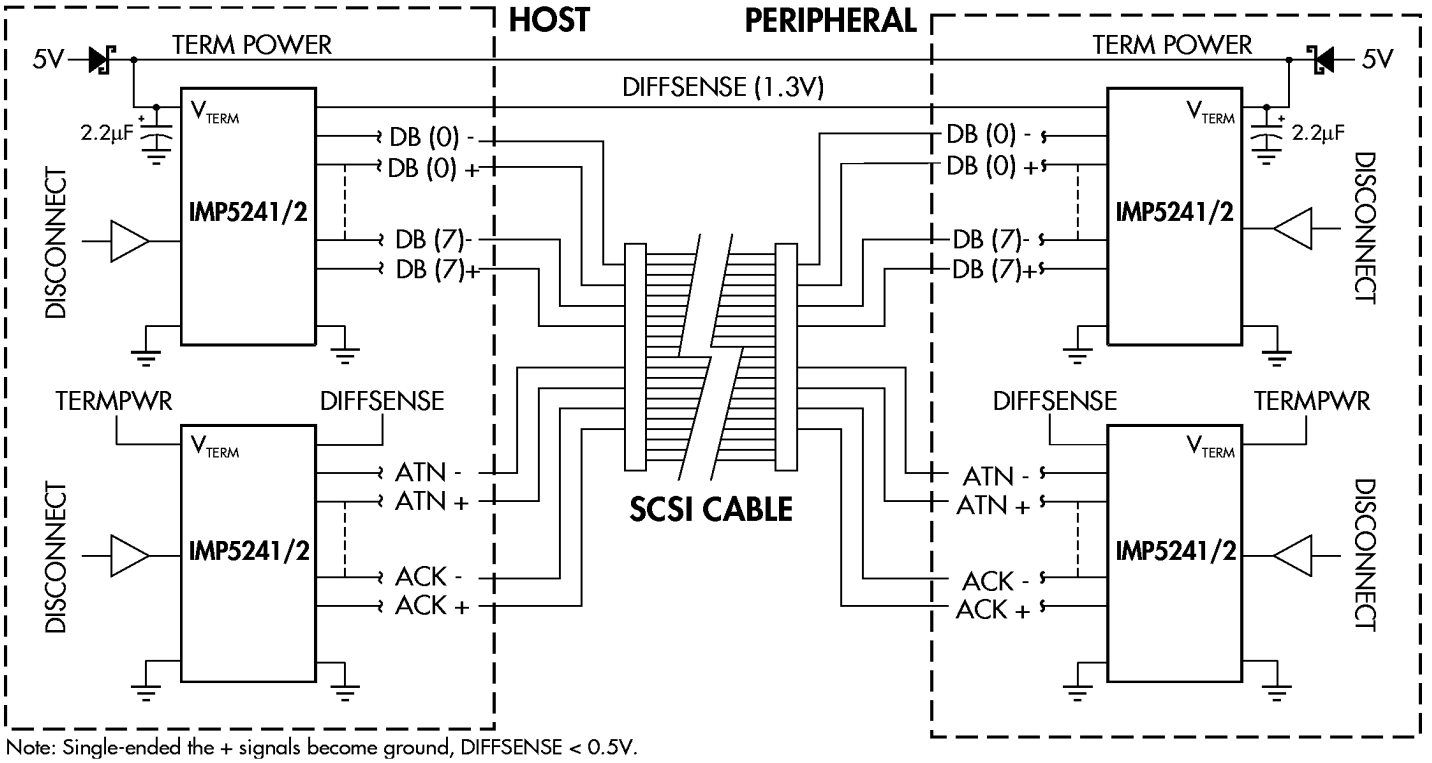
ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Test Conditions	IMP5241/42			Units
				Min.	Typ.	Max.	
Single-Ended Termination Section (continued)							
Ground Driver Impedance			I = 2mA			100	Ω
Thermal Shutdown					150		°C
Channel Bandwidth					40		MHz
DISCONNECT Section							
DISCONNECT Thresholds				0.8		2.0	V
Input Current	IMP5241		DISCONNECT = 0V			10	µA
	IMP5242		$\overline{\text{DISCONNECT}}$ = 0V			100	nA
	IMP5241		DISCONNECT = 4.75V			100	nA
	IMP5242		$\overline{\text{DISCONNECT}}$ = 2.4V			10	µA
MASTER / $\overline{\text{SLAVE}}$ Section							
MASTER / $\overline{\text{SLAVE}}$ Thresholds				0.8		2.0	V
Input Current			MASTER / $\overline{\text{SLAVE}}$ = 0V			10	µA
			MASTER / $\overline{\text{SLAVE}}$ = 4.75V			100	nA

BLOCK DIAGRAM



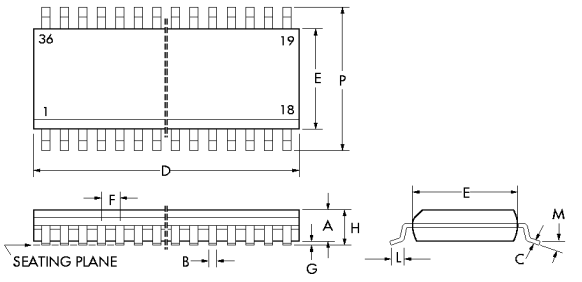
APPLICATION SCHEMATIC



Note: Single-ended the + signals become ground, DIFFSENSE < 0.5V.

PACKAGE DIMENSIONS

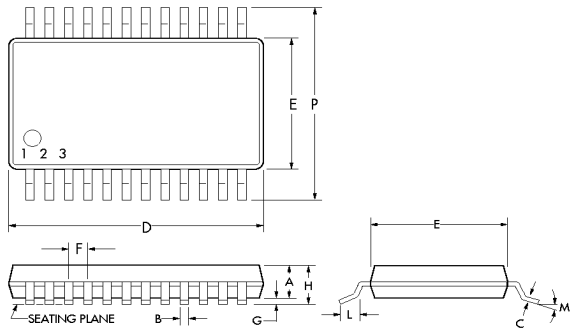
DB 36-Pin Plastic (SSOP) Widebody S.O.I.C.



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.14	2.54	0.084	0.100
B	0.29	0.51	0.011	0.020
C	0.23	0.32	0.0091	0.0125
D	15.20	15.40	0.598	0.606
E	7.40	7.60	0.291	0.299
F	0.80 BSC		0.031 BSC	
G	0.10	0.30	0.004	0.012
H	2.44	2.64	0.096	0.104
L	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
P	10.11	10.51	0.398	0.414
*LC	—	0.10	—	0.004

* Lead Coplanarity

PWP 24-Pin Thin Small Shrink Outline (TSSOP)



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	0.80	1.05	.032	.041
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.0079
D	7.70	7.90	0.303	0.311
E	4.30	4.5	0.169	0.176
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	—	1.20	—	0.047
L	0.45	0.75	0.017	0.030
M	0°	8°	0°	8°
P	6.25	6.50	0.246	0.256
*LC	—	0.10	—	0.004

* Lead Coplanarity

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