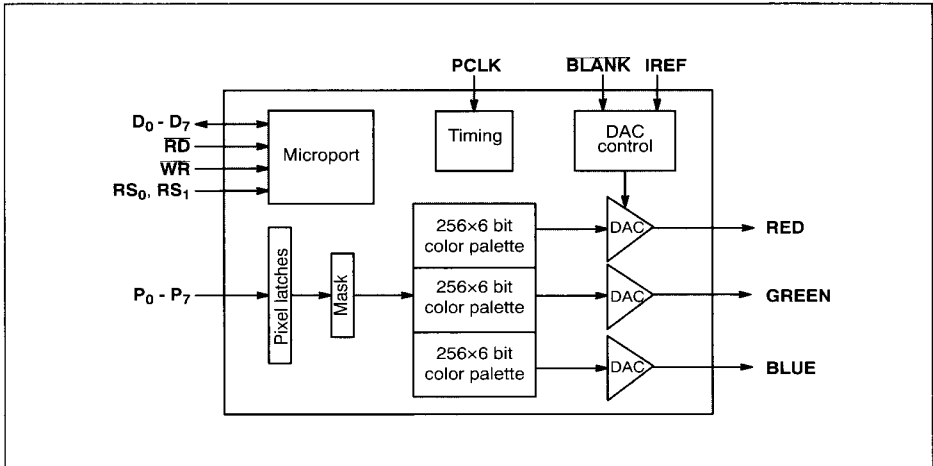


HIGH PERFORMANCE CMOS PALETTE-DAC

DESIGNED TO BE COMPATIBLE WITH
 IBM PS/2, VGA GRAPHICS SYSTEMS



FEATURES

- Compatible with VGA standard IMS G171
- Pixel rates up to 80MHz
- Compatible with the RS170 video standard
- 256K possible colors
- Single monolithic, high performance CMOS
- Pixel word mask
- RGB analogue output, 6 bit DAC per gun
- Composite blank on all three channels
- Low DAC glitch energy
- Video signal output into 37.5Ω
- Up to 8 bits per pixel
- TTL compatible inputs
- Microprocessor compatible interface
- Single +5V power supply
- Low power dissipation, 950mW max. at maximum pixel rate
- Standard 600 mil 28 pin DIL or 32 pin or 44 pin Plastic LCC
- Anti-sparkle microprocessor circuitry

DESCRIPTION

The IMS G176 integrates the functions of a color palette (or color look-up table), digital to analogue converters (DACs) and bi-directional microprocessor interface into a single 28 pin DIL, 32 pin or 44 pin PLCC package.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite blank signals can be generated on all three outputs.

Capable of displaying 256 colors from a total of 262,144 colors, the IMS G176 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colors to be changed in a single write cycle rather than by modifying the look-up table.

TABLE OF CONTENTS

8.1 Description 95

8.2 Pin function reference guide 96

8.3 Internal register description 98

8.4 Device operation 99

8.5 Timing reference guide 101

8.6 Electrical specifications 105

8.7 Package specifications 109

8.8 Ordering information 115



8.1 Description

The IMS G176 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or palette) of 256×18 -bit words, three 6-bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8-bit value read in on the Pixel Address inputs is used as a read address for the palette and results in an 18-bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6-bit DAC.

Pixel rates of up to 80MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G176. This signal acts on all three of the analogue outputs. The **BLANK** signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the palette can be accessed via an 8-bit wide microprocessor interface. The use of an internal synchronizing circuit allows color value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette to facilitate such operations as animation, overlays and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

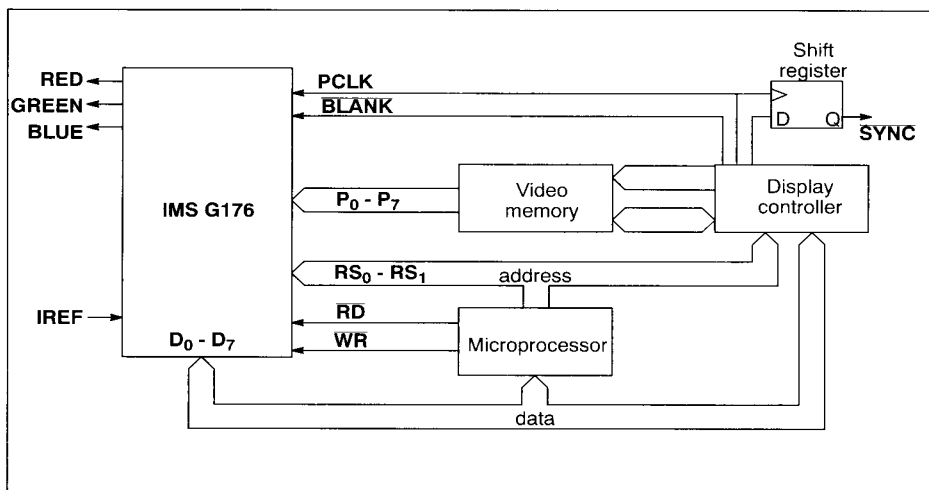


Figure 8.1 Typical IMS G176 application

8.2 Pin function reference guide

8.2.1 Pixel interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
PCLK	13	14	40	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the color palette to the analogue outputs.
P ₀ -P ₇	5-12	6-13	32-39	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the color palette.
BLANK	16	20	7	I	Blank	A low value on this input, when sampled, will cause a color value of zero to be applied to the inputs of the DACs regardless of the color value of the current pixel.

8.2.2 Microprocessor interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
WR	25	29	16	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
RD	15	19	6	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the color palette. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behavior. The Read and Write Enable signals should not be asserted at the same time.
RS ₀ , RS ₁	26, 27	30, 31	17, 18	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal (RD or WR); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
D ₀ -D ₇	17-24	21-28	8-15	I/O	Program Data	Data is transferred between the 8-bit wide Program Data bus and the registers within the IMS G176 under control of the active enable signal (RD or WR). In a write cycle the rising edge of WR validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the RD signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.

8.2.3 Analogue interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
RED	1	2	25	O		These signals are the outputs of the 6-bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. The number of current sources active is controlled by the 6-bit binary value applied.
BLUE	2	3	26	O		
GREEN	3	4	27	O		
IREF	4	5	28	I	Reference current	The reference current drawn from VDD (or AVDD) via the IREF pin determines the current sourced by each of the current sources in the DACs.

8.2.4 Power supply

Signal	Pin number			Signal name	Description
	DIL	PLCC			
		32	44		
VDD	28			Power supply	Digital and analogue supply pads are bonded out to a single pin on the DIL package. The package contains a high-frequency decoupling capacitor between VDD and GND to ensure a high quality analogue supply.
VDD		17	4,21,22	Digital supply	Digital and analogue supply pads are bonded out separately on the PLCC package to give highest possible noise immunity. Due to package size limitations the decoupling capacitor must be provided externally (see Chapter 10).
AVDD		32	20	Analogue supply	The AVDD and VDD pins should be connected to the same power supply immediately outside the IMS G176.
GND	14	16	3	Ground	

8.3 Internal register description

RS ₁	RS ₀	Size (bits)	Register name	Description
0	0	8	Address (write mode)	There is a single Address register within the IMS G176. This register can be accessed through either register select 0,0 or 1,1 Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new color definitions to the color palette: a) Specifies an address within the color palette. b) Initializes the Color Value register.
1	1	8	Address (read mode)	Writing a value to register 1,1 performs the following operations which would normally precede reading one or more color definitions from the color palette: a) Specifies an address within the the color palette. b) Loads the Color Value register with the contents of the location in the palette addressed and then increments the Address register. A read from register 0,0 is functionally equivalent to a read from 1,1.
0	1	18	Color Value	The Color Value register is internally an 18-bit wide register used as a buffer between the microprocessor interface and the color palette. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits D₀-D₅ are used. When a byte is read only the least significant six bits contain information – the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the color look-up specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the color palette specified by the Address register are copied into the Color Value register. The Address register then increments. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the IMS G176 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P₀-P₇). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the palette is being accessed via that interface.

8.4 Device operation

8.4.1 Video path

P₀-P₇ and **BLANK** inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analogue outputs after three further rising edges of Pixel Clock (see Figure 8.2).

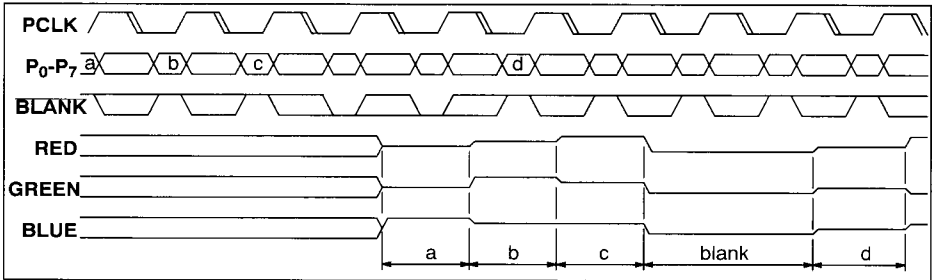


Figure 8.2

8.4.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 9.07 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The **BLANK** input to the IMS G176 acts on all three of the analogue outputs. When the **BLANK** input is low a binary zero is applied to the inputs of the DACs.

The expression for calculating IREF with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAKWHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note that for all values of IREF and output loading:

$$V_{BLACK LEVEL} = 0$$

Information on external current reference circuitry is given in Chapter 10.

8.4.3 Microprocessor interface

Below are listed the three microprocessor interface registers within the IMS G176 and the four locations through which they can be accessed:

RS ₁	RS ₀	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Color Value
1	0	Pixel Mask

The contents of the color palette can be accessed via the Color Value register and the Address register.

The Anti-Sparkle feature enables the user to access the palette during active video without causing random unwanted pixels to be sent to the screen.

Writing to the palette

To set a new color definition a value specifying a location in the color palette is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register the new color definition is transferred to the color palette and the Address register is automatically incremented.

As the Address register increments after each new color definition has been transferred from the Color Value register to the color palette, it is simple to write a set of consecutive locations with new color definitions. First the start address of the set of locations is written to the write mode Address register; then the color definitions for each location are written sequentially to the Color Value register.

Reading from the palette

To read a color definition a value specifying the location in the palette to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Color Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read the location in the palette currently specified by the Address register is copied to the Color Value register and the Address register is again incremented automatically.

Thus a set of color definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the color definitions for each location in the set.

Whenever the Address register is updated any unfinished color definition read or write is aborted and a new one may begin.

Asynchronous microprocessor interface access

Accesses to all registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G176. Data transfers between the palette and the Color Value register and modifications to the Pixel Mask register are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers or modifications to take place.

The Pixel Mask register

The pixel address used to access the color palette through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the palette contents. Thus, by partitioning the color definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is completely independent of the Address and Color Value registers.

8.5 Timing reference guide

8.5.1 Microprocessor interface

Symbol	Parameter	All	40 MHz	50 MHz	66 MHz	80 MHz	Units	Notes
		Max.	Min.	Min.	Min.	Min.		
tWLWH	WR pulse width low		50	50	50	50	ns	
tRLRH	RD pulse width low		50	50	50	50	ns	
tSVWL	Register select setup time		15	10	10	10	ns	
tSVRL	Register select setup time		15	10	10	10	ns	
tWLSX	Register select hold time		15	10	10	10	ns	
tRLSX	Register select hold time		15	10	10	10	ns	
tDVWH	Write data setup time		15	10	10	10	ns	
tWHDX	Write data hold time		15	10	10	10	ns	
tRLQX	Output turn-on delay		5	5	5	5	ns	
tRLQV	Read enable access time	40					ns	
tRHQX	Output hold time		5	5	5	5	ns	
tRHQZ	Output turn-off delay	20					ns	1
tWHWL1	Successive write interval		4xtCHCH +30ns				ns	2
tWHRL1	Write followed by read interval							
tRHRL1	Successive read interval							
tRHWL1	Read followed by write interval							
tWHWL2	Write after color write							
tWHRL2	Read after color write		6xtCHCH +40ns				ns	2
tRHWL2	Write after color read							
tRHRL2	Read after color read		6xtCHCH +40ns				ns	2
tWHRL3	Read after read address write							
tCYC	Write/Read cycle time		6xtCHCH +40ns				ns	2,3
	Write/Read enable transition time	50						

Table 8.1 Microprocessor interface timing parameters

Notes

- 1 Measured $\pm 200\text{mV}$ from steady output voltage.
- 2 This parameter allows for synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.
- 3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the microprocessor port are internally synchronized to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the microprocessor port being specified in terms of pixel clock periods.

In the case of the IMS G176 the minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is $6 \times tCHCH + 40\text{ns}$.

For example, in the case of a 25MHz system the pixel clock period (tCHCH) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

$$6 \times 40\text{ns} + 40\text{ns} = 280\text{ns}$$

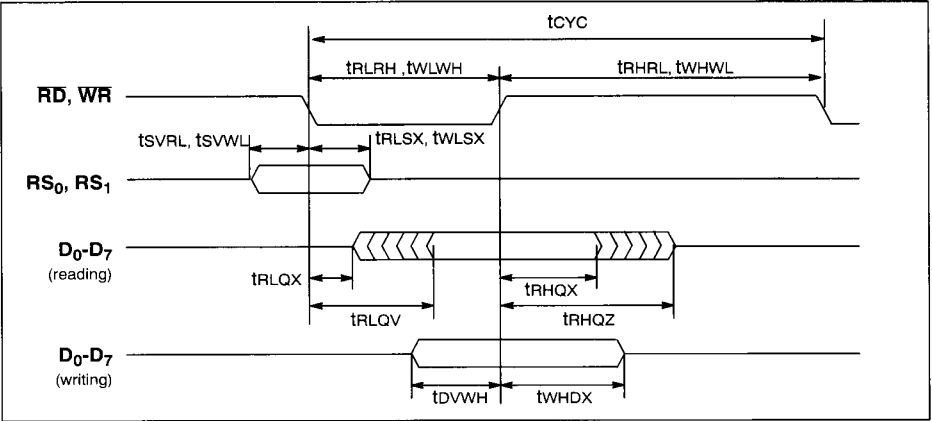


Figure 8.3 Basic read/write cycle

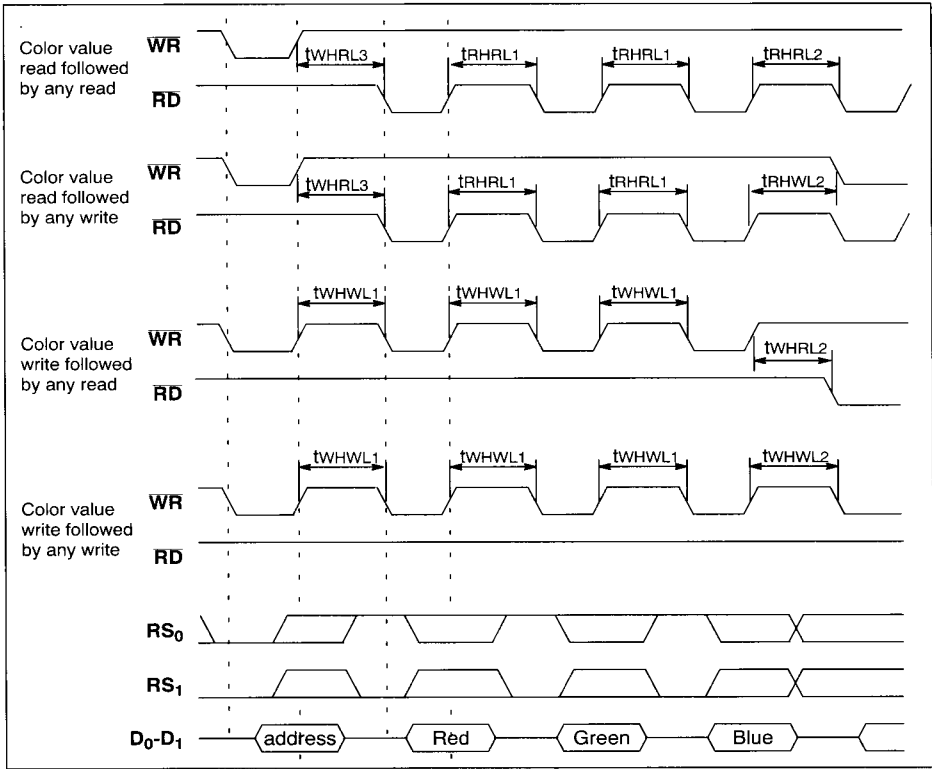


Figure 8.4 Color value read and write accesses



8.5.2 Video operation

Symbol	Parameter	All	40 MHz	50 MHz	66 MHz	80 MHz	Units	Notes
		Max.	Min.	Min.	Min.	Min.		
tCHCH	PCLK period	10000	25	20	15.1	12.5	ns	1
Δ tCHCH	PCLK jitter	± 5					%	
tCLCH	PCLK width low	10000	9	6	5	5	ns	
tCHCL	PCLK width high	10000	7	6	5	5	ns	
tPVCH	Pixel address set-up time		5	4	3	3	ns	2
tCHPX	Pixel address hold time		5	4	3	3	ns	2
tBVCH	BLANK setup time		5	4	3	3	ns	
tCHBX	BLANK hold time		5	4	3	3	ns	
tCHAV	PCLK to valid DAC output	30	5	5	5	5	ns	3
Δ tCHAV	Differential output delay	2					ns	4
	Pixel clock transition time	50					ns	

Notes

- 1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.
- 2 It is required that the Pixel Address input to the color palette be set up as a valid logic level with the appropriate setup and hold times to each rising edge of **PCLK** (this requirement must be met during the blanking period).
- 3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.
- 4 Between different analogue outputs on the same device.

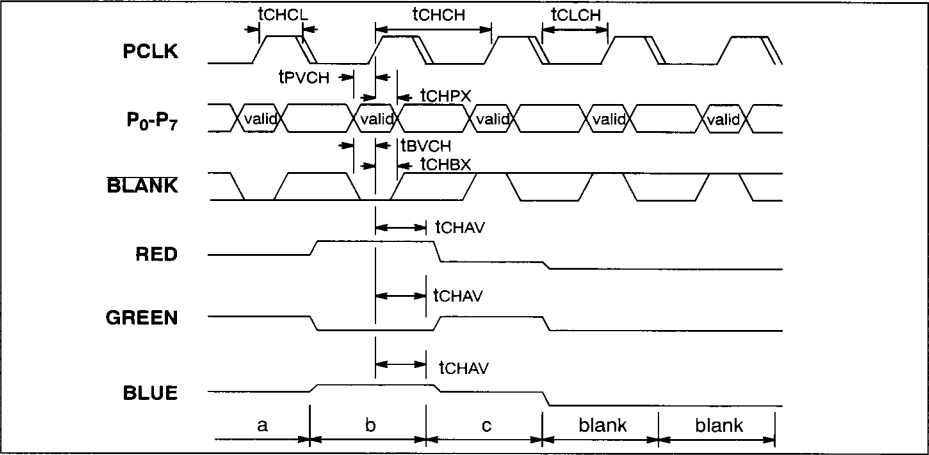


Figure 8.5 Video operation

8.6 Electrical specifications

8.6.1 Absolute maximum ratings *

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	GND-1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	-55	125	°C	
TA	Temperature under bias	-40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	-15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.6.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive supply voltage	4.50	5.0	5.50	V	2,3,IMS G176-40/50
VDD	Positive supply voltage	4.75	5.0	5.25	V	2,3,IMS G176-66/80
GND	Ground		0		V	
VIH	Input logic '1' voltage	2.0		VDD+0.5	V	
VIL	Input logic '0' voltage	-0.5		0.8	V	4
TA	Ambient operating temperature	0		70	°C	5
IREF	Reference current	-6.0		-10	mA	6

Notes (Note 1 applies to all parameters)

- 1 All voltages are with respect to GND unless specified otherwise.
- 2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.
- 3 These voltage ranges apply equally for AVDD and VDD when using the PLCC packaged device.
- 4 $V_{IL}(\min) = -1.0V$ for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.
- 5 With a 400 linear ft/min transverse air flow.
- 6 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes
VREF	Voltage at IREF input (pin 4)	VDD-3	VDD	V	4
IIN	Digital input current (any input)		±10	µA	5,6
IOZ	Off state digital output current		±50	µA	5,7
VOH	Output logic '1'	2.4		V	IO = -5mA
VOL	Output logic '0'		0.4	V	IO = 5mA

Notes (Notes 1, 2 and 3 apply to all parameters)

- 1 All voltages are with respect to GND unless specified otherwise.
- 2 The Pixel Clock frequency must be stable for a period of at least 20µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.
- 3 Over the range of the DC operating conditions unless specified otherwise.
- 4 These voltages apply equally for AVDD and VDD when using the PLCC packaged device.
- 5 VDD = max, GND ≤ VIN ≤ VDD.
- 6 On digital inputs (**P₀-P₇**, **PCik**, **RD**, **BLANK**, **WR** and **RS₀-RS₁**).
- 7 On digital input/output (**D₀-D₇**).

Average power supply current

	40MHz	50MHz	66MHz	80MHz	Units	Notes
IDD Max	155	160	190	210	mA	3
IDD Typ	130	135	145	150	mA	4,5
IDD Typ	70	75	85	90	mA	4,6

Notes (Notes 1 and 2 apply to all parameters)

- 1 The Pixel Clock frequency must be stable for a period of at least 20µs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.
- 2 Over the range of the DC operating conditions unless specified otherwise.
- 3 IO = IO(max) (see DAC characteristics, Section 8.6.3). IDD is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.
- 4 The IMS G176 color palette use the current switching method to control the DACs. Thus, the average current drawn is dependent on the intensity of the DACs at that time.
- 5 Typical IDD with IREF=10mA and with the DACs drawing full current (to display a white screen).
- 6 Typical IDD with IREF=10mA and DACs drawing minimum current (to display a black screen).

8.6.3 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
	Resolution	6			bits	
VO(max)	Output voltage			1.5	V	IO≤10mA
IO(max)	Output current			-21	mA	VO≤1V, note 4
IO	Full scale output current	-17.72	-18.65	-19.58	mA	
K	DAC gain constant		2.058			6
	Full scale error			±5	%	5
	DAC to DAC correlation error			±2	%	6
	Integral linearity error			±0.5	LSB	7
	Rise time (10% to 90%)			6	ns	8, IMS G176-66/80
	Rise time (10% to 90%)			8	ns	8, IMS G176-40/50
	Full scale settling time			12.5	ns	8,9,10, IMS G176-80
	Full scale settling time			15.3	ns	8,9,10, IMS G176-66
	Full scale settling time			20	ns	8,9,10, IMS G176-50
	Full scale settling time			25	ns	8,9,10, IMS G176-40
	Glitch energy		120		pVsec	8,10

Notes (Notes 1, 2 and 3 apply to all parameters)

- 1 All voltages are with respect to GND unless specified otherwise.
- 2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.
- 3 Tested over the operating temperature range and at nominal supply voltage with IREF = -9.07mA.
- 4 $IO = K \times IREF$
- 5 Full scale error from the value predicted by the DAC gain constant, K.
- 6 About the mid point of the distribution of the three DACs measured at full scale deflection.
- 7 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.
- 8 Load = 37.5Ω + 30pF with IREF = -9.07mA.
- 9 From a 2% change in the output voltage until settling to within 2% of the final value.
- 10 This parameter is sampled, not 100% tested.

8.6.4 AC test conditions

Parameter	
Input pulse levels	GND to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see Figure 8.6

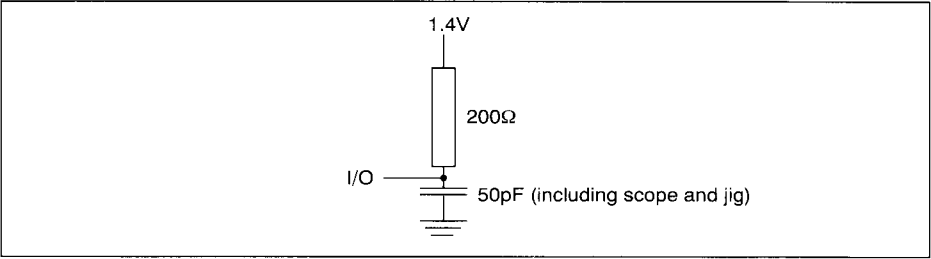


Figure 8.6 Digital output load

8.6.5 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes (Notes 1 and 2 apply to all parameters)

- 1 These parameters are sampled, not 100% tested.
- 2 Measured on a Boonton meter.
- 3 **RD** ≥ VIH(min) to disable **D0-D7**
- 4 **BLANK** ≤ VIL(max) to disable **RED, GREEN** and **BLUE**.

8.7 Package specifications

8.7.1 28 pin dual-in-line package

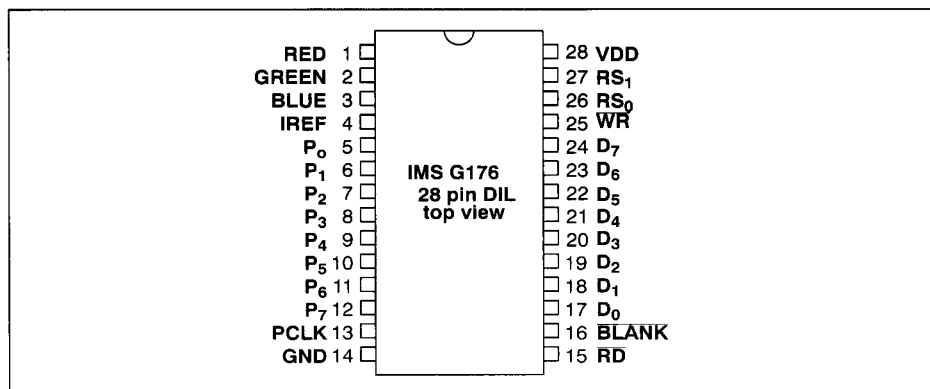


Figure 8.7 IMS G176 28 pin dual-in line package pinout

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.195	—	—	4.953
A1	0.015	—	—	0.381	—	—
A2	0.120	—	0.180	3.048	—	4.572
B	0.014	0.018	0.022	0.356	0.457	0.559
B1	0.045	0.055	0.065	1.143	1.397	1.651
C	0.008	0.010	0.012	0.203	0.254	0.305
D	1.366	1.450	1.470	34.696	36.830	37.338
E	0.583	—	0.625	14.808	—	15.875
E1	0.492	0.550	0.560	12.496	13.970	14.224
e	—	0.100BSC	—	—	2.540BSC	—
eA	—	0.600TYP	—	—	15.240TYP	—
e3	—	1.300BSC	—	—	33.020BSC	—
L	0.125	0.130	0.135	3.175	3.302	3.429
M	0 DEG	—	15 DEG	0 RAD	—	0.26 RAD
S	0.033	0.075	0.080	0.838	1.905	2.032

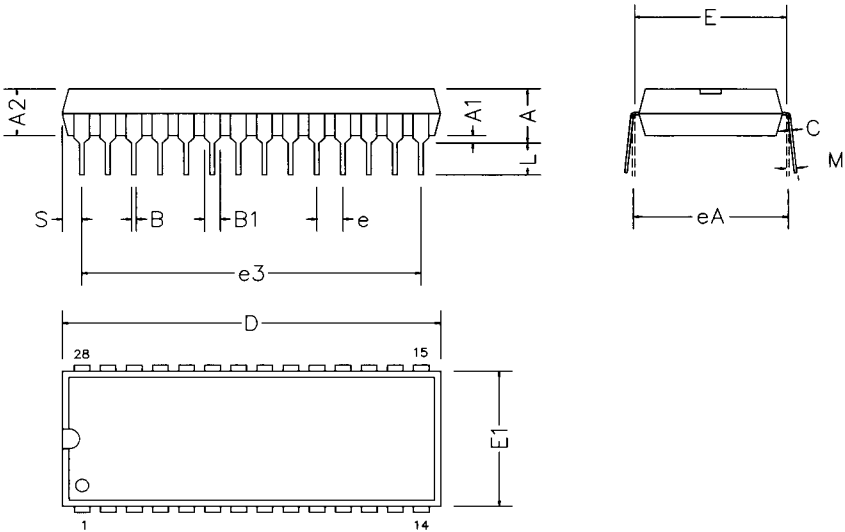


Figure 8.8 28 pin plastic dual-in-line package dimensions

8.7.2 32 pin plastic leaded-chip-carrier package

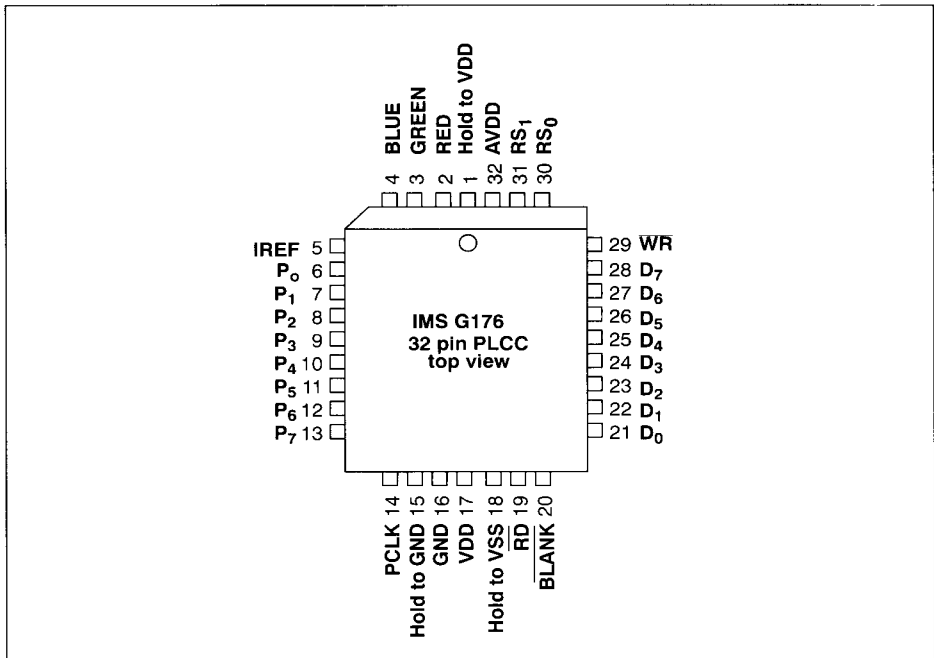
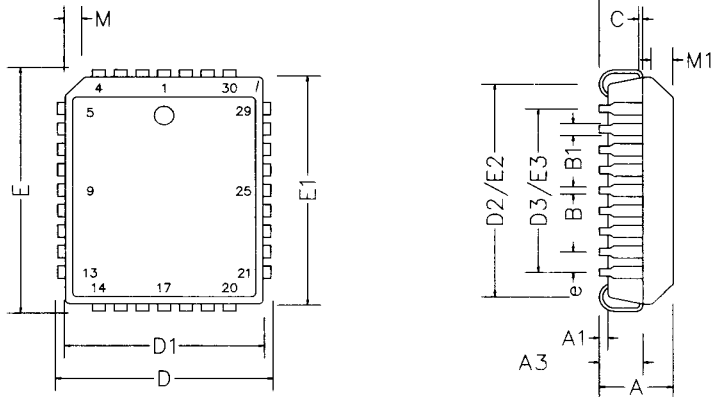


Figure 8.9 IMS G176 32 pin PLCC J-bend package pinout

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.123	0.130	0.140	3.124	3.302	3.556
A1	0.015	—	—	0.381	—	—
A3	0.078	—	0.095	1.981	—	2.413
B	0.013	—	0.023	0.330	—	0.584
B1	0.025	—	0.035	0.635	—	0.889
C	0.0095	0.010	0.0105	0.241	0.254	0.267
D	0.485	0.490	0.495	12.319	12.446	12.573
D1	0.449	0.455	0.460	11.405	11.557	11.684
D2	0.390	0.410	0.430	9.906	10.414	10.922
D3	—	0.300REF	—	—	7.620REF	—
E	0.585	0.590	0.595	14.859	14.986	15.113
E1	0.549	0.555	0.560	13.945	14.097	14.222
E2	0.490	0.520	0.530	12.446	13.208	13.462
E3	—	0.400REF	—	—	10.160REF	—
e	—	0.050BSC	—	—	1.270BSC	—
G	—	—	0.004	—	—	0.102
L	—	N/A	—	—	N/A	—
L1	—	N/A	—	—	N/A	—
M	0.042	—	0.048	1.067	—	1.219
M1	0.023	—	0.029	0.584	—	0.737

 G (Seating Plane Coplanarity)



Notes;

- 1. Maximum lead displacement from notional centre line = ± 0.007 ".

Figure 8.10 32 pin PLCC J-bend package dimensions

8.7.3 44 pin plastic leaded-chip-carrier package

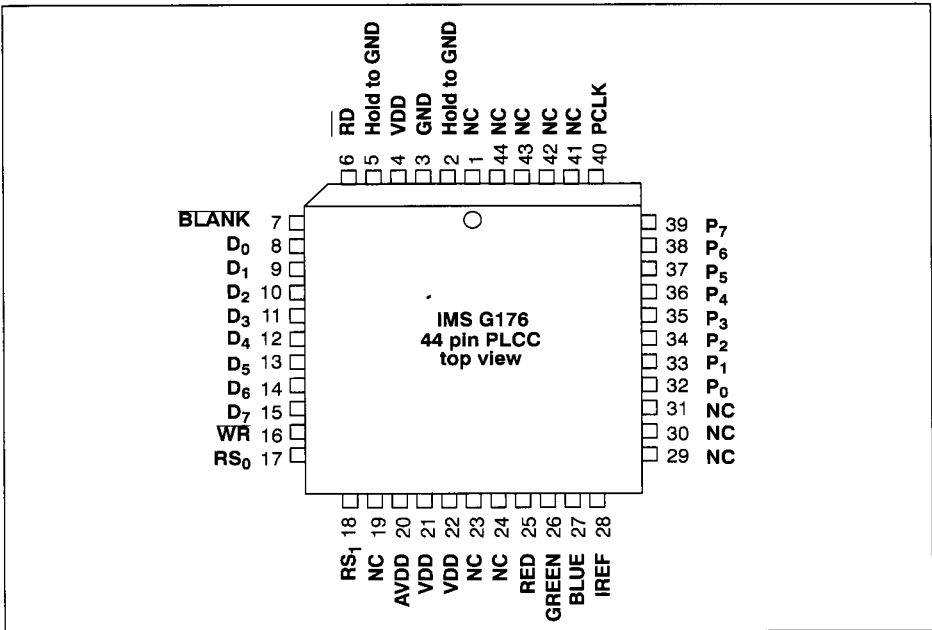
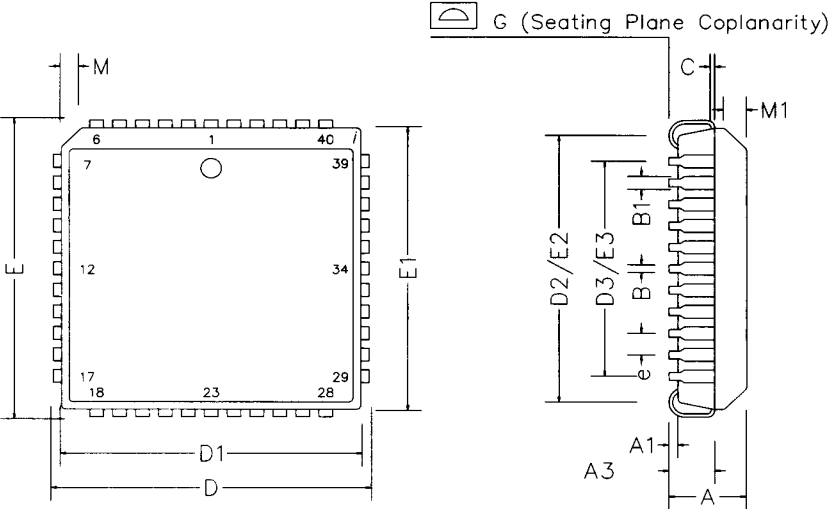


Figure 8.11 IMS G176 44 pin PLCC J-bend package pinout

Note

All **VDD** pins **must** be connected to the 5 Volt power supply.
All **GND** pins **must** be connected to ground.

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.165	0.170	0.180	4.191	4.318	4.572
A1	0.020	—	—	0.508	—	—
A3	0.095	—	0.110	2.413	—	2.794
B	0.013	—	0.023	0.330	—	0.584
B1	0.025	—	0.035	0.635	—	0.889
C	0.0095	0.010	0.0105	0.241	0.254	0.267
D	0.685	0.690	0.695	17.399	17.526	17.653
D1	0.650	0.655	0.660	16.510	16.637	16.764
D2	0.590	0.610	0.630	14.986	15.494	16.002
D3	—	0.500REF	—	—	12.700REF	—
E	0.685	0.690	0.695	17.399	17.526	17.653
E1	0.650	0.655	0.660	16.510	16.637	16.764
E2	0.590	0.610	0.630	14.986	15.494	16.002
E3	—	0.500REF	—	—	12.700REF	—
e	—	0.050BSC	—	—	1.270BSC	—
G	—	—	0.004	—	—	0.102
L	—	N/A	—	—	N/A	—
L1	—	N/A	—	—	N/A	—
M	0.042	—	0.048	1.067	—	1.219
M1	0.042	—	0.056	1.067	—	1.422



- Notes;
1. Maximum lead displacement from notional centre line = $\pm 0.007''$.

Figure 8.12 44 pin PLCC J-bend package dimensions

8.8 Ordering information

Device	Clock rate	Package	Part number
IMS G176	40MHz	28 pin Plastic DIP	IMS G176P-40SF
IMS G176	50MHz	28 pin Plastic DIP	IMS G176P-50SF
IMS G176	66MHz	28 pin Plastic DIP	IMS G176P-66SF
IMS G176	80MHz	28 pin Plastic DIP	IMS G176P-80SF
IMS G176	40MHz	32 pin Plastic LCC	IMS G176J-40SF
IMS G176	50MHz	32 pin Plastic LCC	IMS G176J-50SF
IMS G176	66MHz	32 pin Plastic LCC	IMS G176J-66SF
IMS G176	80MHz	32 pin Plastic LCC	IMS G176J-80SF
IMS G176	40MHz	44 pin Plastic LCC	IMS G176J-40ZF
IMS G176	50MHz	44 pin Plastic LCC	IMS G176J-50ZF
IMS G176	66MHz	44 pin Plastic LCC	IMS G176J-66ZF
IMS G176	80MHz	44 pin Plastic LCC	IMS G176J-80ZF

Note: IMS G176J units can be supplied mounted on tape and reel.