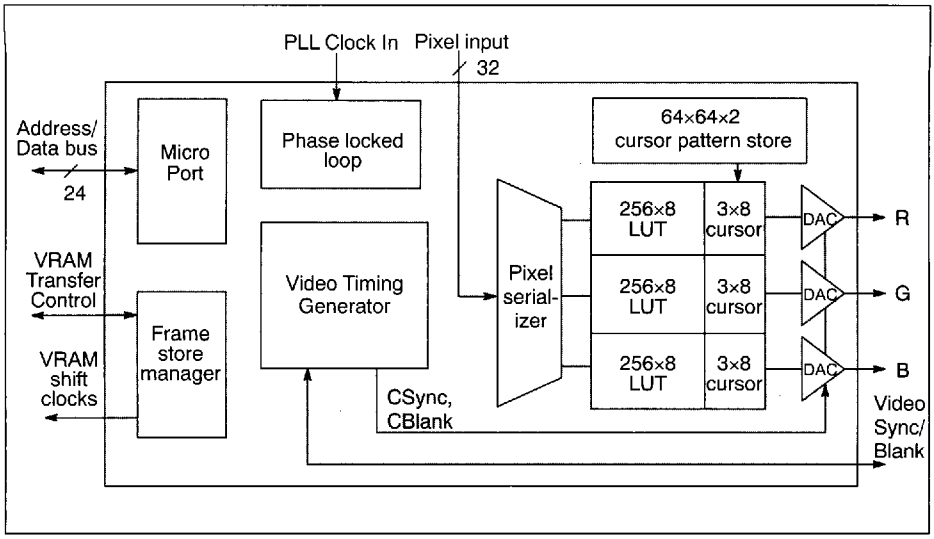
SGS-THOMSON MICROELECTRONICS

IMS G332

COLOR VIDEO CONTROLLER

PRODUCT OVERVIEW



FEATURES

Video rates up to 110MHz
1, 2, 4 and 8 bit pseudo color pixels
15 or 16 bit true color with gamma correction
Software configurable video timing generator
Comprehensive video RAM framestore manager
On-chip phase-locked loop pixel clock generator
64×64 pixel ×3 color hardware cursor
Triple 8 bit DACs
Triple 256×8 anti-sparkle look-up RAM

BENEFITS

Reduced component count
Reduced system power consumption
Enhanced system flexibility
Easy upgradeabilty
Broadcast standards compliance
All digital signals below RFI regulated frequency
Software compatible with IMS G364

APPLICATIONS

High resolution graphics and imaging
Broadcast/CC television systems
Multimedia
Graphical user interfaces
X-terminals
Low cost workstations

DESCRIPTION

The IMS G332 is a high performance CMOS device which integrates all the subsystem functions required to control high resolution color graphics displays.

This device has now been superseded by the IMS G335, which is a drop-in replacement offering higher performance and greater ease of design.

The IMS G335 is recommended for all new designs. Full engineering data on the IMS G332 is still available from your local sales office if required.

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12.1 Introduction

The IMS G332 provides all the necessary functions to control real-time operation of a raster scan video display, using dual-ported video RAMs.

The device consists of a 32 bit variable format multiplexed pixel interface, a programmable video timing generator (VTG), a 256 location color lookup table (LUT) with variable addressing modes, triple 8 bit video Digital-to-Analogue Convertors (video DACs), a 64×64×2 bit cursor store and 3 location cursor LUT, a programmable cursor positioning/insertion controller, a video memory control system and phase-locked loop clock generator.

A brief description of each functional block follows, for more detailed information please refer to the relevant section in the full datasheet.

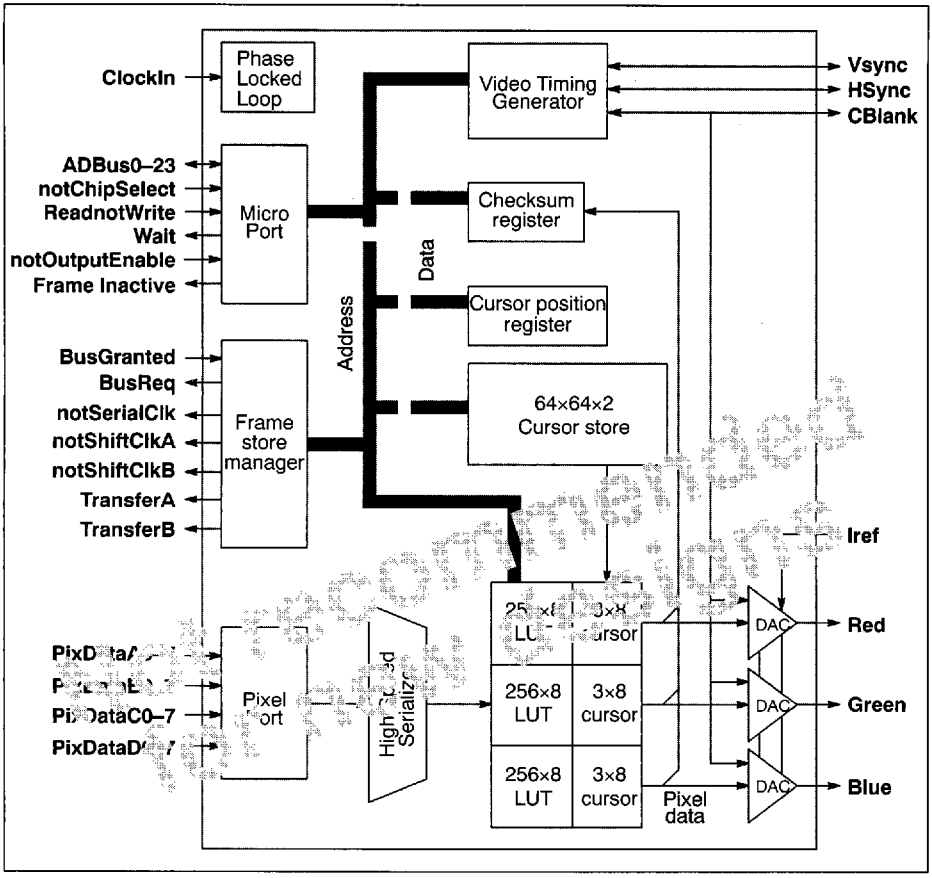

Figure 12.1 IMS G332 Block Diagram

12.1.1 Clocks

An on-chip phase-locked loop clock generator allows the IMS G332 to be driven from a low speed clock in the 5MHz to 10MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL.

12.1.2 Micro Port

The entire IMS G332 register space is read/write accessible via the micro port. This is a 24 bit wide synchronous interface, with multiplexed address and data, for single-cycle access to all registers. A wait pin is provided to allow synchronization between the IMS G332 clock regime and that of the processor or interface bus. This interface is also used to provide the VRAM shift register transfer address.

12.1.3 Video timing generator

The video timing generator is a programmable finite state machine which uses a set of screen description parameters to produce the monitor sync and DAC blanking signals as well as the video RAM shift clock signals. It can be configured to be the system master or, as a slave, to lock onto an external signal which is already synchronous or has been previously genlocked. This may be from another INMOS CVC, giving the potential for multiple, synchronous video systems. The timing generator runs at one quarter of the video dot rate and the screen description parameters therefore have a resolution of four pixel periods.

12.1.4 Framestore manager

All the requirements of supporting a video RAM framestore are met by the IMS G332. The Framestore manager uses two framestore description parameters to maintain a constant supply of pixels to the pixel interface. It supports synchronous reload by supplying the refresh address and the transfer strobes, synchronized to the VRAM SC signals, so that a packed pixel framestore can be implemented regardless of the variations in screen format and framestore architecture. The refresh address generator supports all current VRAM standards together with the NTSC and PAL/SECAM screen formats.

12.1.5 Pixel Port

High pixel rates are achieved by multiplexing the video RAM serial outputs into a 32-bit wide pixel port. The IMS G332 supplies the shift clock signal, automatically adjusting its frequency, along with the multiplex ratio of the port, according to the bits per pixel mode selected. The minimum acceleration ratio is 4:1. achieved in 15 and 16bits per pixel (bpp) mode by the use of an interleaved memory system, for whic' all the necessary signals are supplied.

12.1.6 Hardware Cursor

The hardware cursor is a complete system. The cursor store and lookup table are memory mapped, its position being modified by a single register access which can occur at any time, becoming valid at the next frame scan. The cursor position is stored in 2's complement relative to the top left pixel on the screen and is independent of monitor specifications.

12.1.7 Anti-sparkle Color Palette

The serialized pixels are used as addresses into a triple 256×8 pipelined RAM. In pseudo color modes one address is applied to all three RAMs giving a maximum of 256 simultaneous colors out of a possible 16·7 million. In true color each RAM is independently addressed for gamma correction of up to 64 thousand simultaneous colors. The palette has an anti-sparkle mechanism which reduces the visible effect of palette updates during display.

12.1.8 Video DACs

The three 8-bit DACs drive RS-170 level signals directly into a 37.5Ω load. They are blanked with programmable setup, internally by the VTG, externally by the **CBlank** pin or by a combination of the two. Composite Sync may be added to all three DACs.

12.1.9 System operation

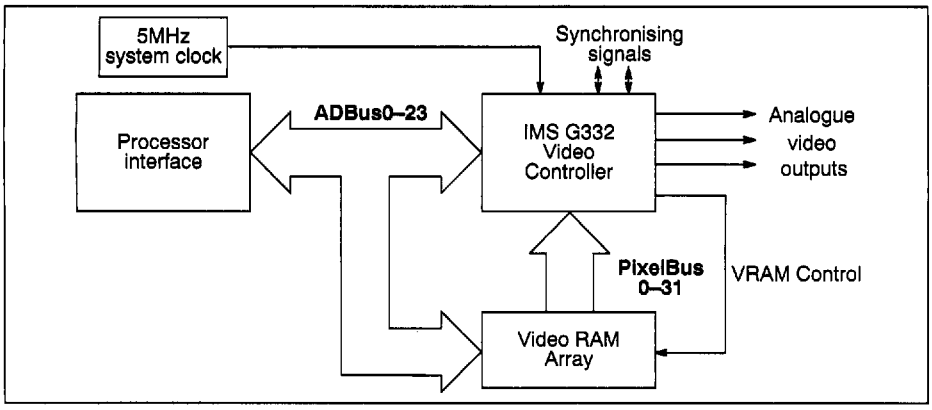

Figure 12.2 IMS G332 operating in a simple graphics system

Figure 12.2 shows how the IMS G332 would fit into a typical single-bitmap display system. The clock is typically sourced from a 5MHz crystal, with the video data being streamed to the screen at the full video rate of up to 110MHz. The video RAM array is directly accessed by the processor, with screen management automatically being performed by the IMS G332. All external digital signals and clocks are running at one quarter of the video rate, alleviating problems of high speed system design.

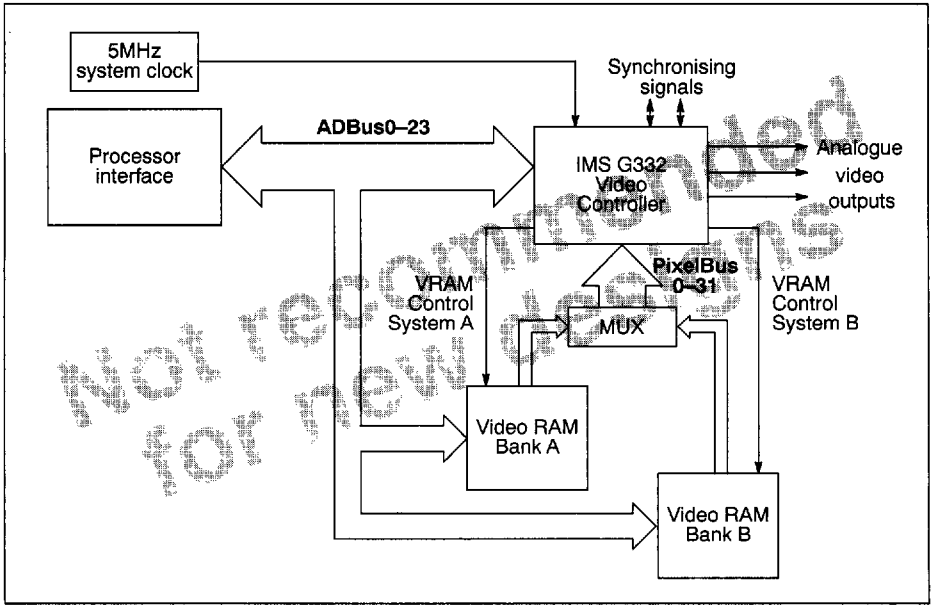

Figure 12.3 IMS G332 operating with an interleaved memory system

Figure 12.3 shows the organization of an interleaved framestore. The IMS G332 accepts alternate loads from each bank in turn through an external multiplexor (or if the video rate is low enough - about 85MHz - the VRAM serial output enables can be used instead of external hardware). The IMS G332 supplies all the controls required to implement this architecture.

12.2 Package specifications

100 pin ceramic quad flatpack package

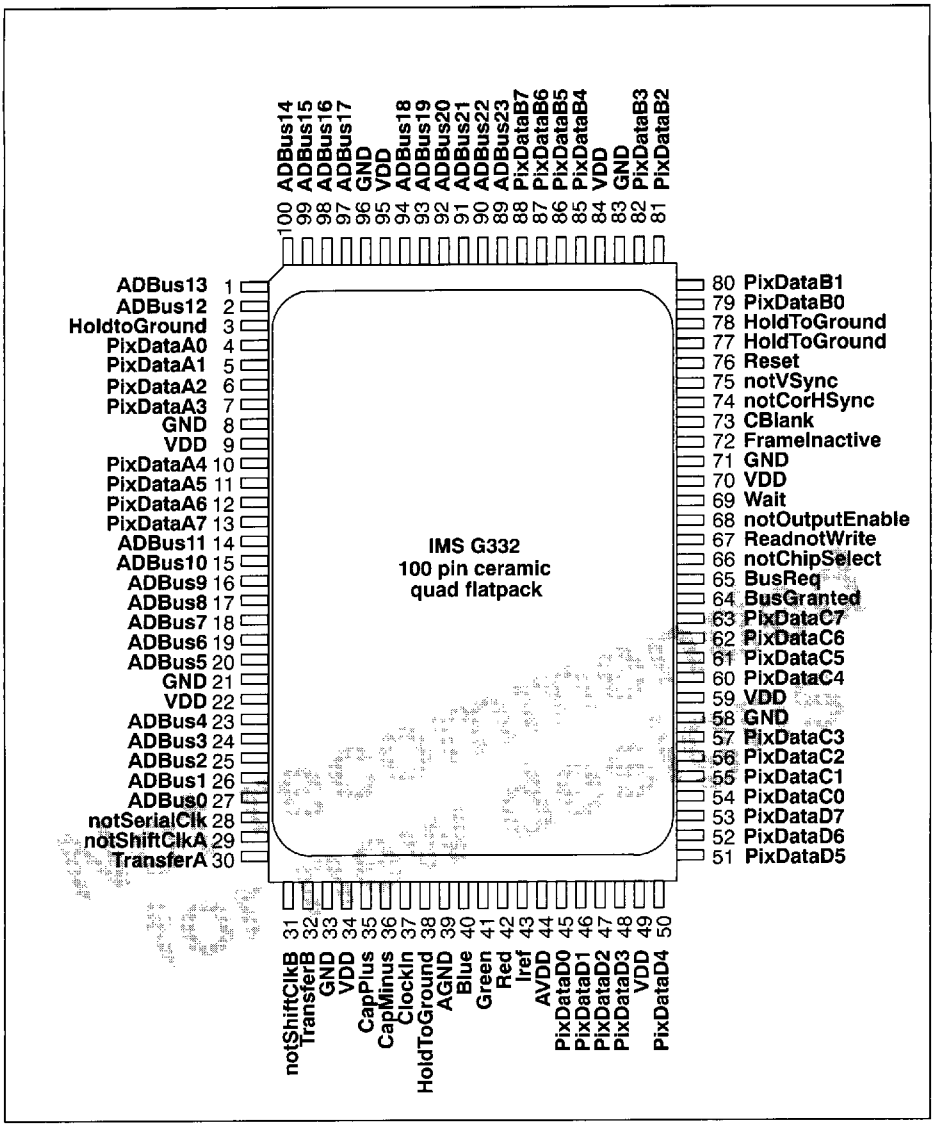

Figure 12.4 IMS G332 pin configuration

DIM	CONTROL DIMENSIONS mm Min	Nom	Max	ALTERNATIVE DIMENSIONS INCH Min	Nom	Max
A			3.400			0.134
A_1	0.250			0.010		
A_2			3.073			0.121
D	23.65	23.90	24.15	0.931	0.941	0.951
D_1	19.80	20.00	20.20	0.780	0.787	0.795
D_3		18.85 REF			0.742 REF	
E	17.65	17.90	18.15	0.695	0.705	0.715
E_1	13.84	14.00	14.15	0.545	0.551	0.557
E_3		12.35 REF			0.486 REF	
L	0.650	0.800	0.950	0.026	0.031	0.037
e		0.650 BSC			0.026 BSC	
B	0.22		0.38	0.009		0.015

Notes

1 Dimension D1 and E1 measured at the ceramic side. Base to window frame misalignment is 0.40mm max. An additional glass meniscus of 0.2mm max is allowed at the leadframe interface.

2 Coplanarity 0.1 mm Max

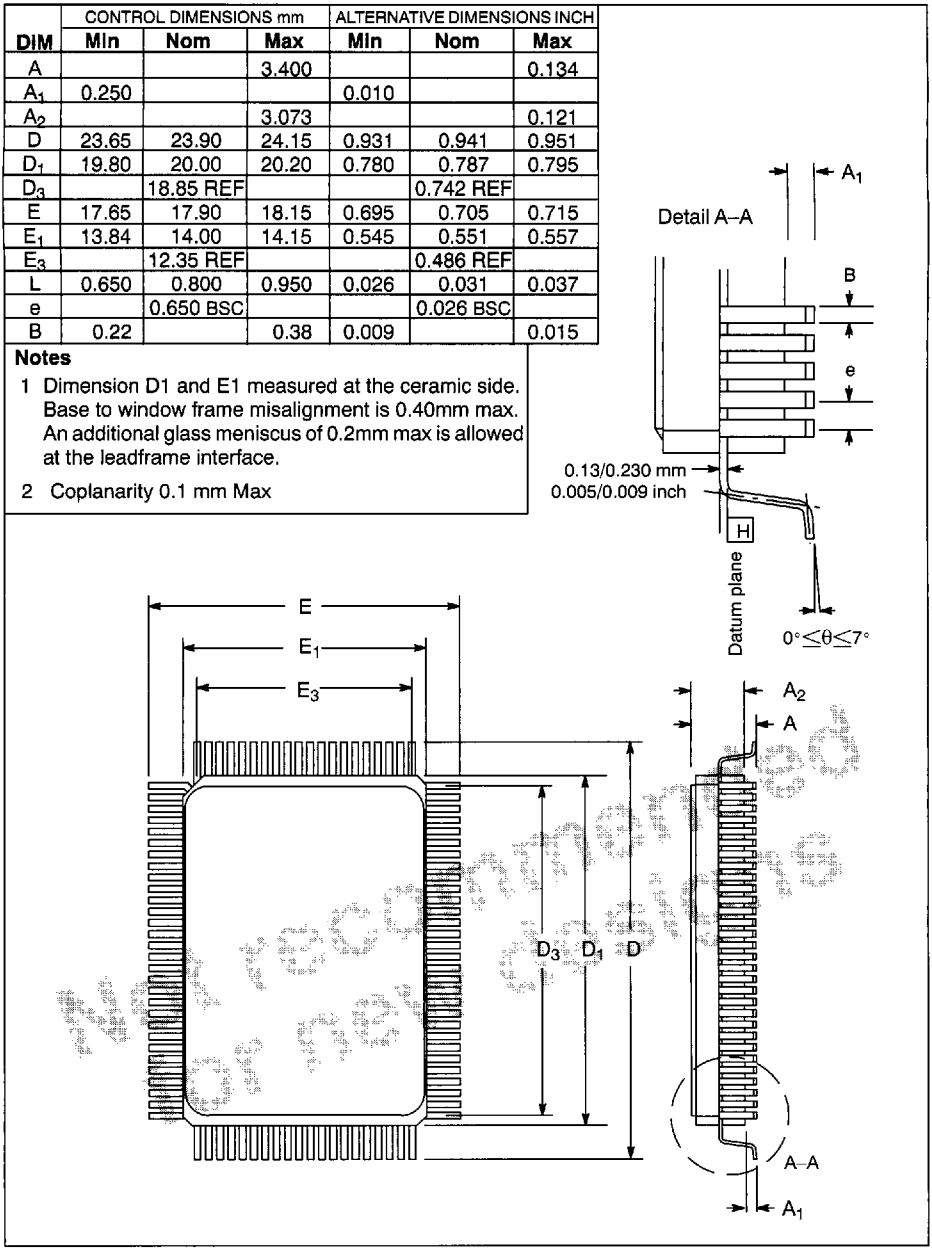

Figure 12.5 100 pin ceramic quad flat pack dimensions (cavity-up)

12.3 Ordering information

Device	Clock rate	Package	Part number
IMS G332	85 MHz	100 pin ceramic quad flatpack	IMS G332F-85S
IMS G332	100 MHz	100 pin ceramic quad flatpack	IMS G332F-10S
IMS G332	110 MHz	100 pin ceramic quad flatpack	IMS G332F-11S