Electrical Specification

Absolute Maximum Ratings (1)

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	-0.3 to +7.0	V
V_{IN}	Input Voltage (2)	-0.3 to V_{DD}+0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{SINK}	Sink Current per Pin	150	mA

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	+4.75 to +5.25	V
T_A	Operating Temperature	0 to +70	°C
R_{OD} (3)	External Resistance	11.4K to 12.6K	Ω
R_{ID} (3)	External Resistance	11.4K to 12.6K	Ω
R_{PU} (3)	External Resistance	11.4K to 12.6K	Ω

Capacitance (4)

Symbol	Parameter	Limits	Units
C_{IN}	Input Capacitance (JTAG, OE , CLK pins)	5	pF
C_{OUT}	Output Capacitance (TDO pin)	8	pF
C_{PORT}	I/O Port Capacitance	8	pF

Notes:
(1) Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A maximum overshoot and undershoot of 2V for a maximum duration of 20ns is acceptable.
(3) Required for IQ320 and IQ240B only.
(4) Capacitance measured at 25°C. Sample-tested only.

DC Specifications (T_A = 0°C to 70°C, V_{DD} = 5V ± 5%)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High-Level Input Voltage		2.0	V_{DD}+0.3	V
V_{IL}	Low-Level Input Voltage		- 0.3	0.8	V
V_{OH}	High-Level Output Voltage (1)	V_{DD} = Min, I_{OH} = - 8 mA	2.4	-	V
V_{OL}	Low-Level Output Voltage	V_{DD} = Min, I_{OL} = 16 mA	-	0.4	V
$\|I_{IL}\|$ $\|I_{IH}\|$	Input Leakage Current	V_{DD} = Max, $0 \le V_{IN} \le V_{DD}$	-	5	µA
$\|I_{OZ}\|$	Tristate Output Off-State Current	V_{DD} = Max, $0 \le V_{IN} \le V_{DD}$	-	5	µA
$I_{PU\text{-}LO}$	Programmed-Low Additional Bus-Repeater Current (2)	V_{DD} = Min, V_O = GND	2.4	3.6	mA
$I_{PU\text{-}HI}$	Programmed-High Additional Bus-Repeater Current (2)	V_{DD} = Min, V_O = GND	16	24	mA
I_{OS}	Short Circuit Current (1, 2, 3)	V_{DD} = Max, V_O = GND	-60	-	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max, Freq = 0 MHz, No Load, $0 \le V_{IN} \le V_{DD}$	-	8.0	mA
Q_{DDD}	Dynamic Power Supply Current per Input per MHz (2)	V_{DD} = Max, No Load, Connect one output per input, Toggle one input @ 50% duty cycle with all other inputs at GND or V_{DD}	-	0.3	mA/ MHz

Notes:
(1) For TTL output mode.
(2) These parameters are guaranteed but not tested in production.
(3) No more than one output should be tested at a time, and the duration of the test should be less than one second.

AC Specifications (T_A = 0°C to 70°C, V_{DD} = 5V ± 5%)

Symbol	Parameter	Speed Grade	-10		-12		-15		-20		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	One Way Signal Propagation Delay Time		-	10	-	12.5	-	15	-	20	ns
$t_{P\Delta}$	Additional Delay per Additional Output Port up to 16 Output Ports (1)		-	1	-	1	-	1	-	1	ns
t_{SK}	Skew Between Output Ports (1)		-	1.5	-	1.5	-	1.5	-	1.5	ns
R_{DATA}	NRZ Data Rate (1)		-	160	-	133	-	100	-	80	Mbs
t_{W+}	Positive Input signal Pulse Width		6	-	7	-	9	-	11	-	ns
t_{W-}	Negative Input signal Pulse Width		6.5	-	8	-	11	-	13	-	ns
t_{PZL}, t_{PZH}	Output Enable to Data Valid Time		-	10	-	12.5	-	15	-	20	ns
t_{PLZ}, t_{PHZ}	Output Disable to Output at High Z Time (1)		-	10	-	12.5	-	15	-	20	ns
f_{RI}	Register Input Clock Frequency (1)		-	100	-	80	-	66	-	50	MHz
t_{W-RI}	Register Input Clock Pulse Width, Low or High		5	-	6	-	7	-	9	-	ns
t_{S-RI}	Register Input Setup Time		0	-	0	-	0	-	0	-	ns
t_{H-RI}	Register Input Hold Time		2	-	2	-	2	-	2	-	ns
t_{P-RI}	Register Input Clock to Output Data Valid		-	16	-	18.5	-	22	-	28	ns
f_{RO}	Register Output Clock Frequency (1)		-	80	-	66	-	50	-	40	MHz
t_{W-RO}	Register Output Clock Pulse Width, Low or High		6	-	7	-	10	-	12	-	ns
t_{S-RO}	Register Output Setup Time		6	-	7	-	8	-	9	-	ns
t_{H-RO}	Register Output Hold Time		0	-	0	-	0	-	0	-	ns
t_{P-RO}	Register Output Clock to Data Valid		-	10	-	12.5	-	15	-	20	ns
f_{RIO}	Register Input/Output Clock Frequency (1)		-	100	-	80	-	66	-	50	MHz
t_{W-RIO}	Register Input/Output Clock Pulse Width, Low or High		5	-	6	-	7	-	9	-	ns
t_{S-RIO}	Register Input/Output Setup Time		0	-	0	-	0	-	0	-	ns
t_{H-RIO}	Register Input/Output Hold Time		2	-	2	-	2	-	2	-	ns
t_{P-RIO}	Register Input/Output Clock to Data Valid		-	10	-	12.5	-	15	-	20	ns
t_{SK-ZC}	ICLK/OCLK skew for zero clock delay output (1)		7	-	8	-	9	-	10	-	ns
t_{SK-OC}	ICLK/OCLK skew for one clock delay output (1)		-	4.5	-	5	-	5.5	-	6	ns
f_{JTAG}	JTAG Clock (TCK) Frequency		-	20	-	20	-	20	-	20	MHz
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width, Low or High		25	-	25	-	25	-	25	-	ns
t_{S-JTAG}	JTAG Setup Time		15	-	15	-	15	-	15	-	ns
t_{H-JTAG}	JTAG Hold Time		15	-	15	-	15	-	15	-	ns
t_{P-JTAG}	JTAG Clock to Output Valid		15	-	15	-	15	-	15	-	ns
f_{RC}	Rapid Connect Strobe Frequency (1)		-	25	-	25	-	25	-	25	MHz
F_{RC}	Rapid Connect Strobe Period		40	-	40	-	40	-	40	-	ns
t_{W-RC}	Rapid Connect Strobe Pulse Width		20	-	20	-	20	-	20	-	ns
t_{S-RC}	Rapid Connect Address and Data Set up Time		15	-	15	-	15	-	15	-	ns
t_{H-RC}	Rapid Connect Address and Data Hold Time		20	-	20	-	20	-	20	-	ns
t_{P-RC}	Rapid Connect Strobe Falling Edge to Data Valid for Making Connection or to Data Invalid for Breaking Connection		35	-	35	-	35	-	35	-	ns

Notes:
(1) These parameters are guaranteed but not tested in production.

Timing Diagrams

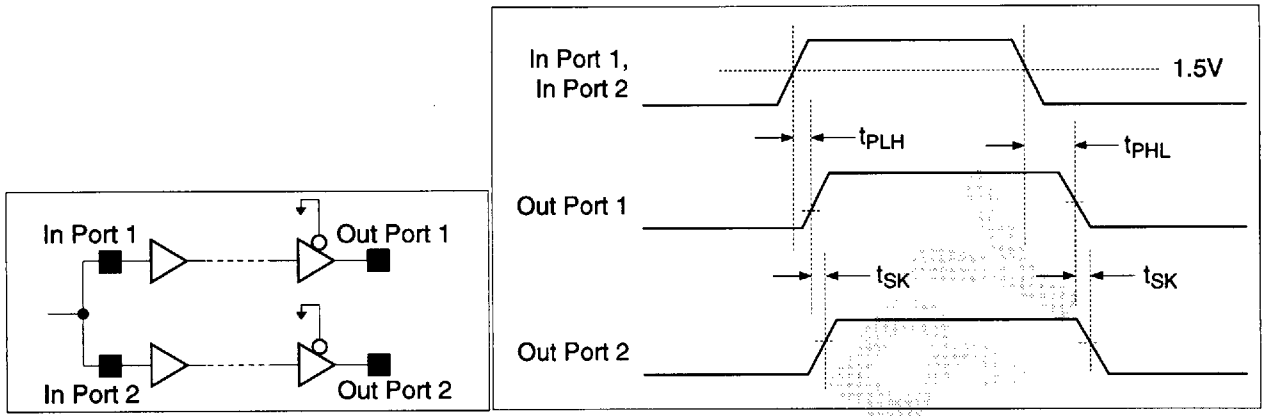


Figure 4a: I/O Port Timing (Flow-through Mode)

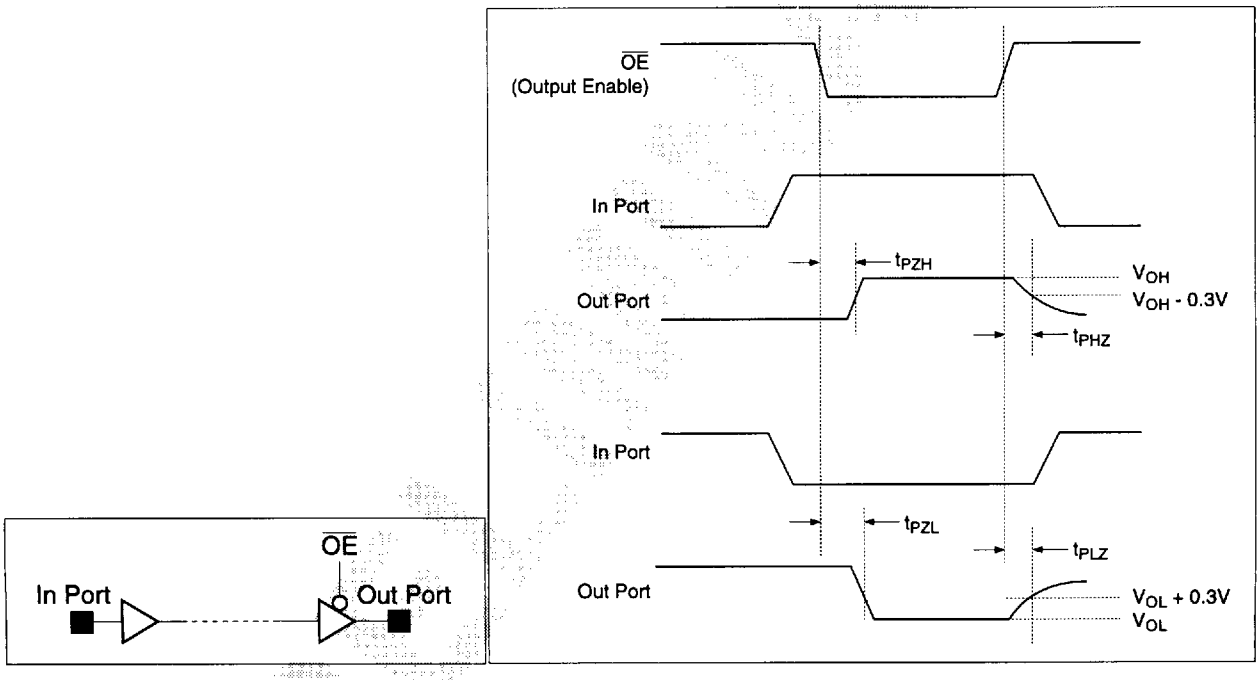


Figure 4b: Output Enable Timing (Flow-through Mode)

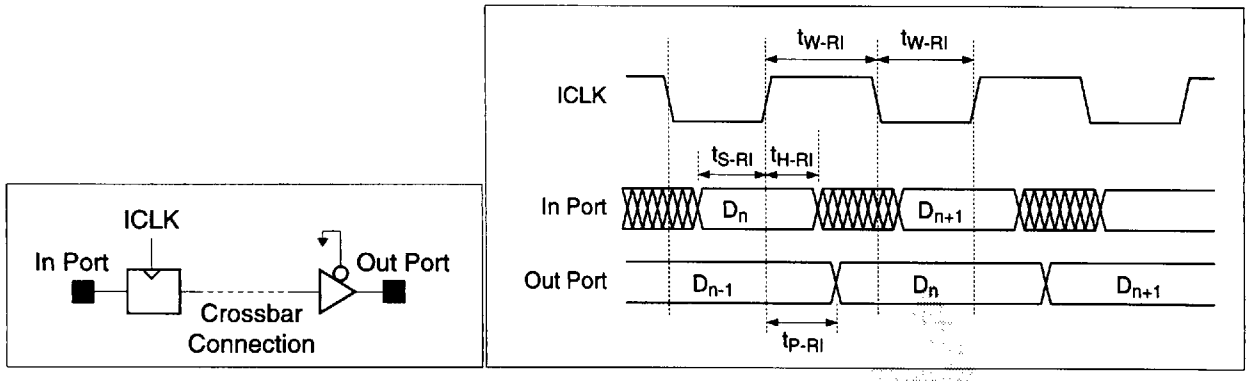


Figure 5a: Clocked Input to Unclocked Output

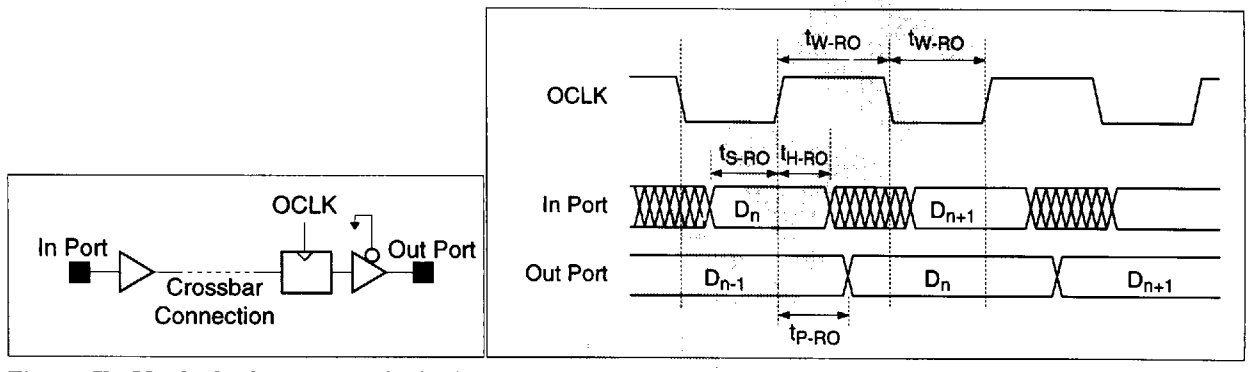


Figure 5b: Unclocked Input to Clocked Output

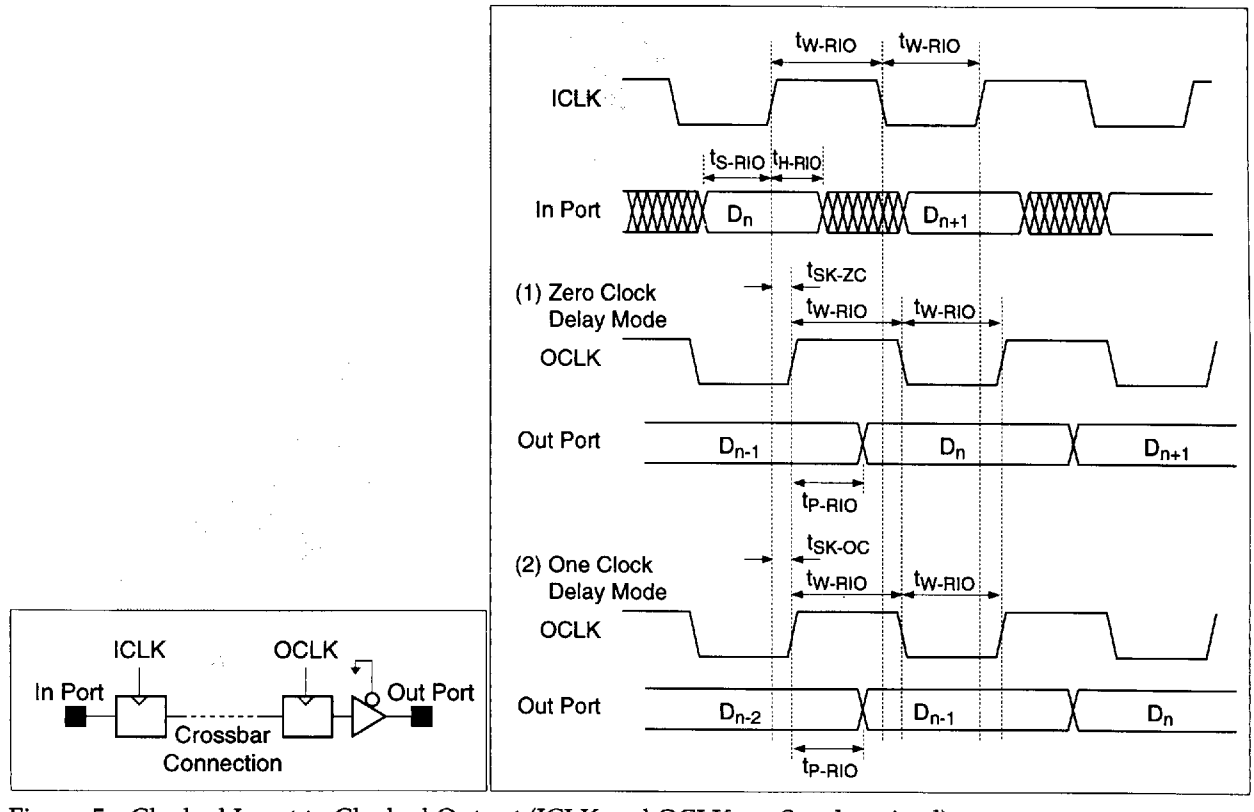


Figure 5c: Clocked Input to Clocked Output (ICLK and OCLK are Synchronized)

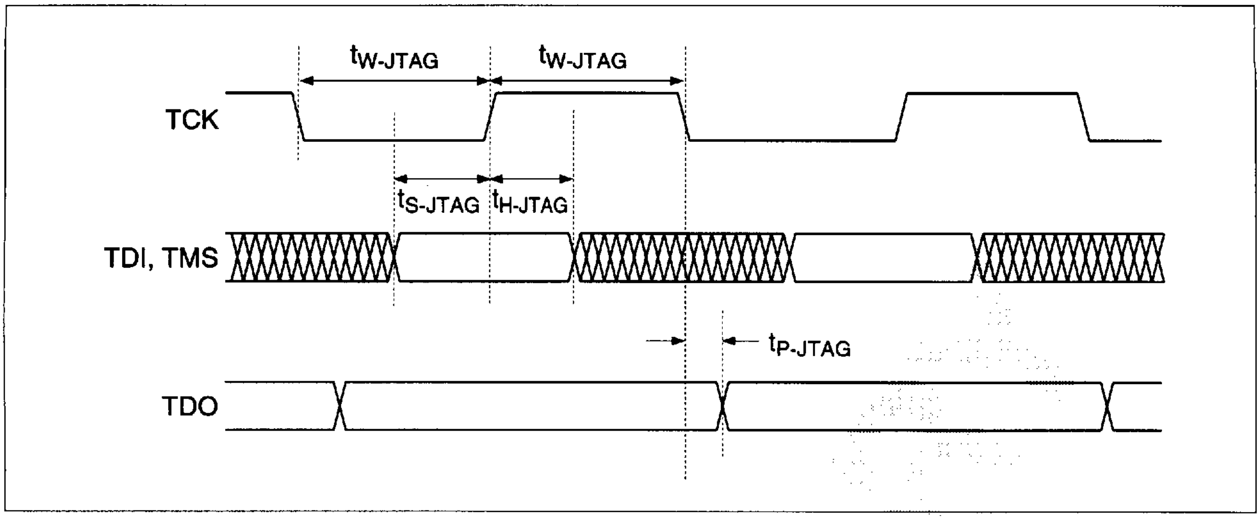


Figure 6: JTAG Timing

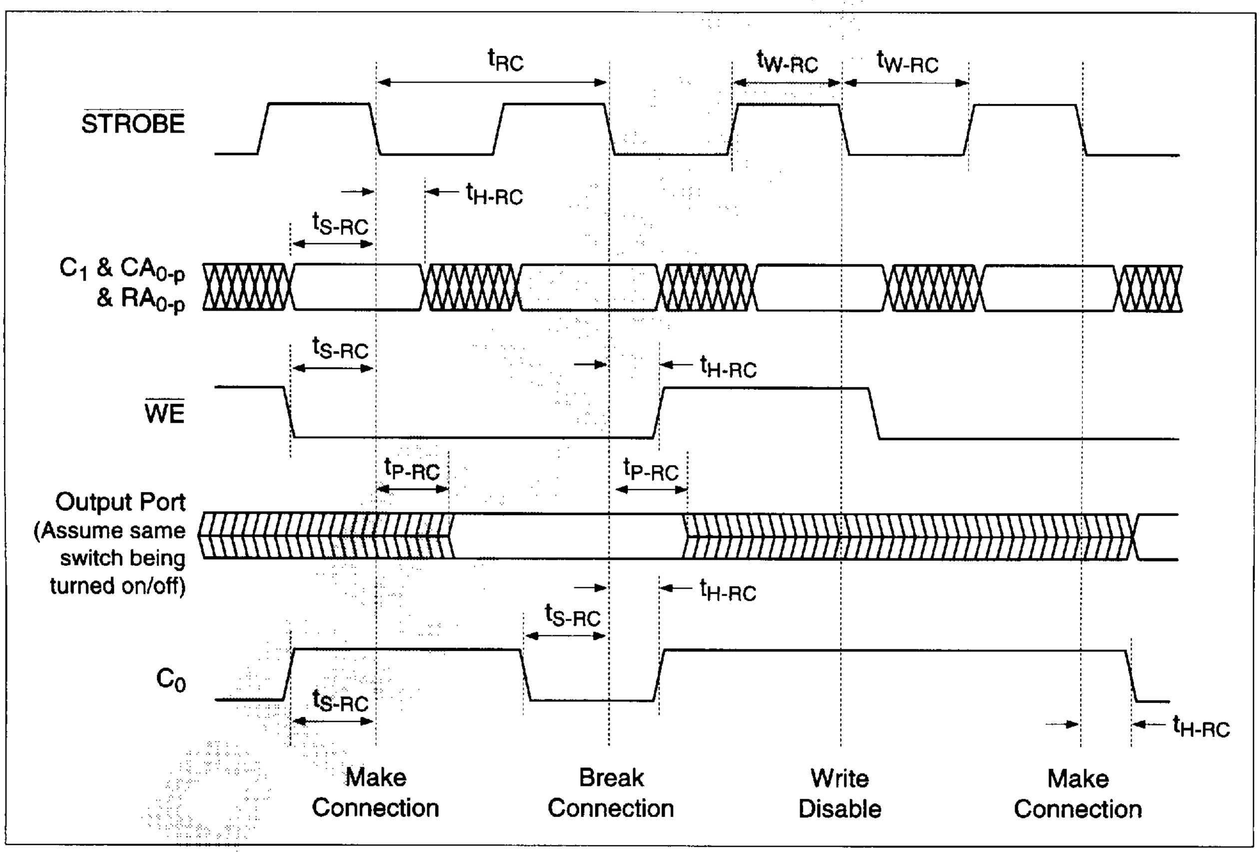
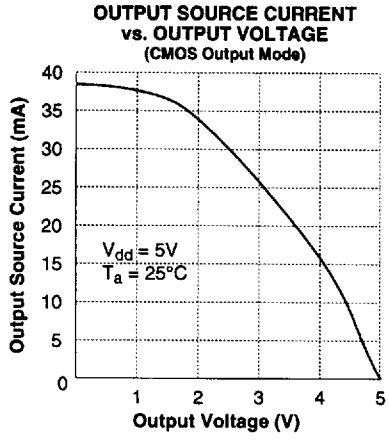
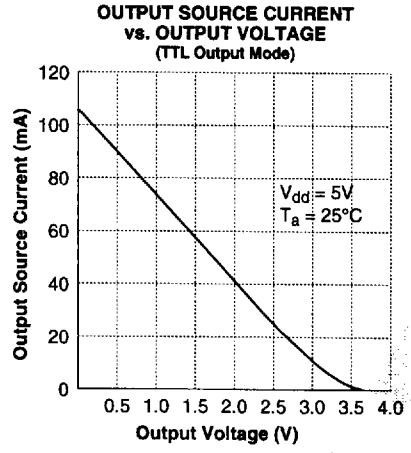
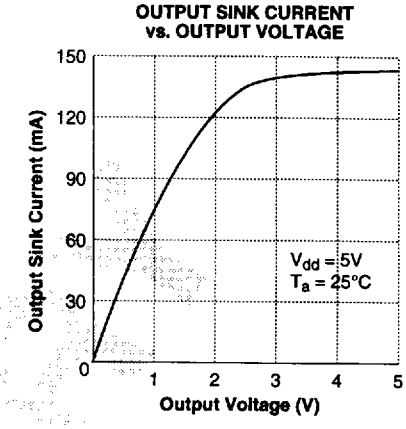


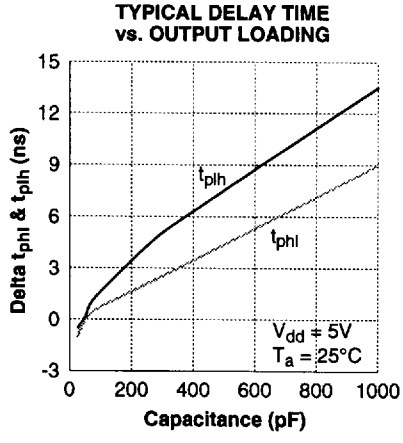
Figure 7: RapidConnect Timing

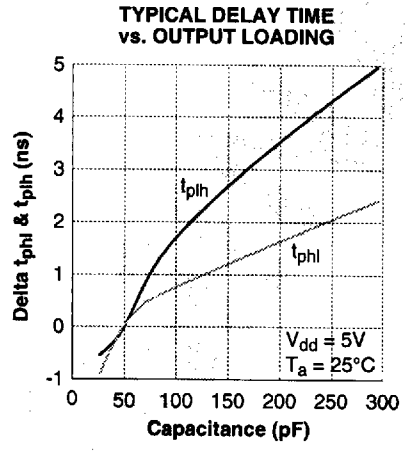
Typical AC and DC Characteristics (Measured for IQ320 and IQ240B)

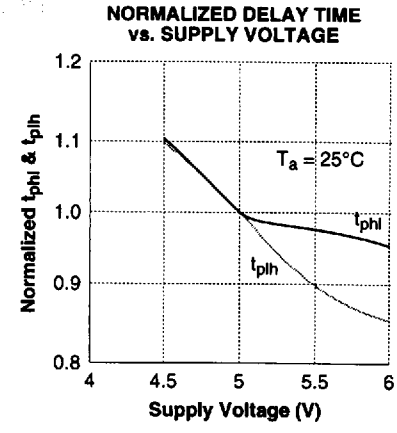


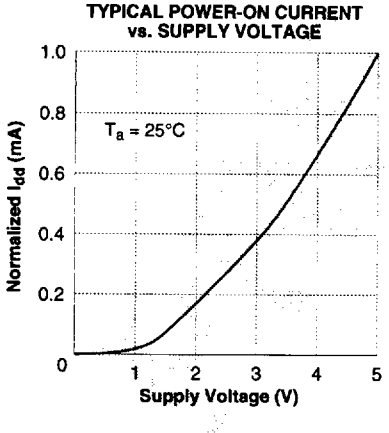


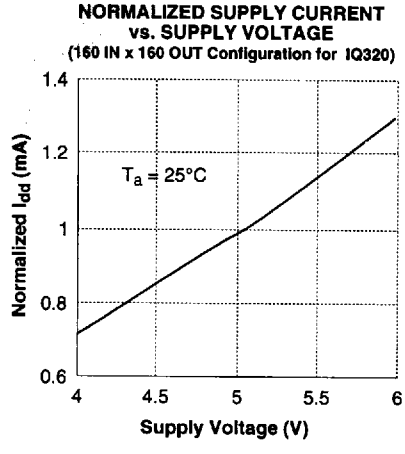


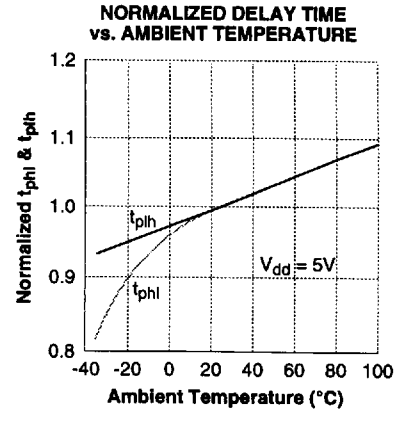












Mechanical Specifications

Package Dimensions

Mechanical specifications for a PPGA/391L package for IQ320, MQFP/304L package for IQ240B, MQFP/208L package for IQ160, MQFP/184L package for IQ128B and MQFP/144L package for IQ96B are shown on the following pages. Data for the other package types will be available at a later date. Contact I-Cube Marketing for more information.

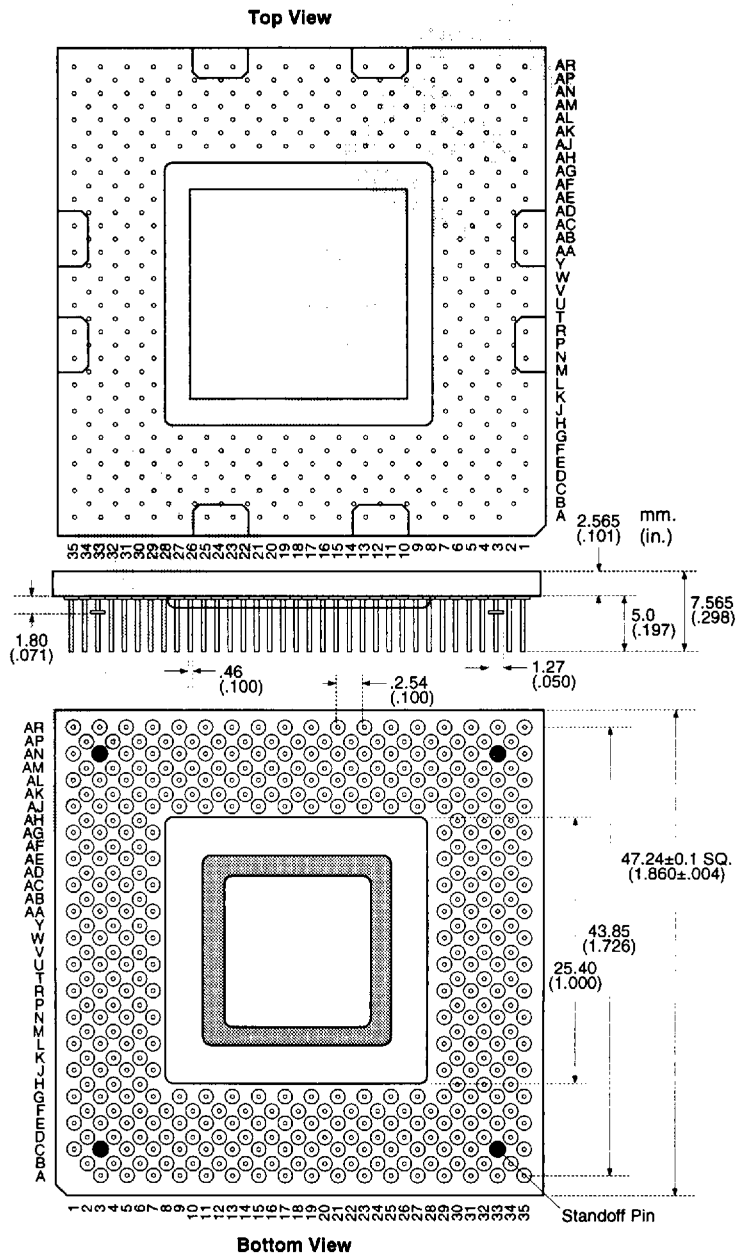


Figure 8: IQ320 [PPGA/391L] Package Dimensions

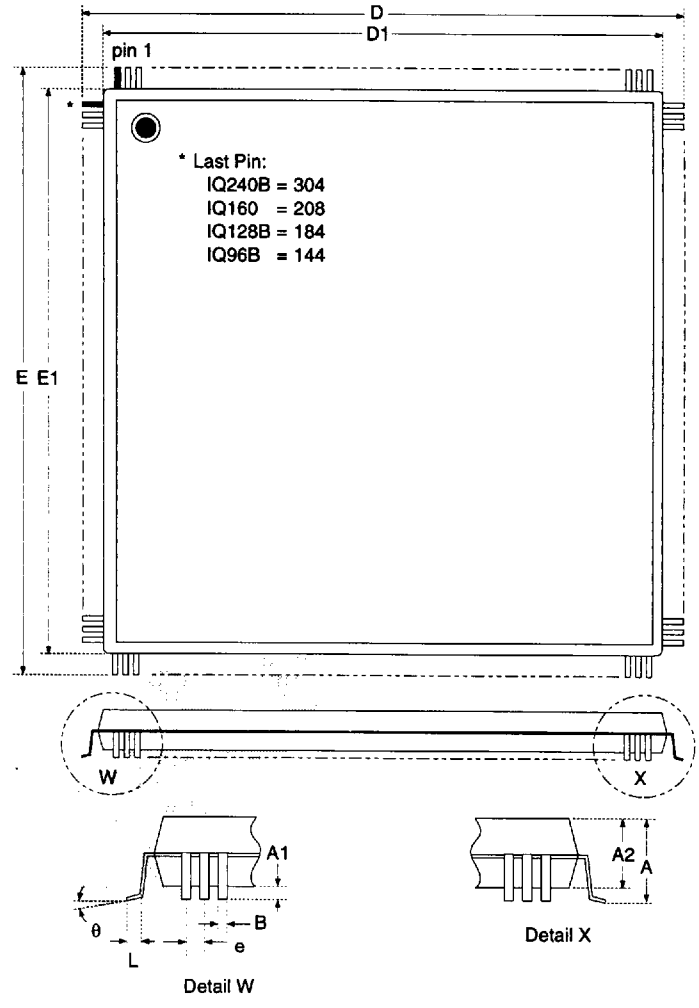


Figure 9: MQFP† Package Dimensions

Package Dimension Table		MQUAD/304L		MQUAD/208L		MQUAD/184L		MQUAD/144L	
		inch	mm	inch	mm	inch	mm	inch	mm
A	max	0.172	4.38	0.156	3.96	0.156	3.96	0.152	3.96
A1	min	0.010	0.25	0.014	0.35	0.014	0.35	0.014	0.35
	max	0.020	0.51	0.021	0.53	0.021	0.53	0.021	0.53
A2	min	0.144	3.66	0.125	3.18	0.125	3.17	0.125	3.17
	max	0.154	3.92	0.135	3.43	0.135	3.43	0.135	3.43
B	min	0.007	0.18	0.006	0.15	0.006	0.16	0.009	0.22
	max	0.011	0.28	0.011	0.28	0.011	0.27	0.014	0.35
D	min	1.669	42.46	1.197	30.45	1.220	31.00	1.219	30.95
	max	1.685	42.87	1.213	30.86	1.236	31.40	1.238	31.45
D1	min	1.558	39.64	1.086	27.63	1.086	27.59	1.086	27.59
	max	1.566	39.84	1.094	27.83	1.094	27.79	1.094	27.79
E	min	1.669	42.46	1.197	30.45	1.220	31.00	1.219	30.95
	max	1.685	42.87	1.213	30.86	1.236	31.40	1.238	31.45
E1	min	1.558	39.64	1.086	27.63	1.086	27.59	1.086	27.59
	max	1.566	39.84	1.094	27.83	1.094	27.79	1.094	27.79
L	min	0.020	0.51	0.020	0.51	0.020	0.50	0.029	0.73
	max	0.030	0.76	0.030	0.76	0.030	0.75	0.041	1.03
e	BSC	0.020	0.50	0.020	0.50	0.020	0.50	0.026	0.65

† Metal Quad Flat Package

Socket Information

Several manufacturers make sockets and adapters for use with FPID device packages. The following is a representative list of manufacturers and their contact information. The sockets can be obtained directly from the manufacturer.

Manufacturer: Yamaichi Electronics Inc.
1420 Koll Circle Suite B
San Jose, CA 95112
USA
Phone: + (408) 452-0797
FAX: + (408) 452-0799

Manufacturer: Emulation Technology, Inc.
2344 Walsh Avenue
Bldg. F
Santa Clara, CA 95051
USA
Phone: + (408) 982-0660
FAX: + (408) 982-0664