IR3P68 Corelated Double Sampling IC

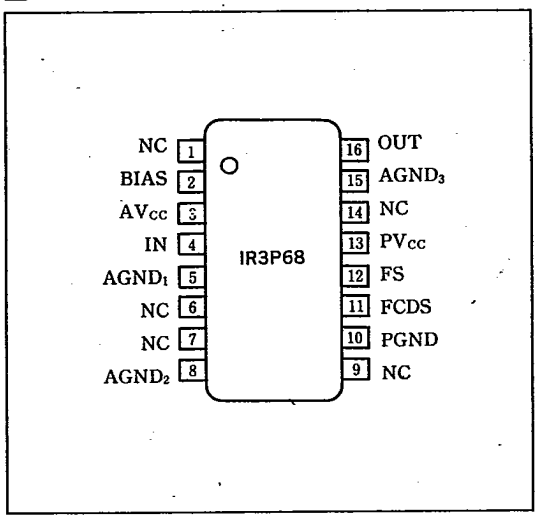
Description

The IR3P68 is a CDS IC for a CCD area sensor, which receives the CCD area sensor output, clamps the feed through level of the sensor output, sample-holds the signal level and then outputs it.

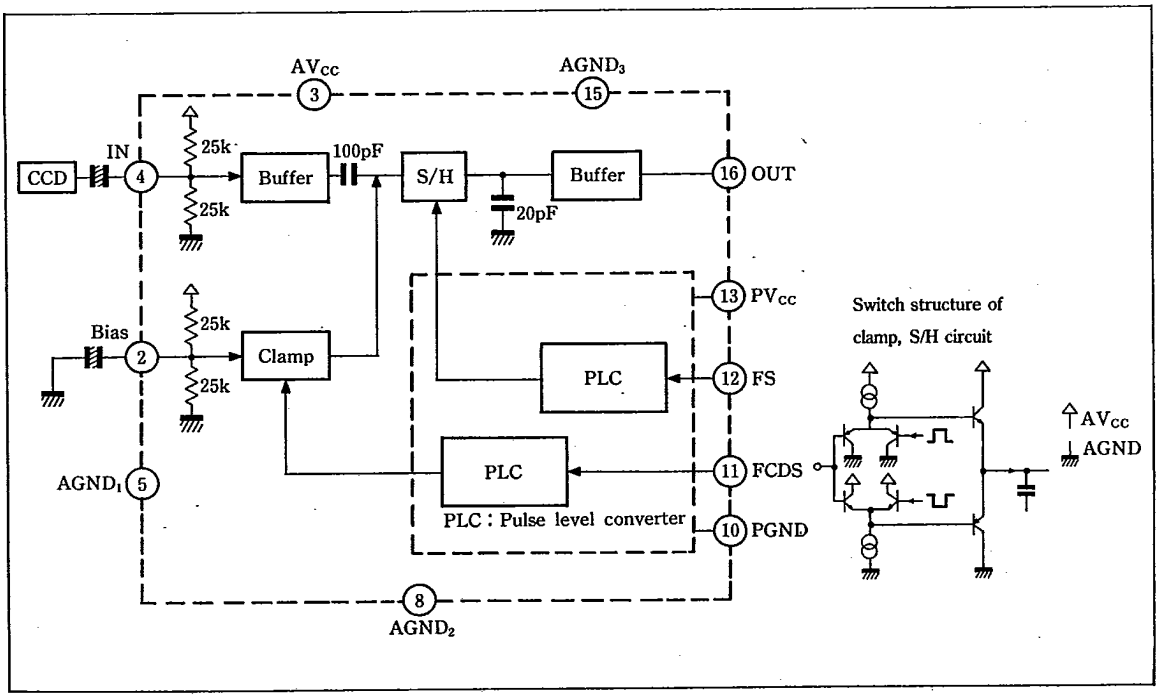
Features

1. Reduces the low range noise included in the CCD area sensor output.
2. Incorporates clamp and sample-hold capacitors.
3. 5V single power supply.
4. 16-pin small-outline package

Pin Connections



Block Diagram



Pin Functions

Pin No.	Symbol	Description	Function
1	NC		Non connection
2	BIAS	Reference voltage	The BIAS pin provides the reference voltage to clamp the feed through level of the CCD area sensor output (It has a bias resistor capable of controlling the clamp level by applying voltage from external)
3	AV_{CC}	Analog power supply	The AV_{CC} pin provides a power supply for buffers, a clamp and an S/H circuit in the IC
4	IN	Input	The IN pin has a DC bias resistor and inputs the CCD area sensor output by a capacity couping
5	$AGND_1$	Analog ground	The $AGND_1$ pin grounds the input
6	NC		Non connection
7	NC		Non connection
8	$AGND_2$	Analog ground	The $AGND_2$ grounds the output
9	NC		Non connection
10	PGND	Pulse ground	The PGND pin grounds the PLC (pulse Level Converter) circuits in the IC
11	FCDS	Pulse input	The FCDS pin inputs the pulse for clamping feedthrough level of the CCD area sensor output
12	FS	Sampling pulse input	The FS pin inputs the pulse to sample and hold the signal level at the CCD area sensor output at H level and L level respectively
13	PV_{CC}	Pulse power supply	The PV_{CC} pin provides a power supply for the PLC (Pulse Level Converter) circuits in the IC
14	NC		Non Connection
15	$AGND_3$	Analog ground	The $AGND_3$ grounds the output
16	OUT	Output	

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	AV_{CC}	Applied to AV_{CC}	7	V
	PV_{CC}	Applied to PV_{CC}	7	V
Input voltage	V_{IP}	Applied to FCDS and FS	$0 \sim PV_{CC}$	V
	V_{IA}	Applied to BIAS and IN	$0 \sim AV_{CC}$	V
Output current	I_O		±5	mA
Power dissipation	P_D	Ta≦60℃	300	mW
Operating temperature	T_{opr}		−10～+60	℃
Storage temperature	T_{stg}		−55～+150	℃

■ Electrical Characteristics (1)

(PV_{CC}=AV_{CC}=5V, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Test circuit
Operating supply voltage	V_{CC}	Applied for PV_{CC} and AV_{CC}	4.75	5.00	5.25	V	
Input "Low" voltage	V_{IL}	Applied for FCDS, and FS			0.8	V	2
Input "High" voltage	V_{IH}	Applied for FCDS and FS	2.0			V	2
Input "Low" current	I_{IL}	Applied for FCDS and FS V_I=0V, absolute value	0.5	0.8	1.1	mA	1
Input "High" current	I_{IH}	Applied for FCDS and FS, V_I=5V			10	μA	1
Supply current	PI_{CC}	Applied for PV_{CC}, FCDS=FS=0V	8	12.5	17	mA	3
	AI_{CC}	Applied for AV_{CC}, FCDS=FS=5V	4	6.3	9	mA	3
Release input pin voltage	V_{IN}	Applied for IN	2.4	2.5	2.6	V	4
	V_{bias}	Applied for BIAS	2.4	2.5	2.6	V	4
Release output pin voltage	V_{OUT}	Applied for OUT FCDS=FS=5V	2.1	2.3	2.5	V	4
Input pin impedance	R_{IN}	Applied for IN, f=1MHz	8	12		kΩ	5
	C_{IN}	Applied for IN, f=1MHz		2.5	4	pF	5
	R_{bias}	Applied for BIAS		12		kΩ	5
Output pin impedance	R_{OUT}	Applied for OUT, f=1MHz		40	100	Ω	5
Gain	G	f=0, 1MHz, 600mV_{P-P}	−2	−0.6	0	dB	6
Lenearity error		V_{in}=0.2~0.6 V_{P-P} Sampling 10MHz		0.5	1	%	7
Input dynamic range		Maximum I/O characteristic Sampling 10MHz	600			mV_{P-P}	7
Hold drift rate				−20		mV/μs	
Hold mode feedthrough		f=1MHz, 300mV_{P-P}	−50	−60		dB	8
S/H offset error	V_{SHO}	in=DC, V_{bias}=2.5V		8		mV	9
Sampling transition noise		in=DC, V_{bias}=2.5V		40		mV_{P-P}	9
Clamp section law frequency rejection ratio		f=0.1MHz	24	30		dB	10
Sample hold slew rate		Sampling rate 10MHz		750		mV/25ns	7
Clamp pulse width				20		ns	
S/H pulse width		f=1MHz, 300mV_{PP}		20		ns	

■ Electrical Characteristics (2)

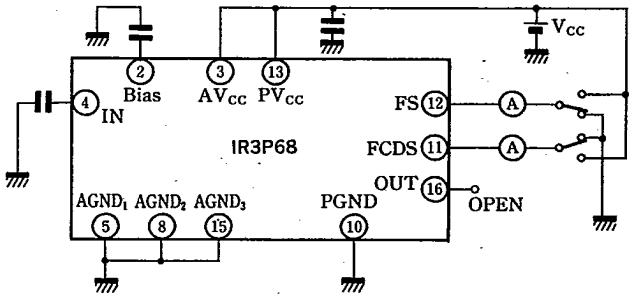
(PV_{CC}=AV_{CC}=4.75V~5.25V, Ta=−10℃~60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Test circuit
Input "Low" voltage	V_{IL}	Applied to FCDS and FS			0.7	V	2
Input "High" voltage	V_{IH}	Applied to FCDS and FS	2.0			V	2
Input "Low" current	I_{IL}	Applied to FCDS and FS V_i=0V absolute value	0.4		1.2	mA	1
Input "High" current	I_{IH}	Applied to FCDS and FS, V_i=5V			10	μA	1
Supply current	PI_{CC}	Applied to PV_{CC}, V_{CC}=5V FCDS=FS=0V	6		20	mA	3
	AI_{CC}	Applied to AV_{CC}, V_{CC}=5V FCDS=FS=5V	3		11	mA	3
Release input voltage	V_{IN}	Applied to IN	2.2		2.8	V	4
	V_{bias}	Applied to BIAS	2.2		2.8	V	4
Release output voltage	V_{OUT}	Applied to OUT, FCDS=FS=5V	1.9		2.7	V	4
Gain	G		−2		0	dB	6
Max. sample rate			10			MHz	

The ratings in the electrical characteristics (1) and (2) are the ones in a sampling rate of 10MHz, unless oterwise specified. For use in 10MHz or more, refer to the Electrical Characteristic Curves.

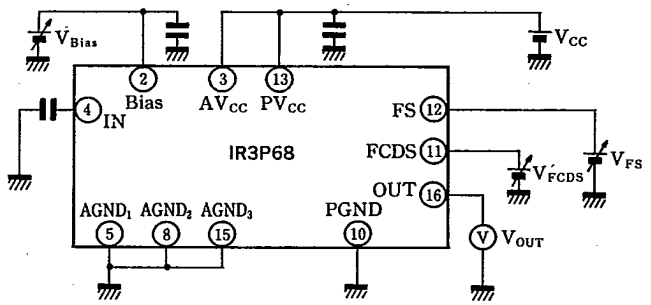
■ Test Circuit

(1) I_{IL}, I_{IH}

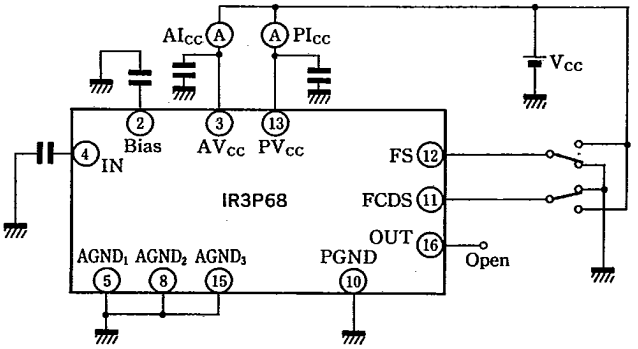


(2) V_{IL}, FS input voltage—Output voltage

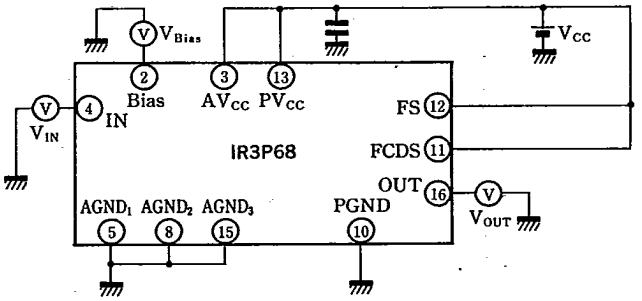
FCDS input voltage—Output voltage



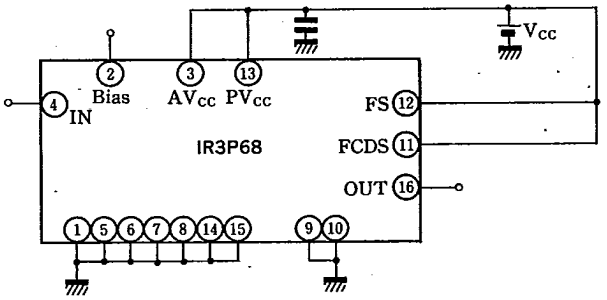
(3) PI_{CC}, AI_{CC}



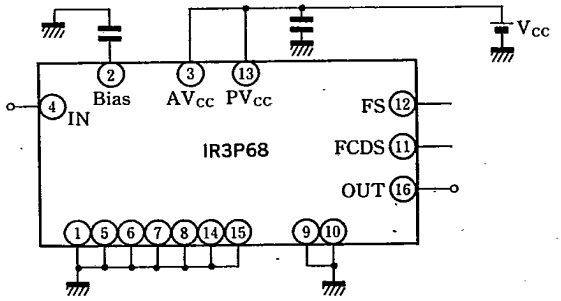
(4) Release input voltage—Release output voltage

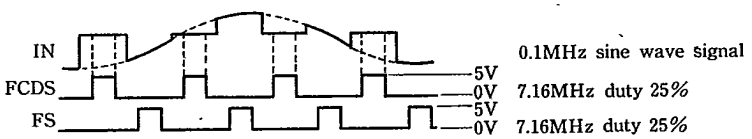


(5) Input impedance—Output impedance

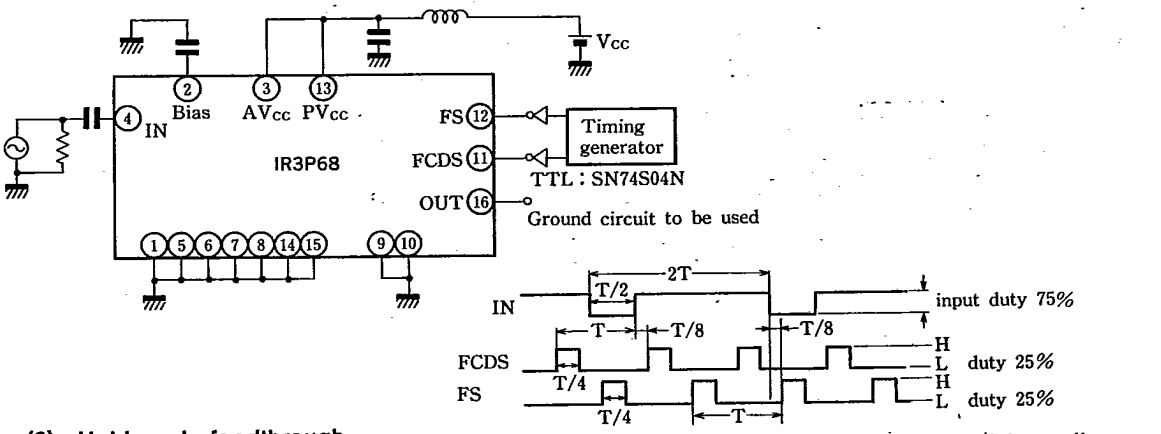


(6) Gain



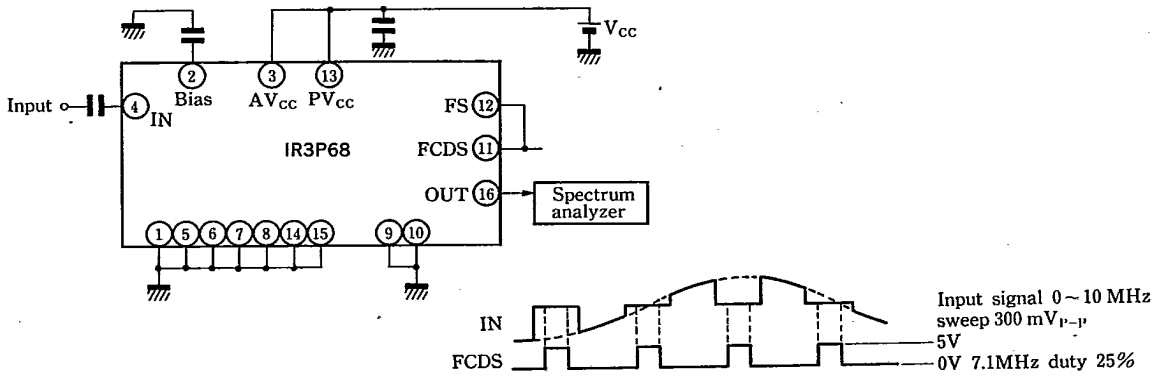


(7) S/H I/O characteristics (Linearity error, Input dynamic range, S/H slew rate)

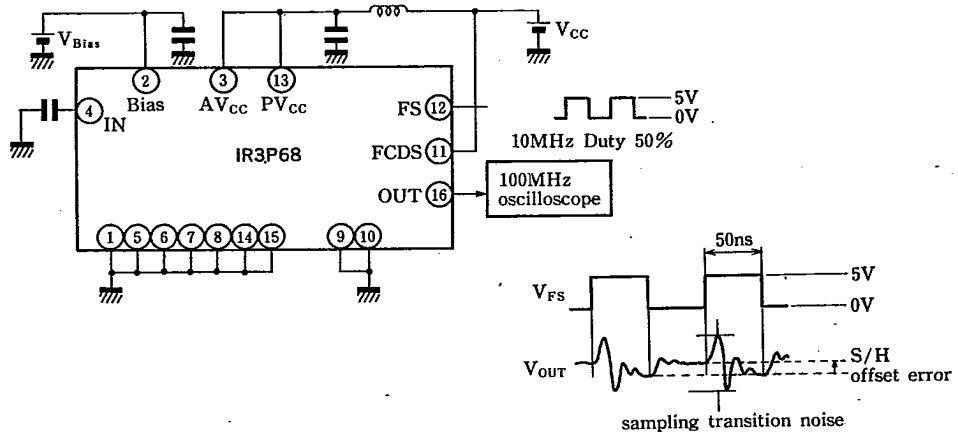


T=1/f, f : sampling rate

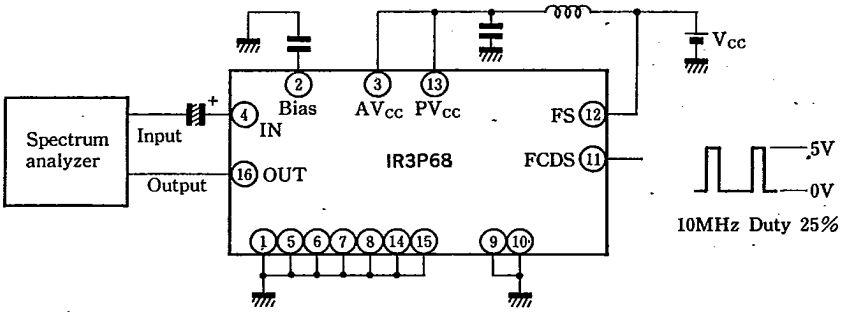
(8) Hold mode feedthrough



(9) S/H offset errer
Sampling transition noise



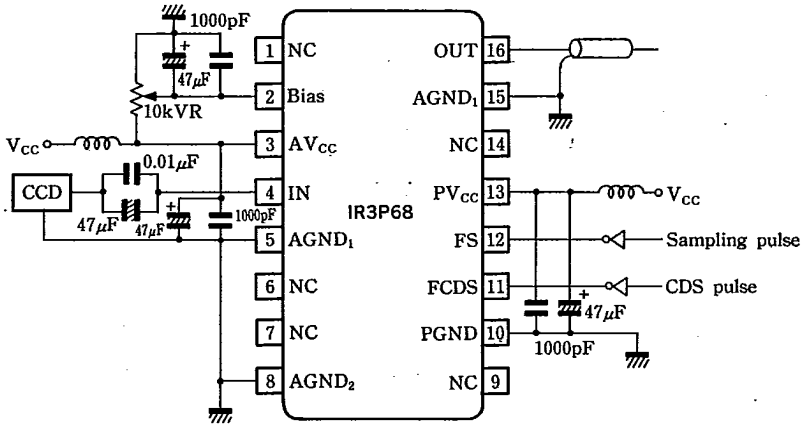
(10) Clamp Characteristics



Input : 0 ~ 10 MHz sweep $0.3V_{P-P}$

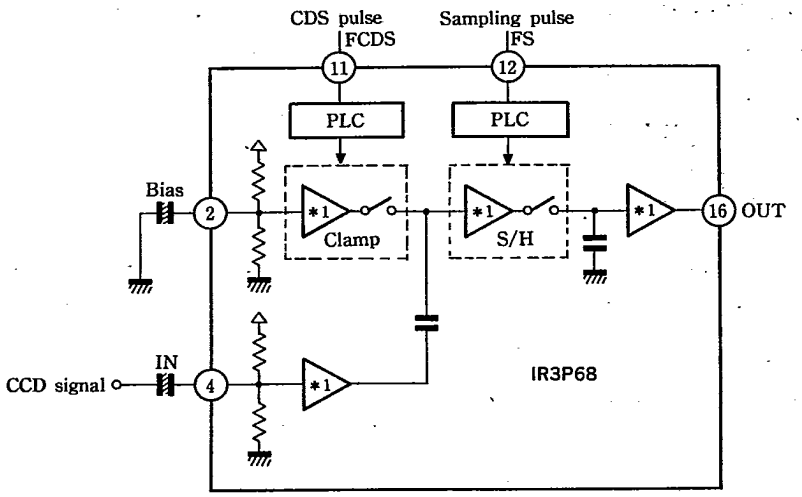
Grounded circuit to be used

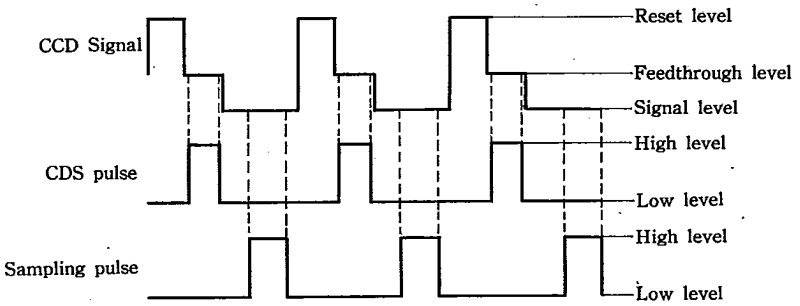
■ Basic Connection Diagram



- For the addition and removal of any external part, consider them in the mounted condition.
- The ground plane type with grounded on one side is recommended for the circuit board.
- $AGND_1$ (pin 5), $AGND_2$ (pin 8) and $AGND_3$ (pin 15) should be connected at the minimum distance and kept at low impedance.
- The bypass capacitor between the power source and GND should be connected at the minimum distance. The use of a chip capacitor is recommended.
- For the peaking coil of the power source, use the one with the self-oscillation frequency of about 100MHz.
- Use pin 5 for GND of the CCD area sensor, pin 10 for GND of FS and FCDS pulses, and pin 15 for GND of outputs.
- It is preferable that the NC pin is connected to GND.
- If there is any external influence, provide a shield plate on the top and bottom of the IC to prevent noise.

Description of Operation



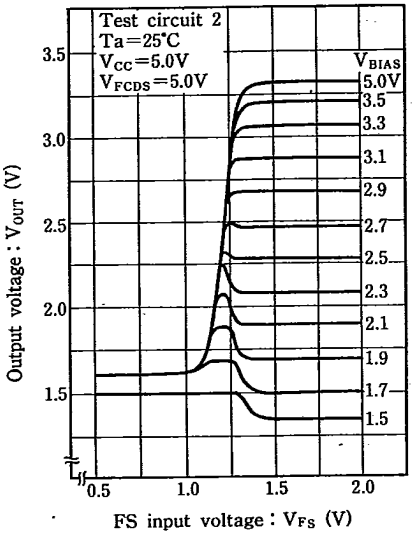


The IR3P68 inputs the CCD area sensor output by means of the capacity connection, clamps the feedthrough level of the CCD area sensor output at the bias potential (pin 2), sample-holds the difference between the signal level and the feedthrough level and then outputs it.

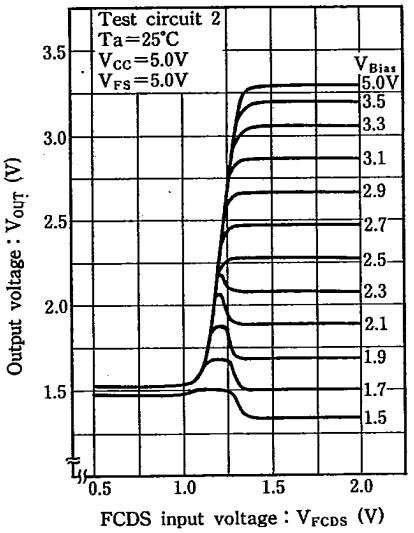
The switch part of each circuit for clamp and S/H is closed when the pulse input is at the H level and opened when at the L level.

Electrical Characteristic Curves

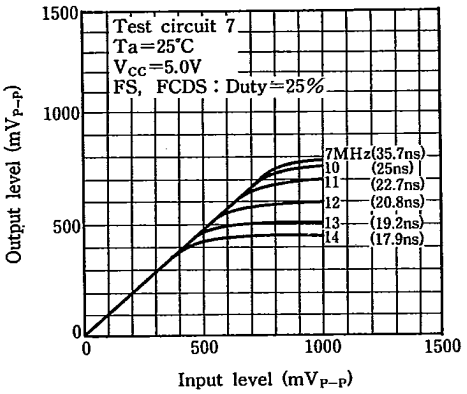
FS input voltage—Output voltage



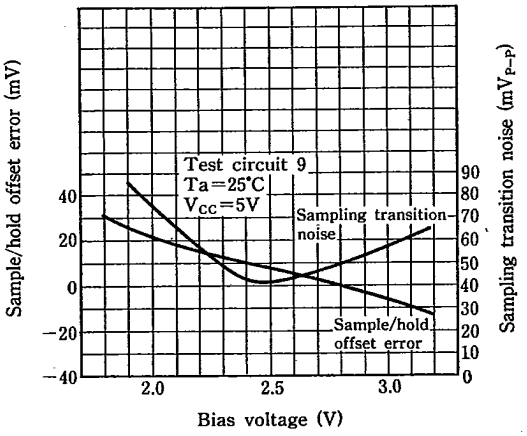
FCDS input voltage—Output voltage



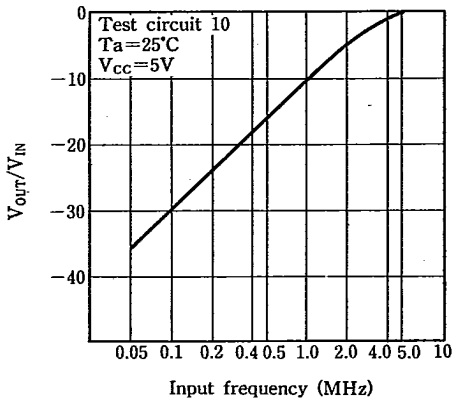
S/H, I/O Characteristics



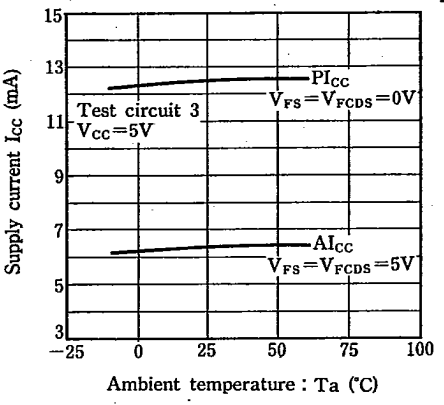
S/H offset errer—Bias voltage
Sampling transition noise—Bias voltage



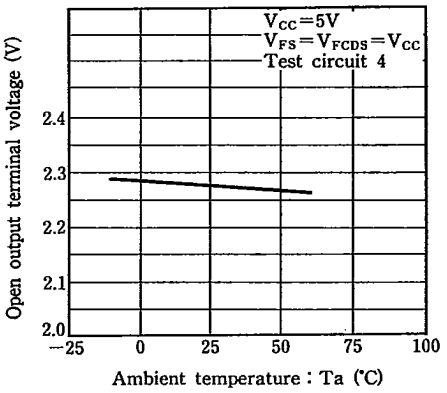
Clamp characteristics (Low range suppression characteristics)



Supply current—Temperature



Release output voltage—Temperature



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