Data Sheet No. PD-9.518A

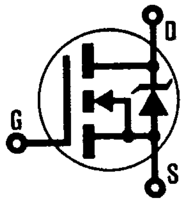
T-39-15

INTERNATIONAL RECTIFIER IOR

REPETITIVE AVALANCHE AND dv/dt RATED

HEXFET® TRANSISTORS

IRF360
IRF362



N-CHANNEL

400 Volt, 0.20 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Product Summary

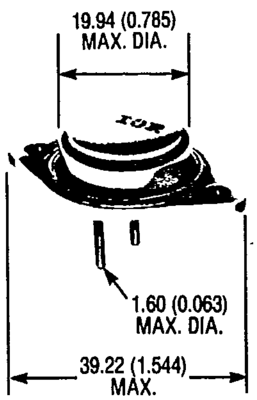
Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRF360	400V	0.20Ω	25A
IRF362	400V	0.25Ω	22A

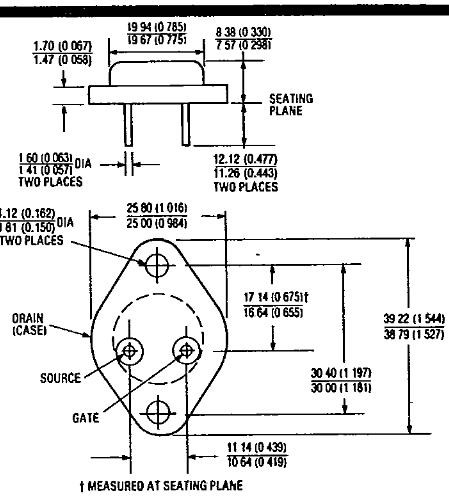
FEATURES:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling

TO-3

CASE STYLE AND DIMENSIONS





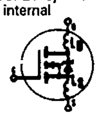
Conforms to JEDEC Outline TO-204AE (Modified TO-3)
Dimensions in Millimeters and (Inches)

IRF360, IRF362 Devices

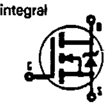
Absolute Maximum Ratings

Parameter		IRF360	IRF362	Units
I_D @ T_C = 25°C	Continuous Drain Current	25	22	A
I_D @ T_C = 100°C	Continuous Drain Current	16	14	A
I_{DM}	Pulsed Drain Current ①	100	88	A
P_D @ T_C = 25°C	Max. Power Dissipation	300		W
	Linear Derating Factor	2.4		W/K ⑤
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	980 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ① (Repetitive or Non-Repetitive)	25 (See E_{AR})		A
E_{AR}	Repetitive Avalanche Energy ①	30 (See I_{AR})		mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0 (See Fig. 17)		V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	400	—	—	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ④	IRF360	—	0.18	0.20	Ω	V_{GS} = 10V, I_D = 14A
		IRF362	—	0.20	0.25		
$I_{D(on)}$	On-State Drain Current ④	IRF360	25	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max. V_{GS} = 10V
		IRF362	22				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250 μA
g_{fs}	Forward Transconductance ④	ALL	14	21	—	S (℧)	I_{DS} = 14A, V_{DS} ≥50V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	−100	nA	V_{GS} = −20V
Q_g	Total Gate Charge	ALL	—	120	170	nC	V_{GS} = 10V, I_D = 25A
Q_{gs}	Gate-to-Source Charge	ALL	—	19	28	nC	V_{DS} = 0.8 x Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	—	60	90	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	22	33	ns	V_{DD} = 200V, I_D ≈ 25A, R_G = 4.3Ω
t_r	Rise Time	ALL	—	94	140	ns	R_D = 7.5Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	80	120	ns	See Fig. 15
t_f	Fall Time	ALL	—	66	99	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. / Modified MOSFET symbol showing the internal inductances. 
L_S	Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	4000	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	550	—	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	97	—	pF	See Fig. 10

Source-Drain Diode Ratings and Characteristics

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	25	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier 
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	—	—	100	A	
V_{SD}	Diode Forward Voltage ④	ALL	—	—	1.8	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	460	1000	ns	T_J = 25°C, I_F = 25A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.1	7.1	16	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$				

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.42	K/W ⑤	
R_{thCS}	Case-to-Sink	ALL	—	0.12	—	K/W ⑤	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	30	K/W ⑤	Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 2.8 mH, Peak I_L = 25A,

③ $I_{SD} \leq$ 25A, di/dt ≤ 170 A/μs, $V_{DD} \leq BV_{DSS}$, $T_J \leq$ 150°C Suggested R_G = 4.3Ω

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ K/W = °C/W W/K = W/°C

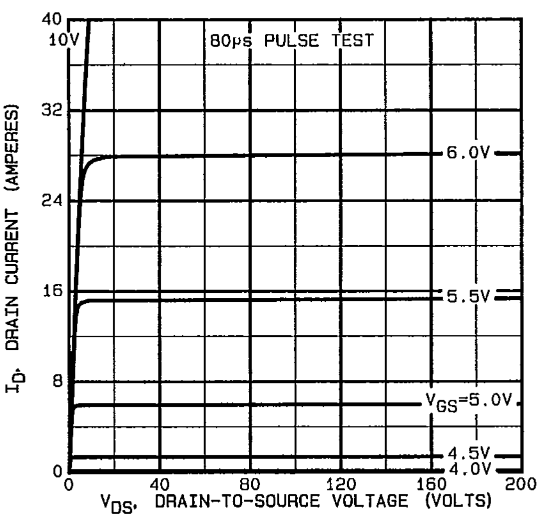


Fig. 1 — Typical Output Characteristics

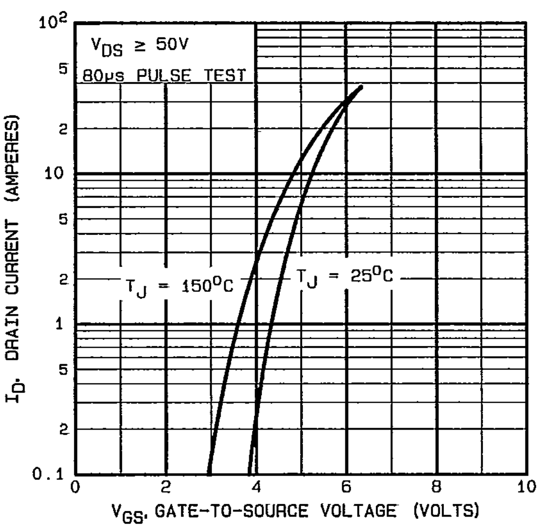


Fig. 2 — Typical Transfer Characteristics

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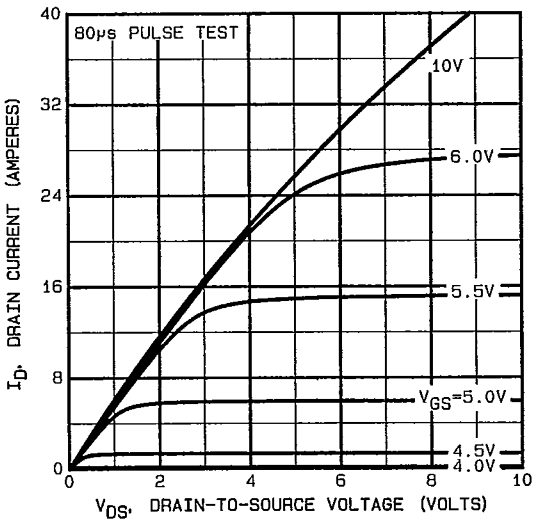

Fig. 3 — Typical Saturation Characteristics

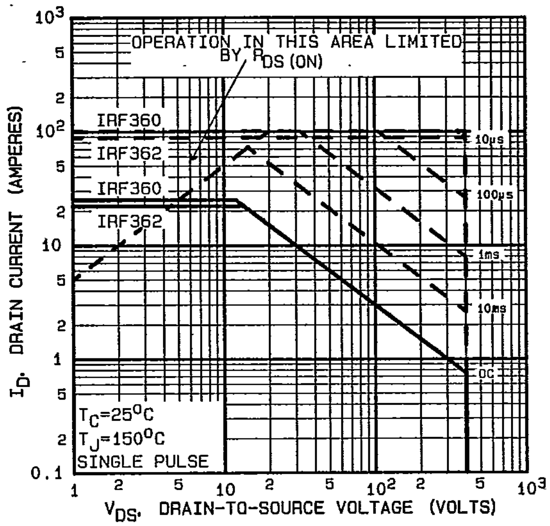

Fig. 4 — Maximum Safe Operating Area

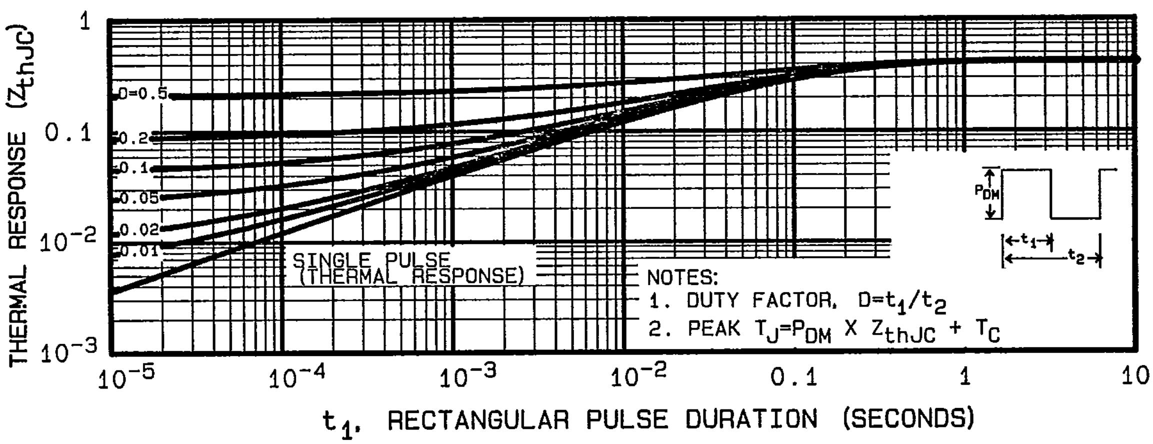

Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

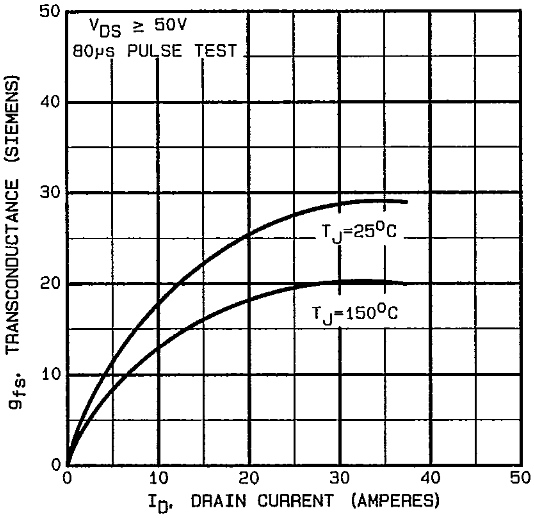

Fig. 6 — Typical Transconductance Vs. Drain Current

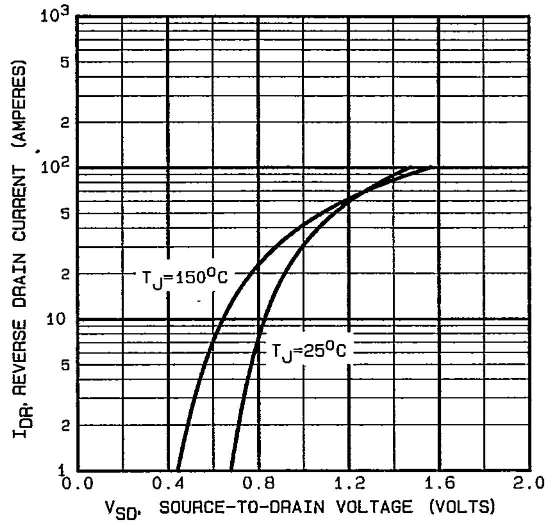

Fig. 7 — Typical Source-Drain Diode Forward Voltage

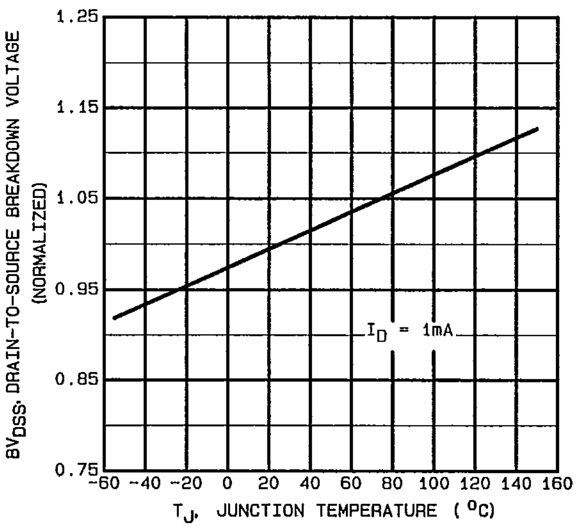

Fig. 8 — Breakdown Voltage Vs. Temperature

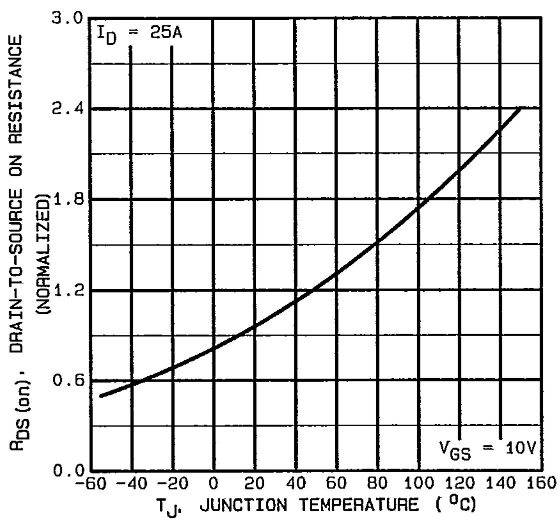

Fig 9 — Normalized On-Resistance Vs. Temperature

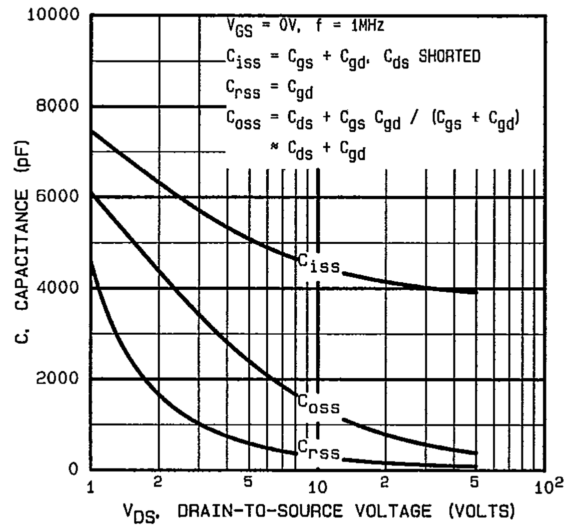

Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

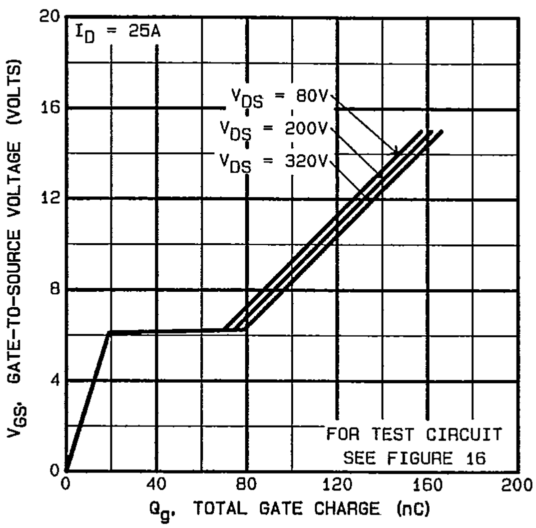

Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

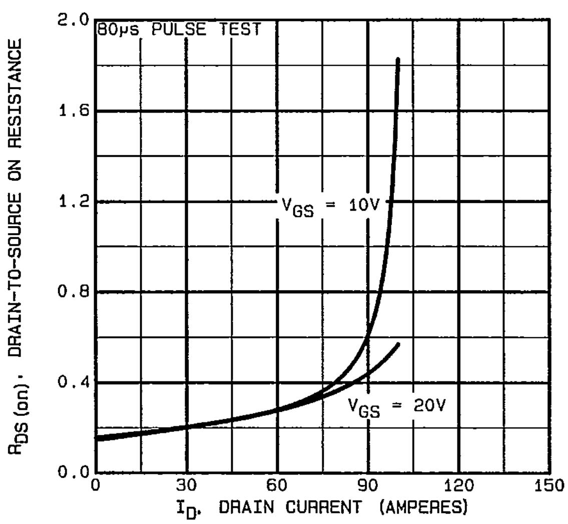

Fig. 12 — Typical On-Resistance Vs. Drain Current

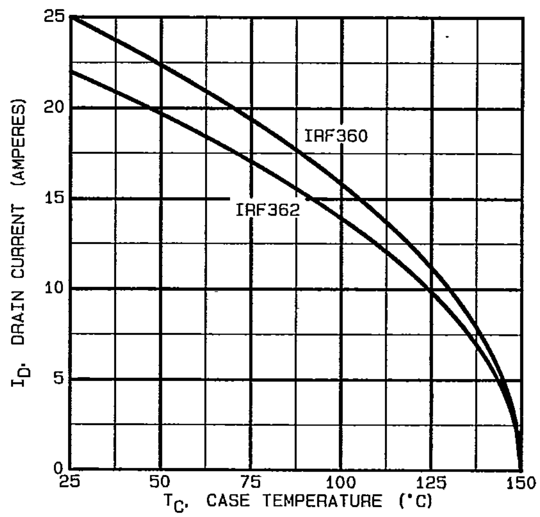

Fig. 13 — Maximum Drain Current Vs. Case Temperature

IRF360, IRF362 Devices

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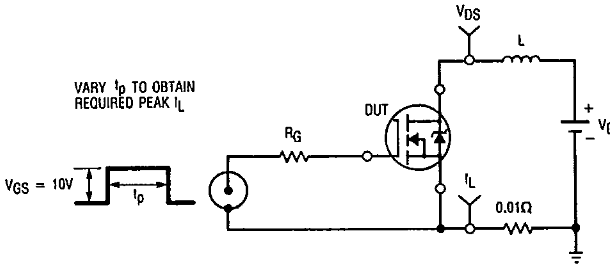

Fig. 14a — Unclamped Inductive Test Circuit

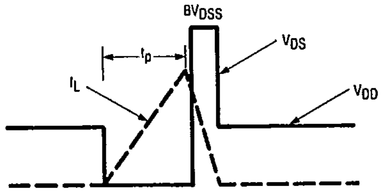

Fig. 14b — Unclamped Inductive Waveforms

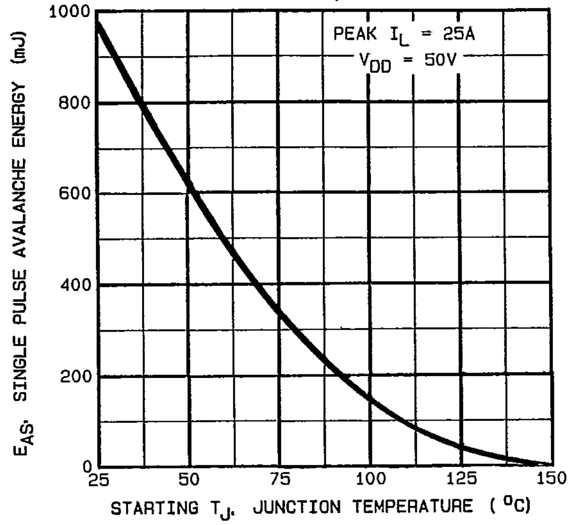

Fig. 14c — Maximum Avalanche Energy Vs. Starting Junction Temperature

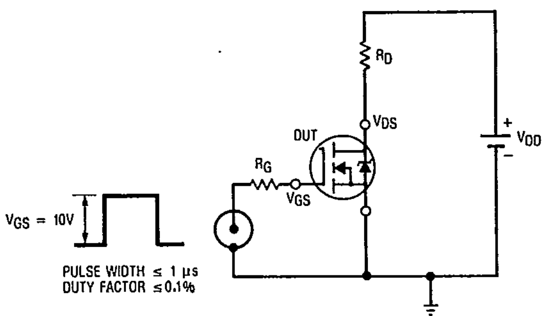

Fig. 15a — Switching Time Test Circuit

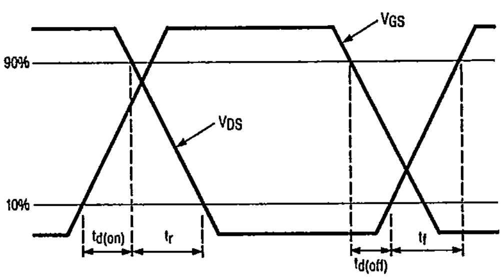

Fig. 15b — Switching Time Waveforms

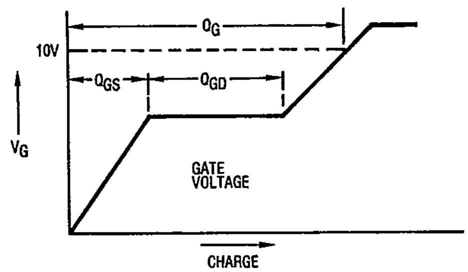

Fig. 16a — Basic Gate Charge Waveform

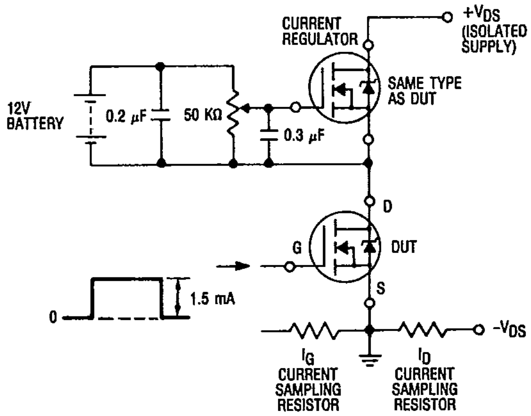

Fig. 16b — Gate Charge Test Circuit

TO-3

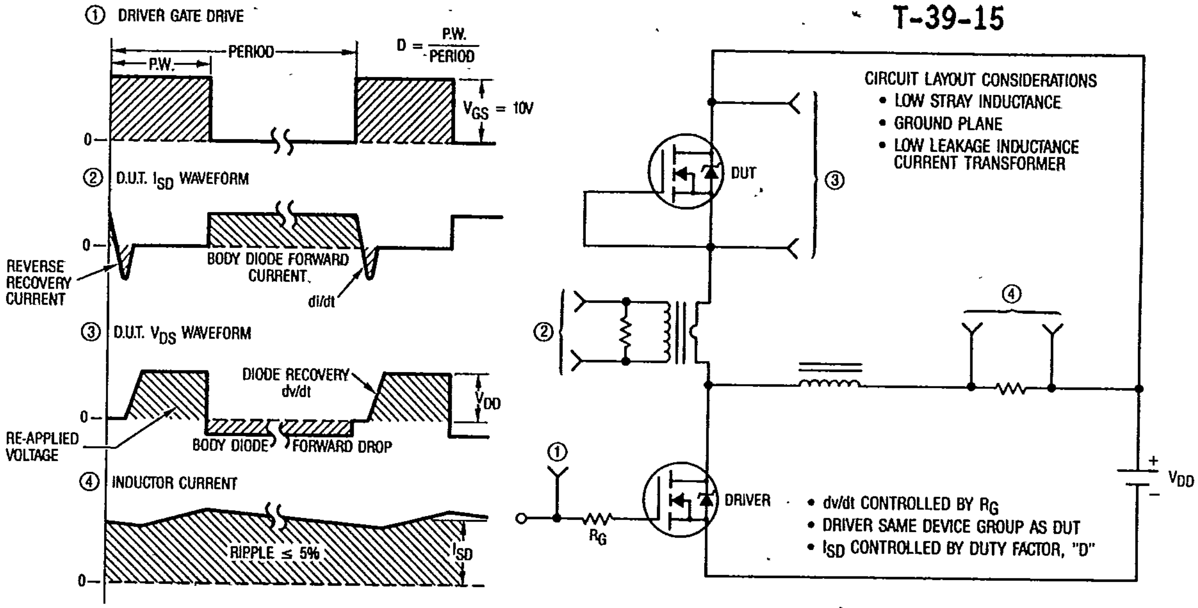

Fig. 17 — Peak Diode Recovery dv/dt Test Circuit

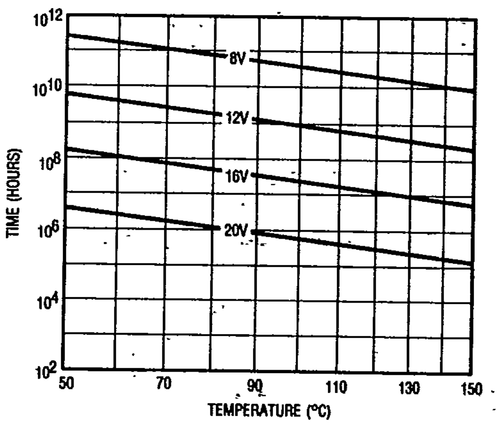

***Fig. 18 — Typical Time to Accumulated 1% Gate Failure**

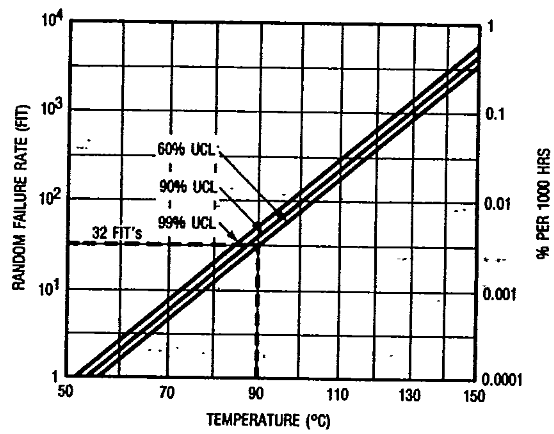

***Fig. 19 — Typical High Temperature Reverse Bias (HTRB) Failure Rate**

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.