International
IOR Rectifier

Provisional Data Sheet No. PD-9.548B

HEXFET® POWER MOSFET

JANTX2N6806
JANTXV2N6806
[REF:MIL-PRF-19500/562]
[GENERIC:IRF9230]
P-CHANNEL

-200 Volt, 0.80Ω HEXFET

HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry achieves very low on-state resistance combined with high transconductance.

HEXFET transistors also feature all of the well-establish advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits, and virtually any application where high reliability is required.

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
JANTX2N6806 JANTXV2N6806	-200V	0.80Ω	-6.5A

Features:

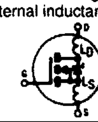
- Avalanche Energy Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed

Absolute Maximum Ratings

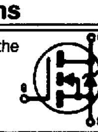
	Parameter	JANTX2N6806, JANTXV2N6806	Units
I_D @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-6.5	A
I_D @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-4.0	
I_{DM}	Pulsed Drain Current ①	-28	
P_D @ T_C = 25°C	Max. Power Dissipation	75	W
	Linear Derating Factor	0.60	W/K ⑤
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	66	mJ
I_{AR}	Avalanche Current ①	-6.5	A
E_{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10.5 seconds)	
	Weight	11.5 (typical)	g

JANTX2N6806, JANTXV2N6806 Device

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	V_{GS} = 0V, I_D = -1.0 mA	
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.20	—	V/°C	Reference to 25°C, I_D = -1.0 mA	
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.80	Ω	V_{GS} = -10V, I_D = -4.0A④	
		—	—	0.92		V_{GS} = -10V, I_D = -6.5A	
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA	
g_{fs}	Forward Transconductance	2.0	—	—	S (℧)	V_{DS} > -15V, I_{DS} = -4.0A ④	
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V_{DS} = 0.8 x Max Rating, V_{GS} = 0V	
		—	—	-250		V_{DS} = 0.8 x Max Rating V_{GS} = 0V, T_J = 125°C	
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V	
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V	
Q_g	Total Gate Charge	8	—	31	nC	V_{GS} = -10V, I_D = -6.5A	
Q_{gs}	Gate-to-Source Charge	0.8	—	7.0		V_{DS} = Max. Rating x 0.5	
Q_{gd}	Gate-to-Drain ("Miller") Charge	5.0	—	17		see figures 6 and 13	
$t_{d(on)}$	Turn-On Delay Time	—	—	50	ns	V_{DD} = -100V, I_D = -6.5A,	
t_r	Rise Time	—	—	100		R_G = 7.5Ω, V_{GS} = -10V	
$t_{d(off)}$	Turn-Off Delay Time	—	—	100			
t_f	Fall Time	—	—	80		see figure 10	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	Modified MOSFET symbol showing the internal inductances. 
L_S	Internal Source Inductance	—	13.0	—		Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	
C_{iss}	Input Capacitance	—	700	—	pF	V_{GS} = 0V, V_{DS} = -25V	
C_{oss}	Output Capacitance	—	200	—		f = 1.0 MHz	
C_{rss}	Reverse Transfer Capacitance	—	40	—		see figure 5	

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-6.5	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-28		
V_{SD}	Diode Forward Voltage	—	—	-6.0	V	T_j = 25°C, I_S = -6.5A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	400	ns	T_j = 25°C, I_F = -6.5A, di/dt ≤ -100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	4.0	μC	V_{DD} ≤ -50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	1.67	K/W	
R_{thJA}	Junction-to-Ambient	—	—	30		Typical socket mount

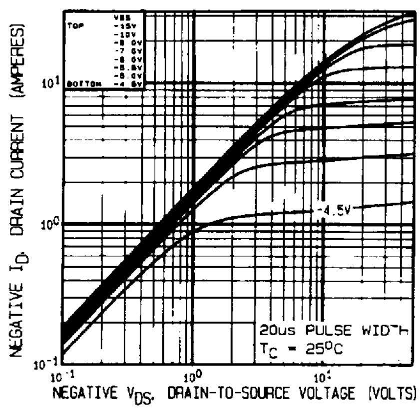


Fig. 1 — Typical Output Characteristics $T_C = 25°C$

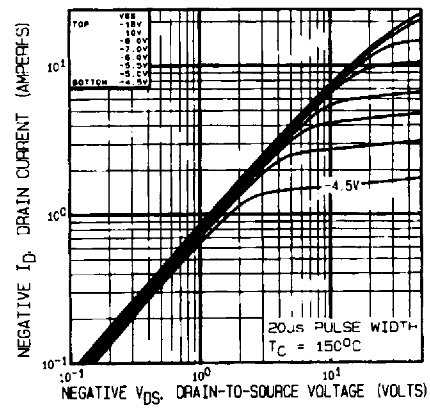


Fig. 2 — Typical Output Characteristics $T_C = 150°C$

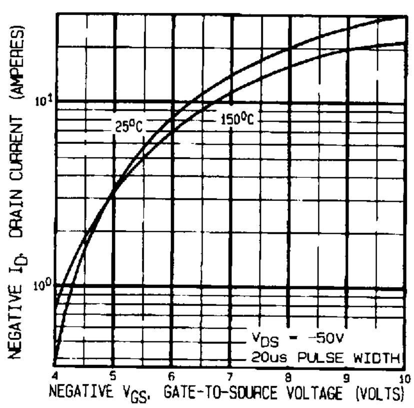


Fig. 3 — Typical Transfer Characteristics

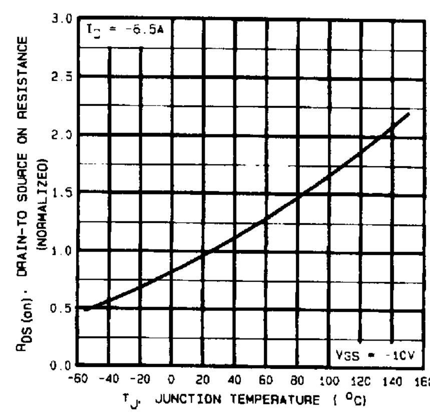


Fig. 4 — Normalized On-Resistance Vs.Temperature

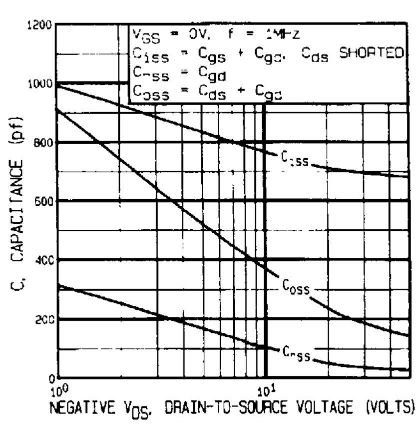


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

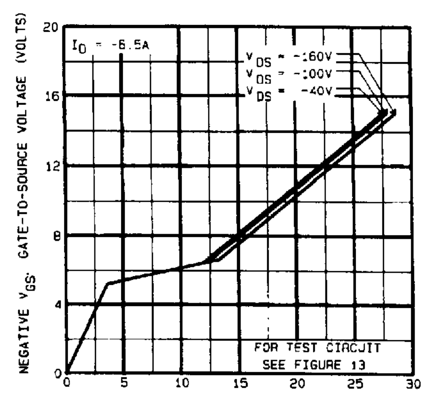


Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage

JANTX2N6806, JANTXV2N6806 Device

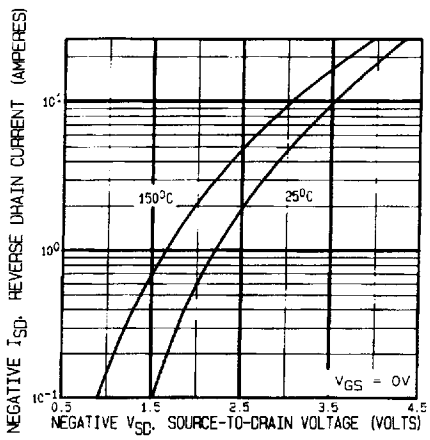


Fig. 7 — Typical Source-to-Drain Diode Forward Voltage

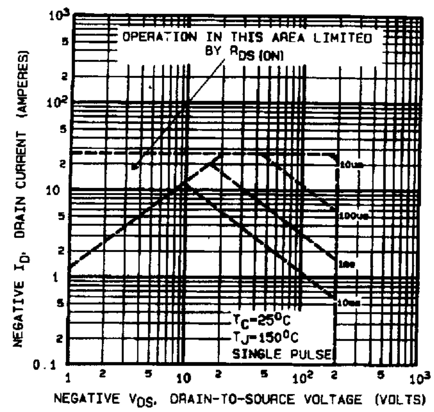


Fig. 8 — Maximum Safe Operating Area

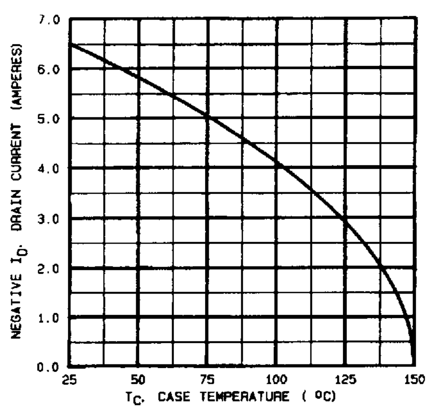


Fig. 9 — Maximum Drain Current Vs. Case Temperature

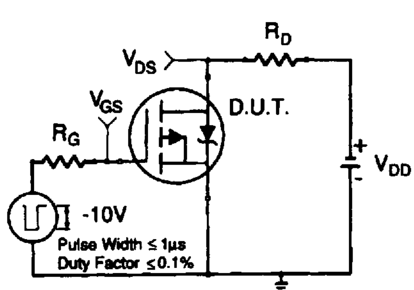


Fig. 10a — Switching Time Test Circuit

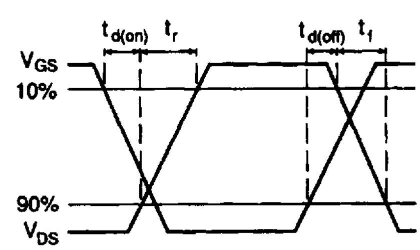


Fig. 10b — Switching Time Waveforms

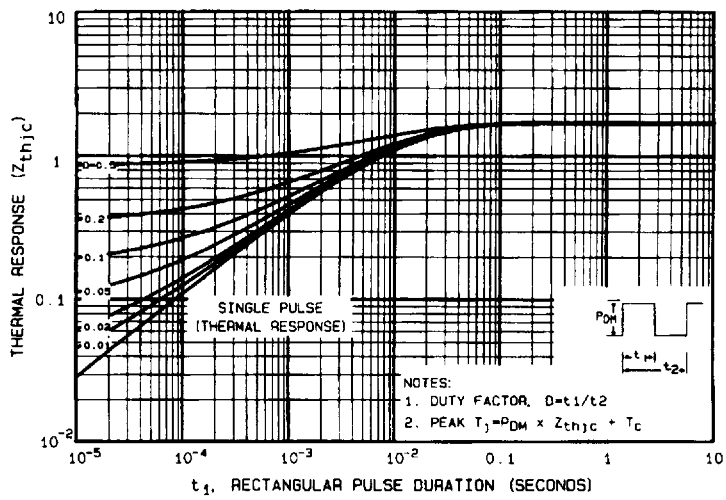


Fig. 11 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

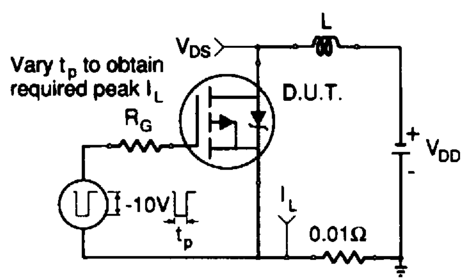


Fig. 12a — Unclamped Inductive Test Circuit

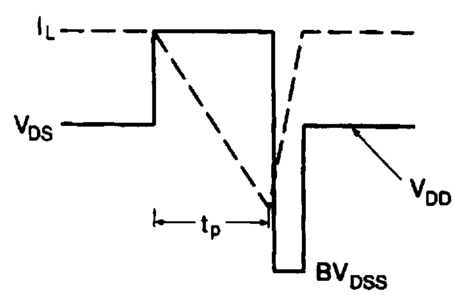


Fig. 12b — Unclamped Inductive Waveforms

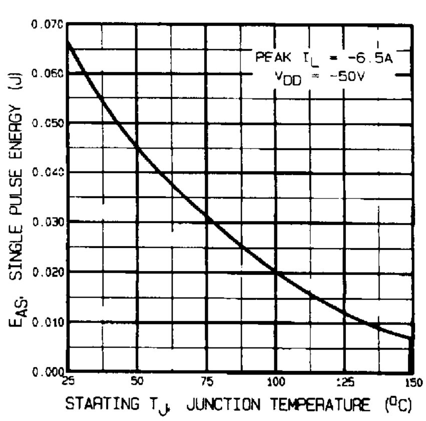


Fig. 12c — Max. Avalanche Energy vs. Current

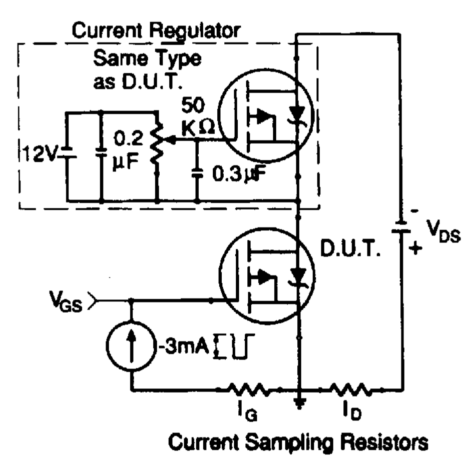


Fig. 13a — Gate Charge Test Circuit

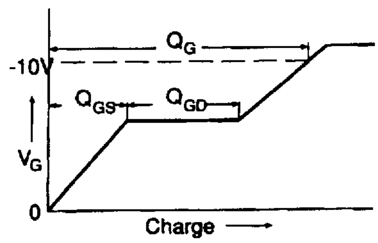


Fig. 13b — Basic Gate Charge Waveform

① Repetitive Rating; Pulse width limited by maximum junction temperature. (see figure 11)

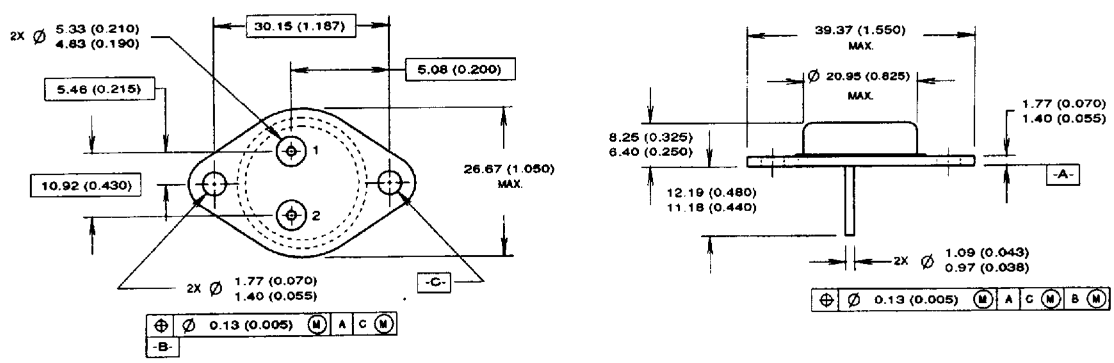
② @ V_{DD} = -50V, Starting T_J = 25°C,
$E_{AS} = [0.5 \cdot L \cdot (I_L^2) \cdot [BV_{DSS}/(BV_{DSS}-V_{DD})]$
Peak I_L = -6.5A, V_{GS} = -10V, $25 \leq R_G \leq 200\Omega$

③ $I_{SD} \leq$ -6.5A, di/dt $\leq$ -120A/µs,
$V_{DD} \leq BV_{DSS}$, $T_J \leq$ 150°C

④ Pulse width $\leq$ 300 µs; Duty Cycle $\leq$ 2%

⑤ K/W = °C/W
W/K = W/°C

Case Outline and Dimensions — TO-204AA (Modified TO-3)



All dimensions are shown millimeters (inches)

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