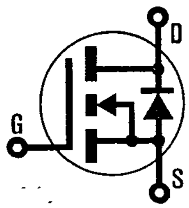
Data Sheet No. PD-9.378E
T-39-09

INTERNATIONAL RECTIFIER IOR

HEXFET® TRANSISTORS IRFF220 IRFF221 IRFF222 IRFF223

N-CHANNEL POWER MOSFETs TO-39 PACKAGE



200 Volt, 0.8 Ohm HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

Features:

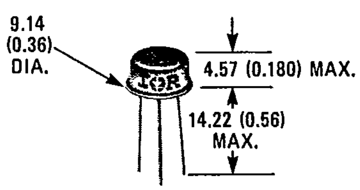
- Fast Switching
- Low Drive Current
- Ease of Paralleling
- Excellent Temperature Stability

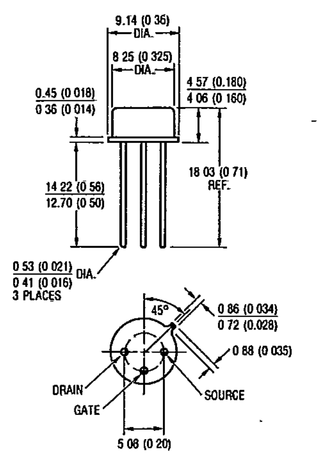
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFF220	200V	0.8Ω	3.5A
IRFF221	150V	0.8Ω	3.5A
IRFF222	200V	1.2Ω	3.0A
IRFF223	150V	1.2Ω	3.0A

TO-39

CASE STYLE AND DIMENSIONS





Conforms to JEDEC Outline TO-205AF (TO-39)
Dimensions in Millimeters and (Inches)

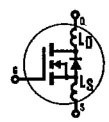
IRFF220, IRFF221, IRFF222, IRFF223 Devices

Absolute Maximum Ratings

	Parameter	IRFF220	IRFF221	IRFF222	IRFF223	Units
V_{DS}	Drain — Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain — Gate Voltage (R_{GS} = 20 kΩ)①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate — Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/K ④
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 14	14	12	12	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain — Source Breakdown Voltage	IRFF220 IRFF222	200	—	—	V	V_{GS} = 0V
		IRFF221 IRFF223	150	—	—	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate — Source Leakage Forward	ALL	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate — Source Leakage Reverse	ALL	—	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF220 IRFF221	3.5	—	—	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF222 IRFF223	3.0	—	—	A	
$R_{DS(on)}$	Static Drain — Source On-State Resistance ②	IRFF220 IRFF221	—	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.0A
		IRFF222 IRFF223	—	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.25	—	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.0A
C_{iss}	Input Capacitance	ALL	—	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	—	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	—	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	—	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	—	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	50	100	ns	
t_f	Fall Time	ALL	—	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	11	15	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8V Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	5.0	—	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	—	6.0	—	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die. / Modified MOSFET symbol showing the internal device inductances.
L_S	Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	6.25	K/W ④	
R_{thJA}	Junction-to-Ambient	ALL	—	—	175	K/W ④	Typical socket mount

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF220 IRFF221	—	—	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFF222 IRFF223	—	—	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF220 IRFF221	—	—	14	A	
		IRFF222 IRFF223	—	—	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF220 IRFF221	—	—	2.0	V	$T_C = 25°C, I_S = 3.5A, V_{GS} = 0V$
		IRFF222 IRFF223	—	—	1.8	V	$T_C = 25°C, I_S = 3.0A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	—	350	—	ns	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	—	2.3	—	μC	$T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$. ② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

④ K/W = °C/W
W/K = W/°C

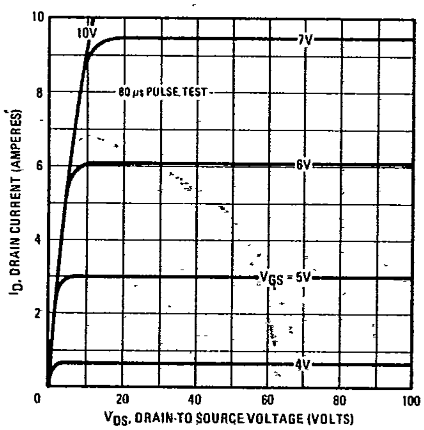


Fig. 1 — Typical Output Characteristics

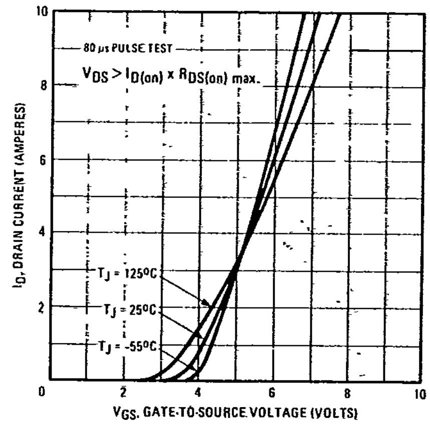


Fig. 2 — Typical Transfer Characteristics

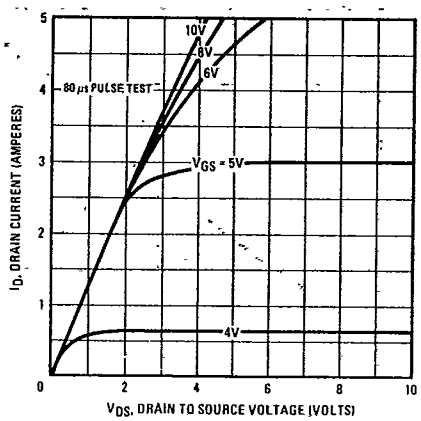


Fig. 3 — Typical Saturation Characteristics

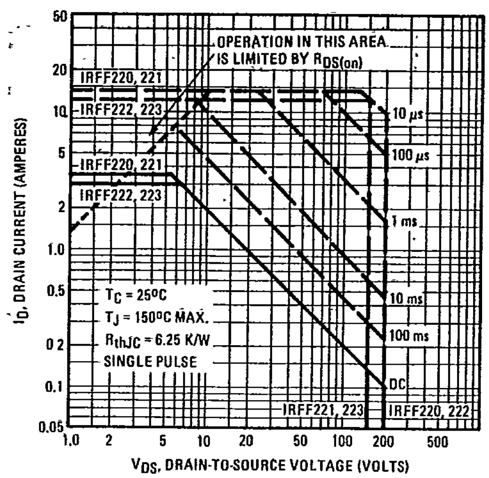


Fig. 4 — Maximum Safe Operating Area

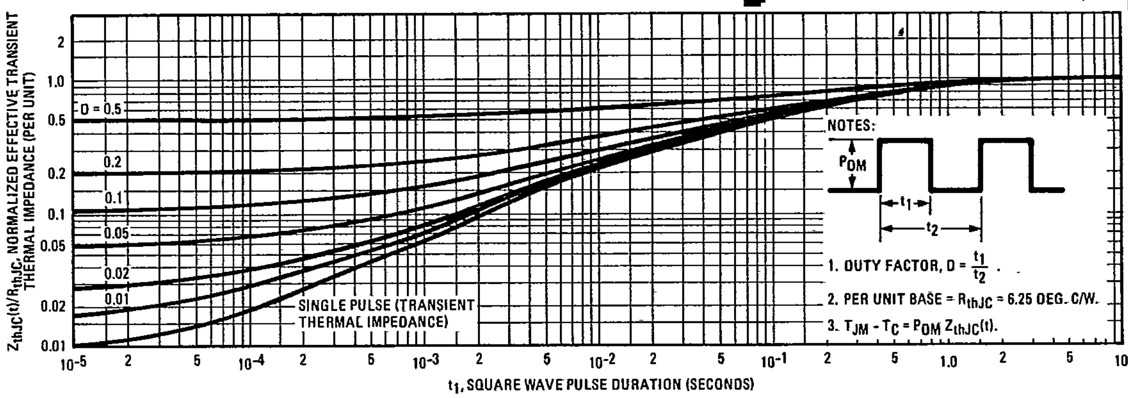


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

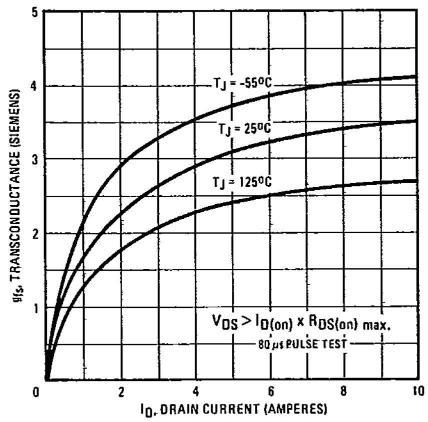


Fig. 6 — Typical Transconductance Vs. Drain Current

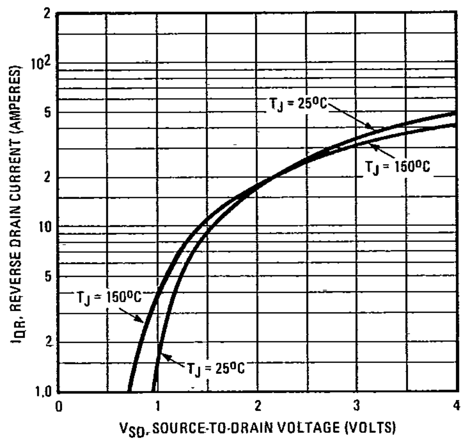


Fig. 7 — Typical Source-Drain Diode Forward Voltage

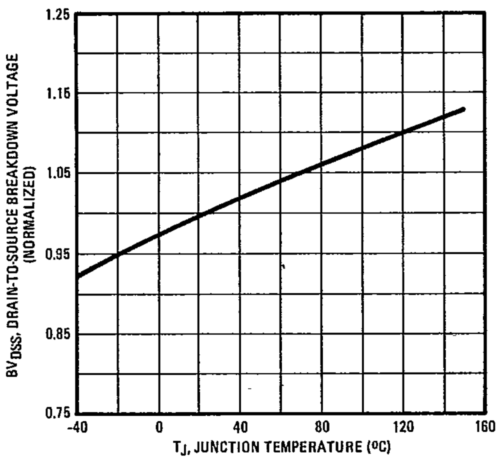


Fig. 8 — Breakdown Voltage Vs. Temperature

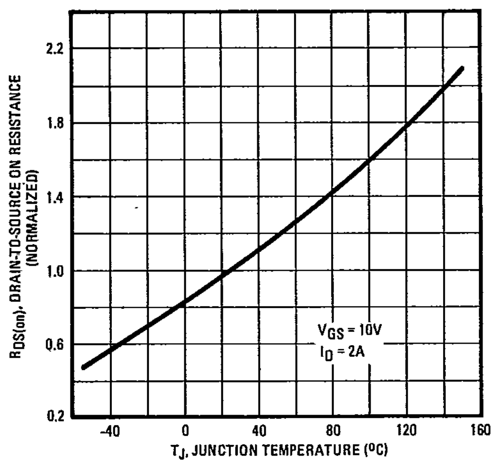


Fig. 9 — Normalized On-Resistance Vs. Temperature

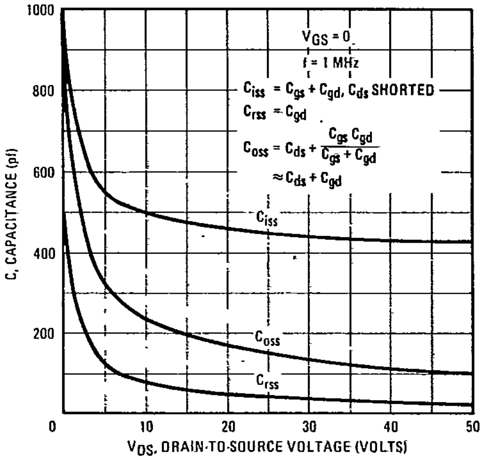


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

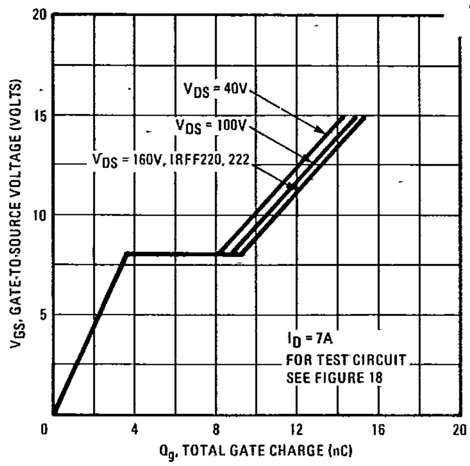


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

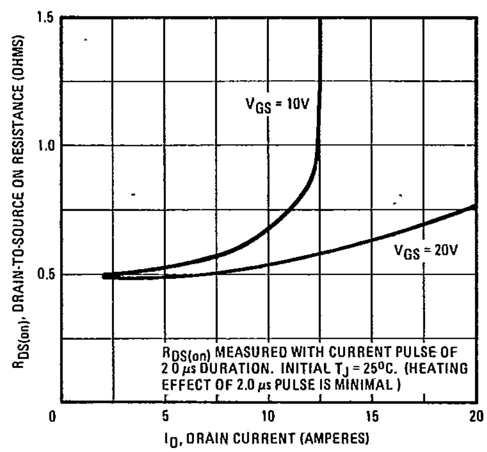


Fig. 12 — Typical On-Resistance Vs. Drain Current

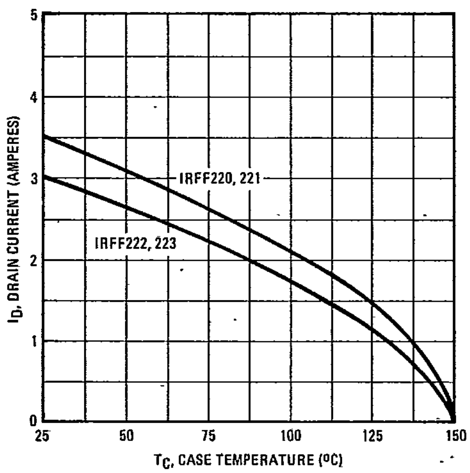


Fig. 13 — Maximum Drain Current Vs. Case Temperature

TO-39

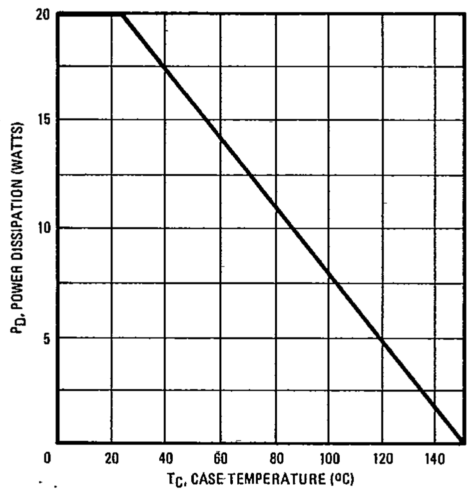


Fig. 14 — Power Vs. Temperature Derating Curve

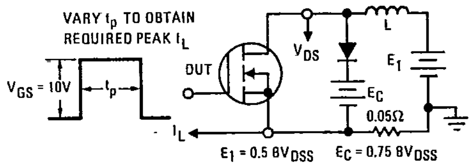


Fig. 15 — Clamped Inductive Test Circuit

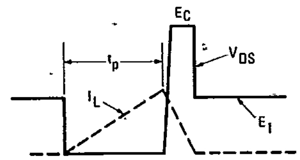


Fig. 16 — Clamped Inductive Waveforms

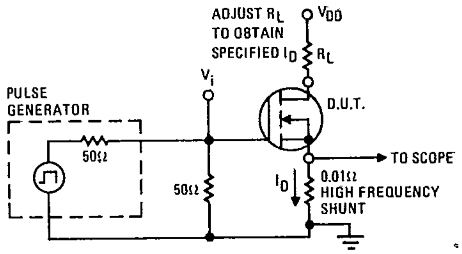


Fig. 17 — Switching Time Test Circuit

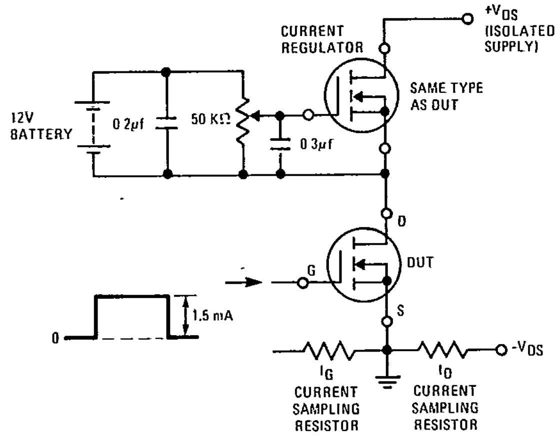


Fig. 18 — Gate Charge Test Circuit

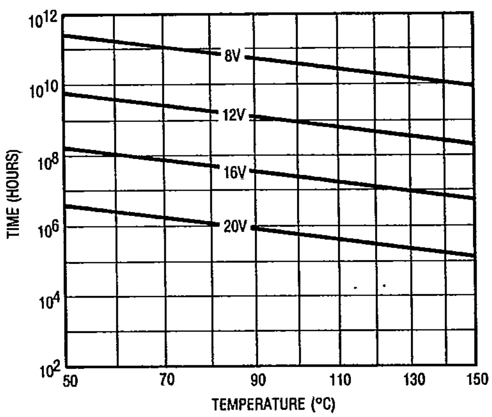


*Fig. 19 — Typical Time to Accumulated 1% Gate Failure

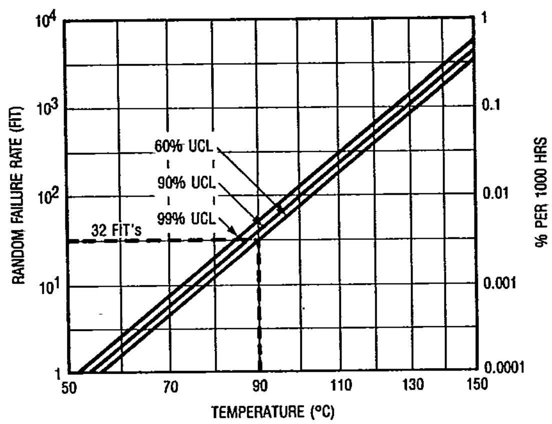


Fig. 20 — Typical High Temperature Reverse Bias (HTRB) Failure Rate

*The data shown is correct as of April 15, 1987. This information is updated on a quarterly basis; for the latest reliability data, please contact your local IR field office.