



HARRIS

IRFP9240R/P9241R

IRFP9242R/P9243R

Avalanche Energy Rated
P-Channel Power MOSFETs

August 1991

T-39-23

Features

- -10A and -12A, -200V and -150V
- $r_{DS(ON)} = 0.50\Omega$ and 0.7Ω
- Single Pulse Avalanche Energy Rated
- SOA Is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

The IRFP9240R, IRFP9241R, IRFP9242R and IRFP9243R are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

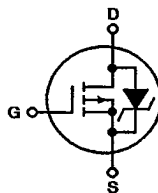
Package

TO-247
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$) Unless Otherwise Specified

	IRFP9240R	IRFP9241R	IRFP9242R	IRFP9243R	UNITS
Drain-Source Voltage (1)	V_{DS} -200	-150	-200	-150	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} -200	-150	-200	-150	V
Continuous Drain Current					
$T_C = 25^\circ\text{C}$	I_D -12	-12	-10	-10	A
$T_C = 100^\circ\text{C}$	I_D -7.5	-7.5	-6.3	-6.3	A
Pulsed Drain Current (3)	I_{DM} -48	-48	-40	-40	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D 150	150	150	150	W
(See Figure 14)					
Linear Derating Factor	1.2	1.2	1.2	1.2	W/ $^\circ\text{C}$
(See Figure 14)					
Single Pulse Avalanche Energy Rating (4)	E_{AS} 790	790	790	790	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
- Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
- $V_{DD} = 50\text{V}$, Start $T_J = +25^\circ\text{C}$, $L = 8.2\text{mH}$, $R_G = 50\Omega$, Peak $I_L = 12\text{A}$ (See Figures 15 and 16)

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
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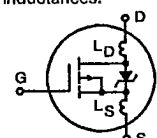
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Specifications IRFP9240R, IRFP9241R, IRFP9242R, IRFP9243R

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

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CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRFP9240R, IRFP9242R	BV _{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-200	-	-	V
IRFP9241R, IRFP9243R			-150	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	$V_{DS} = V_{GS}, I_D = -250\mu A$	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I _{GSS}	$V_{GS} = 20V$	-	-	100	nA
Gate-Source Leakage Reverse	I _{GSS}	$V_{GS} = -20V$	-	-	-100	nA
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$	-	-	-250	μA
		$V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V, T_J = +125^\circ\text{C}$	-	-	-1000	μA
On-State Drain Current (Note 2) IRFP9240R, IRFP9241R	I _{D(ON)}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, V_{GS} = -10V$	-12	-	-	A
			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP9240R, IRFP9241R	r _{DS(ON)}	$V_{GS} = -10V, I_D = -6.3A$	-	0.38	0.50	Ω
			-	0.50	0.70	Ω
Forward Transconductance (Note 2)	g _{fs}	$V_{DS} \leq -50V, I_D = -6.3A$	3.8	5.7	-	S(V)
Input Capacitance	C _{ISS}	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$	-	1400	-	pF
Output Capacitance	C _{OSS}	See Figure 10	-	350	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	140	-	pF
Turn-On Delay Time	t _{d(ON)}	$V_{DD} = -100V, I_D = -12A, R_G = 9.1\Omega$	-	18	22	ns
Rise Time	t _r	See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	45	68	ns
Turn-Off Delay Time	t _{d(OFF)}		-	75	90	ns
Fall Time	t _f		-	29	44	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g	$V_{GS} = -10V, I_D = -12A, V_{DS} = 0.8 \text{ Max Rating}$. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	38	57	nC
Gate-Source Charge	Q _{gs}		-	8.0	-	nC
Gate-Drain ("Miller") Charge	Q _{gd}		-	21	-	nC
Internal Drain Inductance	L _D	Measured between contact screw on header that is closer to source & gate pins & center of die.	-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the source pin, 6mm (0.25") from header & source bonding pad.	-	12.5	-	nH
Junction-to-Case	R _{θJC}		-	-	0.83	$^\circ\text{C/W}$
Case-to-Sink	R _{θCS}	Mounting surface flat, smooth and greased	-	0.1	-	$^\circ\text{C/W}$
Junction-to-Ambient	R _{θJA}	Free Air Operation	-	-	30	$^\circ\text{C/W}$

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Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V _{SD}	$T_J = +25^\circ\text{C}, I_S = -12A, V_{GS} = 0V$	-	-	-1.5	V
Reverse Recovery Time	t _{rr}	$T_J = +25^\circ\text{C}, I_F = -11A, dI_F/dt = 100A/\mu s$	-	210	-	ns
Reverse Recovered Charge	Q _{RR}		-	2.0	-	μC
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES: 1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$ 2. Pulse Test: Pulse width $\leq 300\mu s$,
Duty Cycle $\leq 2\%$ 3. Repetitive Rating: Pulse width limited by max.
junction temperature. See Transient Thermal
Impedance Curve (Figure 5)4. $V_{DD} = 50V$, Start $T_J = +25^\circ\text{C}$, $L = 8.2\text{mH}$,
 $R_G = 50\Omega$, Peak $I_L = 12A$ (See Figures 15
and 16)

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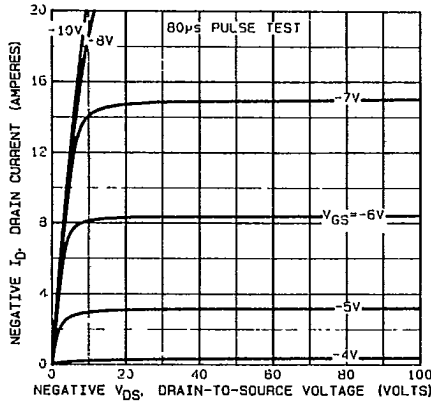


Fig. 1 - Typical output characteristics.

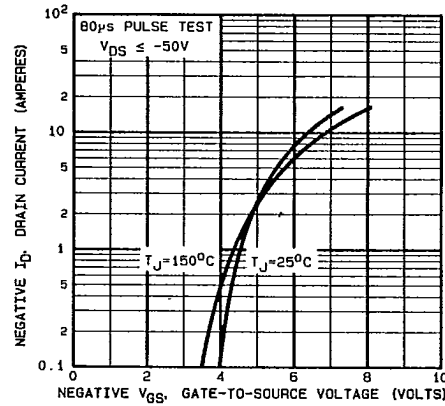


Fig. 2 - Typical transfer characteristics.

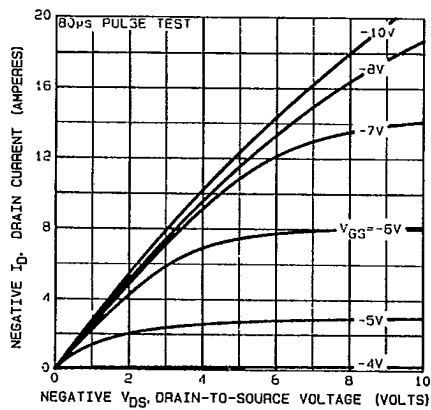


Fig. 3 - Typical saturation characteristics.

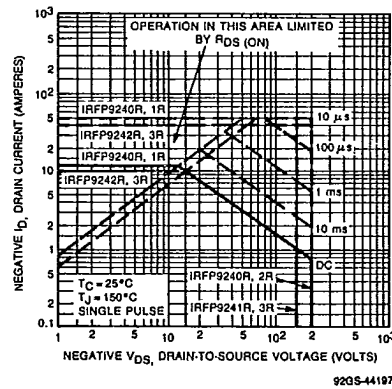


Fig. 4 - Maximum safe operating area.

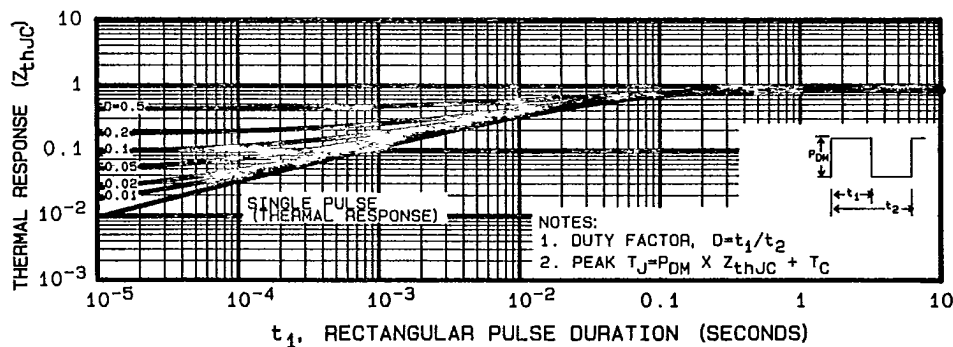


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

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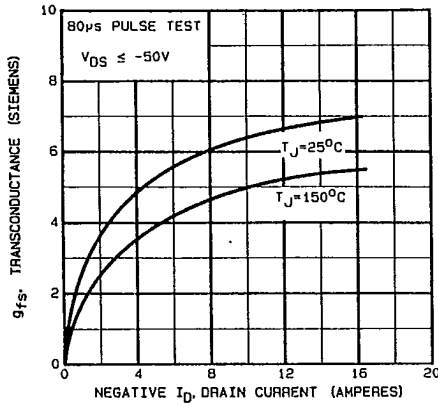


Fig. 6 - Typical transconductance vs. drain current.

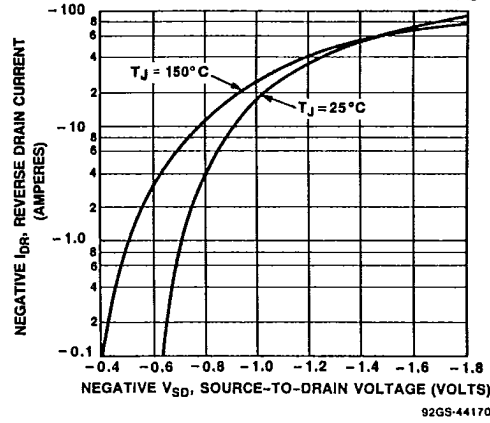


Fig. 7 - Typical source-drain diode forward voltage.

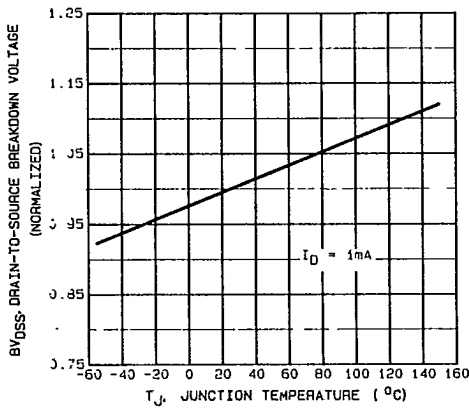


Fig. 8 - Breakdown voltage vs. temperature.

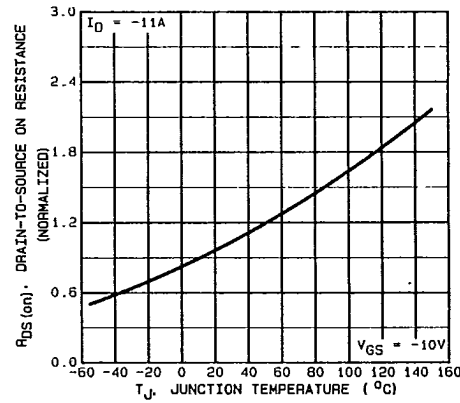


Fig. 9 - Normalized on-resistance vs. temperature.

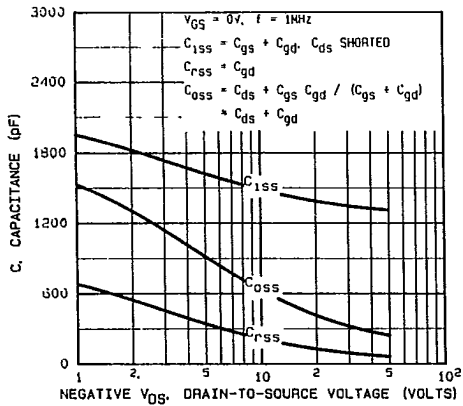


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

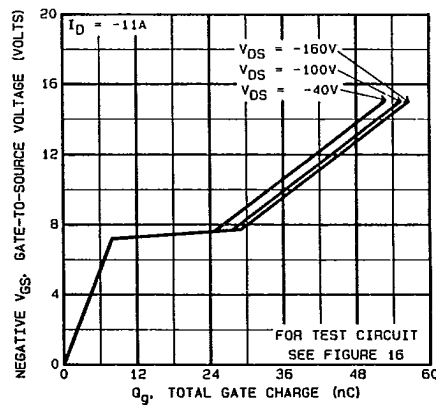


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

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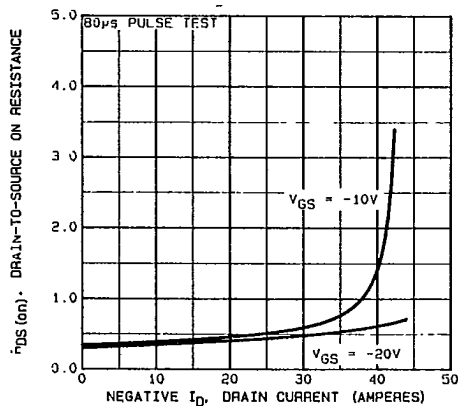


Fig. 12 - Typical on-resistance vs. drain current.

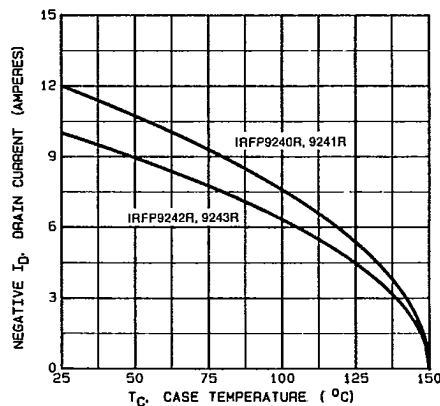


Fig. 13 - Maximum drain current vs. case temperature.

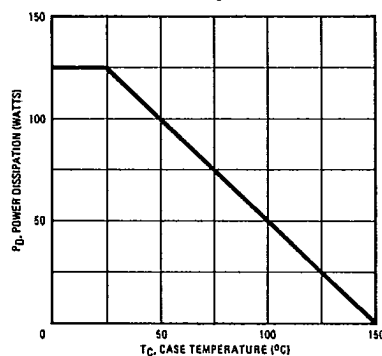


Fig. 14 - Power vs. temperature derating curve.

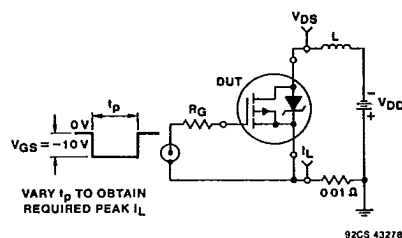


Fig. 15 - Unclamped inductive test circuit.

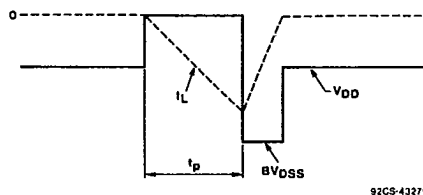


Fig. 16 - Unclamped inductive waveforms.

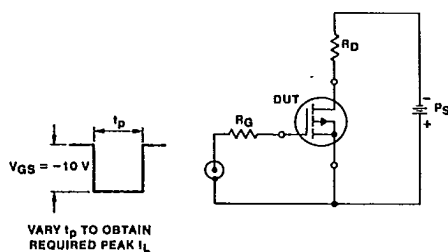


Fig. 17 - Switching time test circuit.

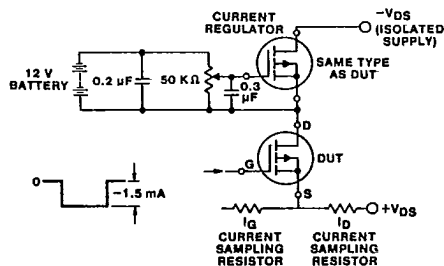


Fig. 18 - Gate charge test circuit.