

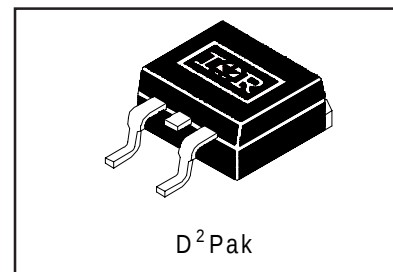
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

V_{DSS}	$R_{ds(on)}$ max	I_D
500V	0.52Ω	11A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified (See AN 1001)



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V ^⑥	11	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V ^⑥	7.0	
I_{DM}	Pulsed Drain Current ^{① ⑥}	44	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ^{③ ⑥}	6.9	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Applicable Off Line SMPS Topologies:

- Two Transistor Forward
- Half & Full Bridge
- Power Factor Correction Boost

Notes ^① through ^⑥ are on page 8

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.060	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.52	Ω	$V_{GS} = 10V, I_D = 6.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	6.1	—	—	S	$V_{DS} = 50V, I_D = 6.6A$ ⑥
Q_g	Total Gate Charge	—	—	52	nC	$I_D = 11A$
Q_{gs}	Gate-to-Source Charge	—	—	13		$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	18		$V_{GS} = 10V$, See Fig. 6 and 13 ④⑥
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	35	—		$I_D = 11A$
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		$R_G = 9.1\Omega$
t_f	Fall Time	—	28	—		$R_D = 22\Omega$, See Fig. 10 ④⑥
C_{iss}	Input Capacitance	—	1423	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	208	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	8.1	—		$f = 1.0MHz$, See Fig. 5⑥
C_{oss}	Output Capacitance	—	2000	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	55	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	97	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤⑥

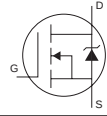
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②⑥	—	275	mJ
I_{AR}	Avalanche Current①	—	11	A
E_{AR}	Repetitive Avalanche Energy①	—	17	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	44		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 11A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	510	770	ns	$T_J = 25^\circ\text{C}, I_F = 11A$
Q_{rr}	Reverse Recovery Charge	—	3.4	5.1	μC	$di/dt = 100A/\mu s$ ④⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

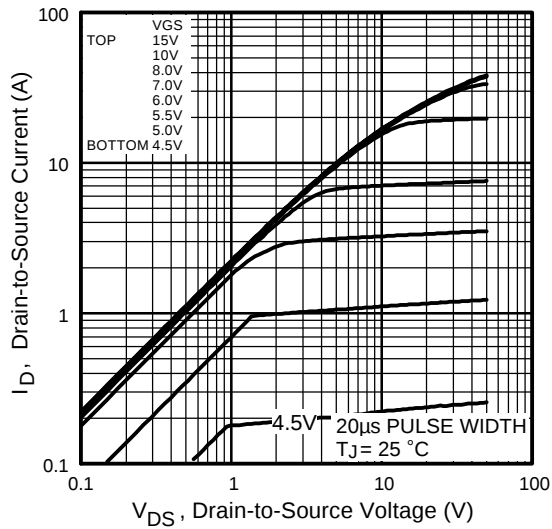


Fig 1. Typical Output Characteristics

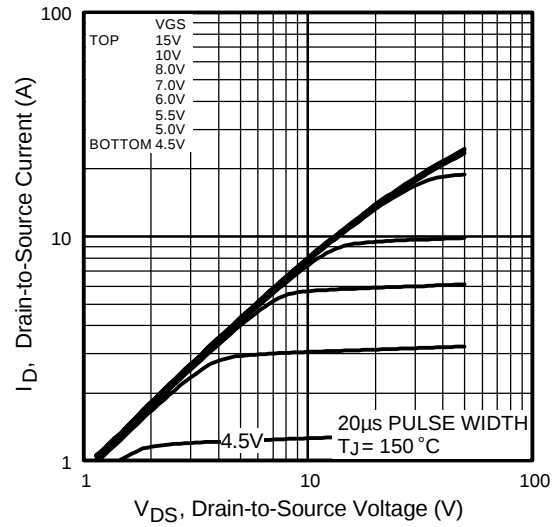


Fig 2. Typical Output Characteristics

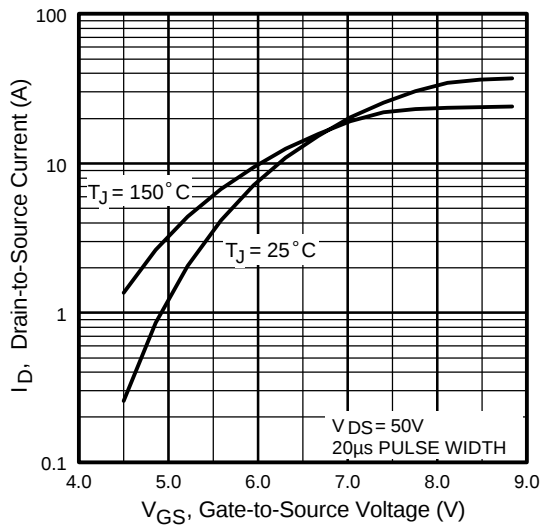


Fig 3. Typical Transfer Characteristics

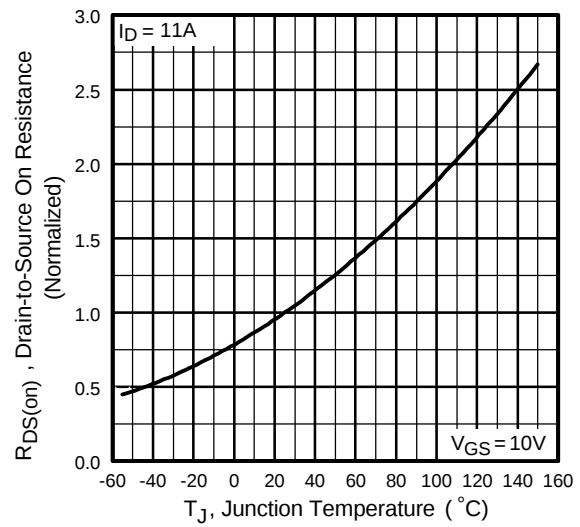
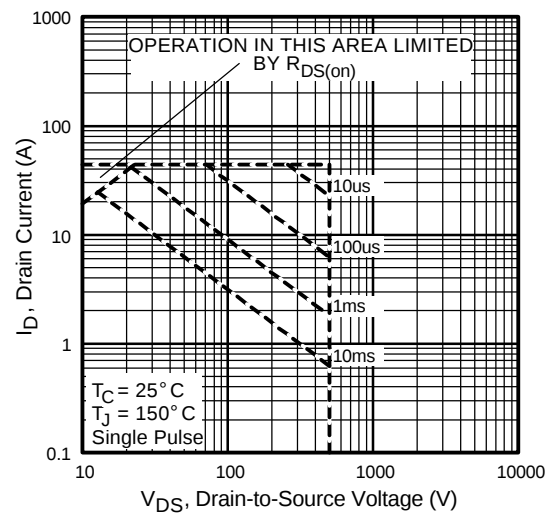
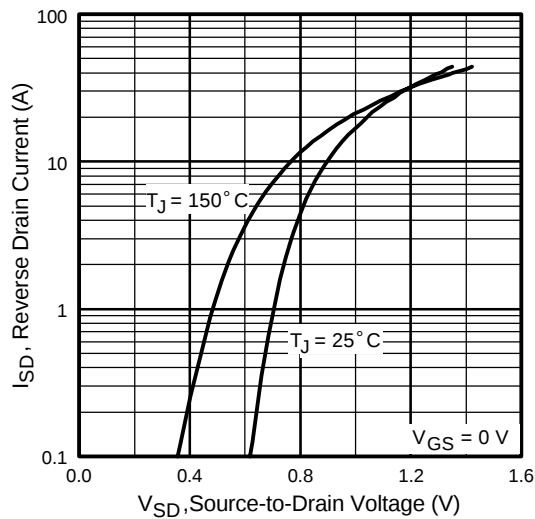
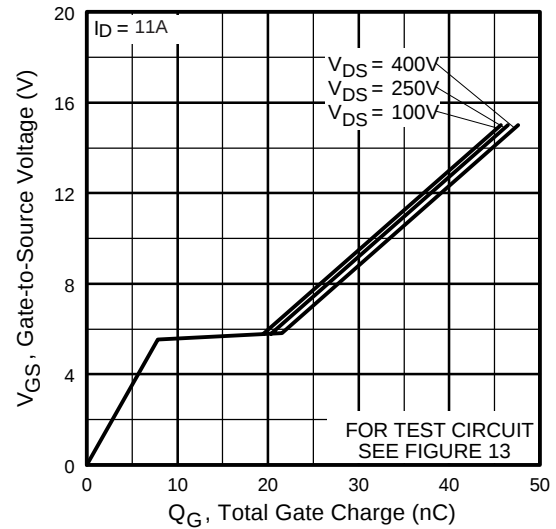
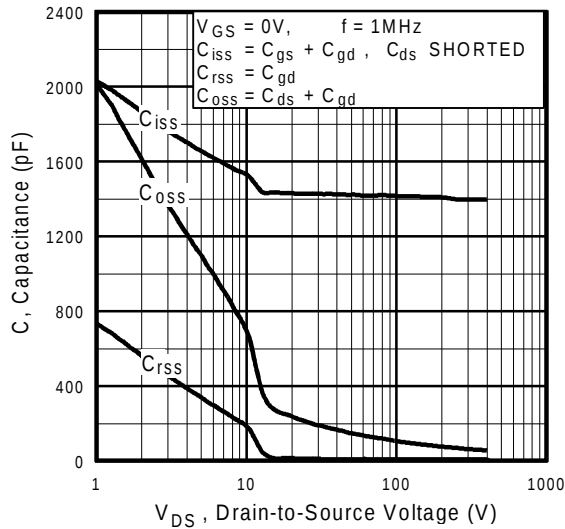


Fig 4. Normalized On-Resistance Vs. Temperature

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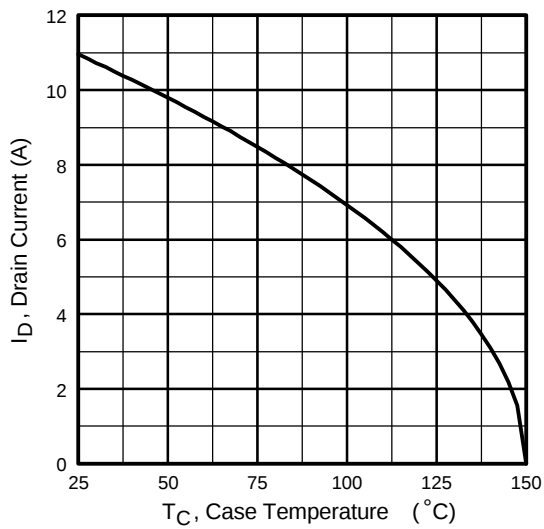


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

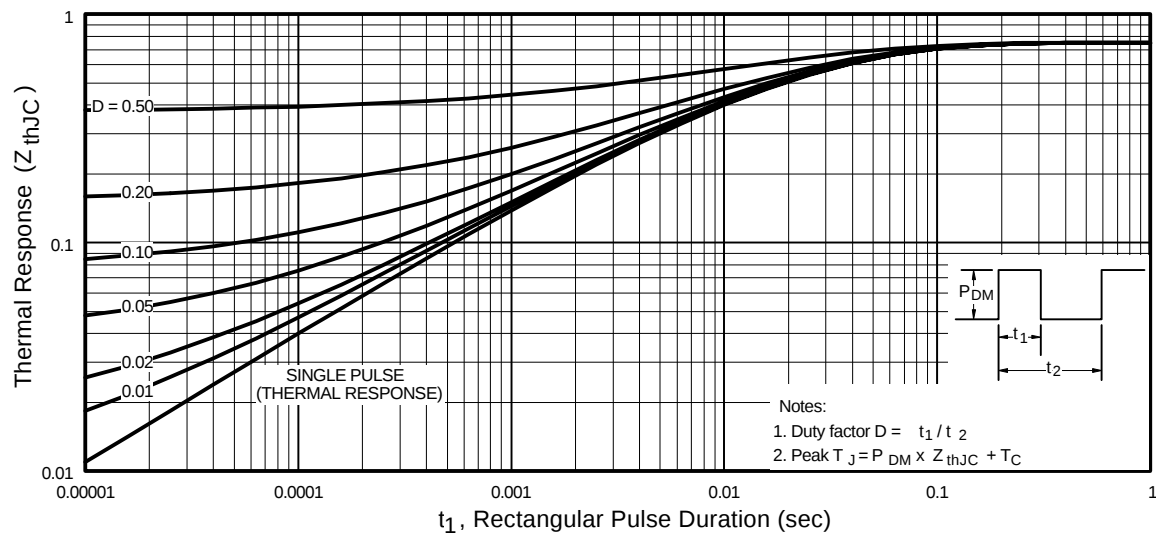


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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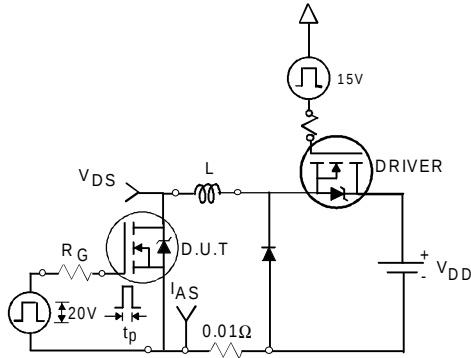


Fig 12a. Unclamped Inductive Test Circuit

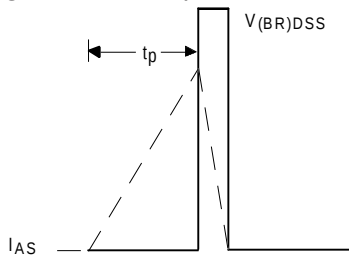


Fig 12b. Unclamped Inductive Waveforms

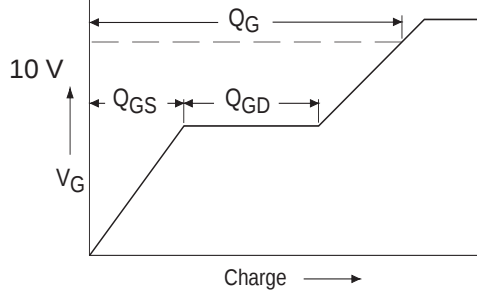


Fig 13a. Basic Gate Charge Test Circuit

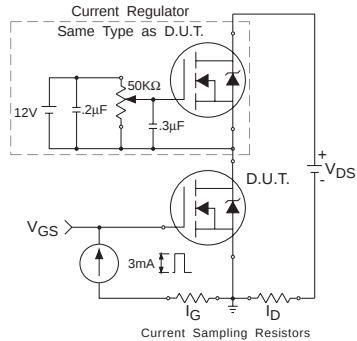


Fig 13b. Gate Charge Test Circuit

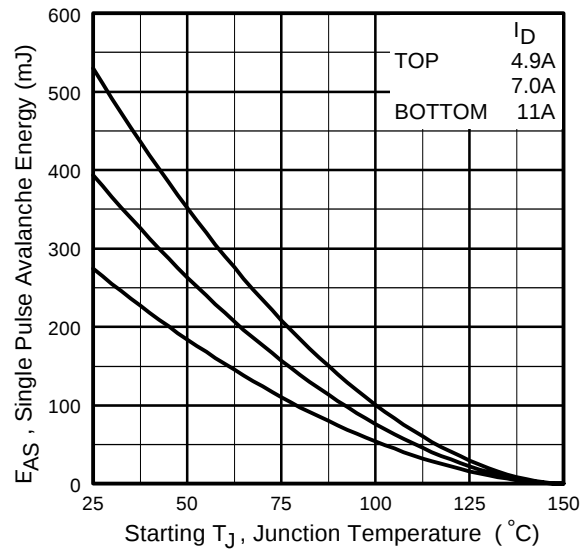


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

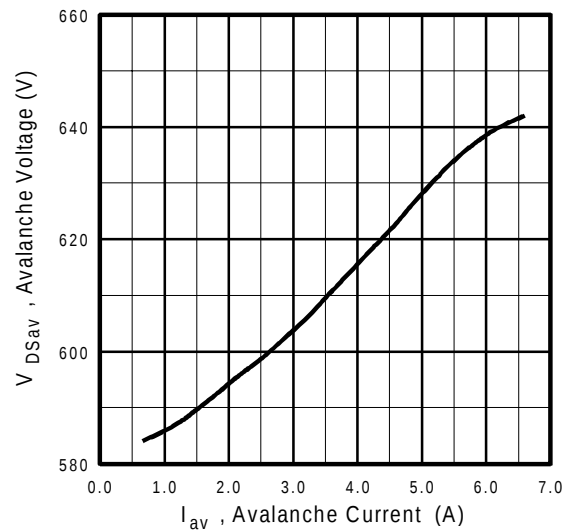


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

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Peak Diode Recovery dv/dt Test Circuit



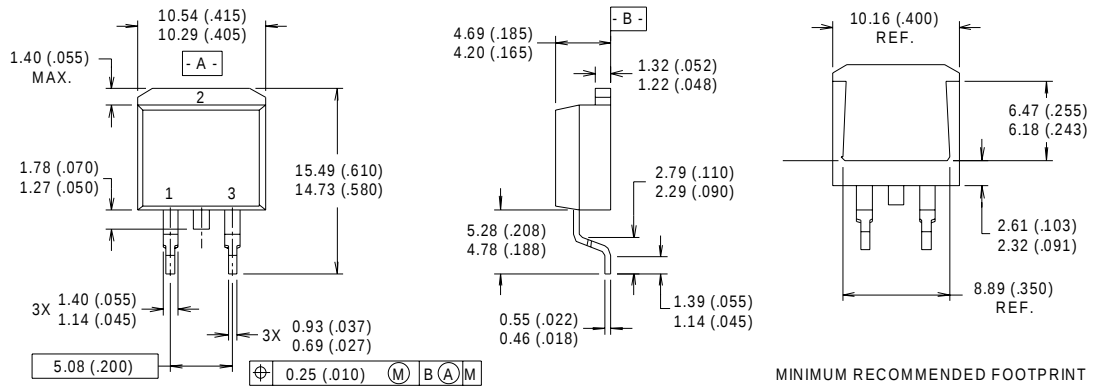
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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D²Pak Package Outline



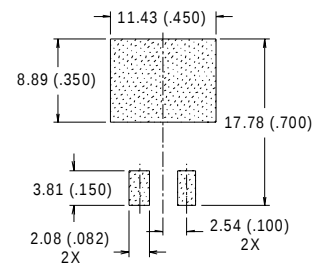
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

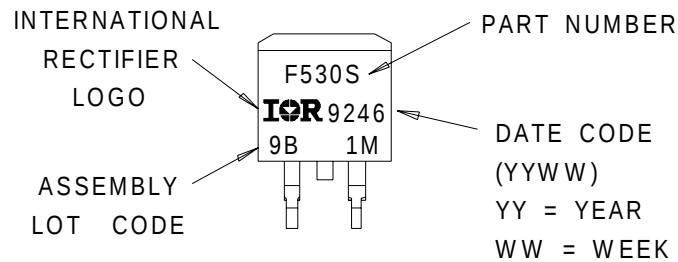
- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



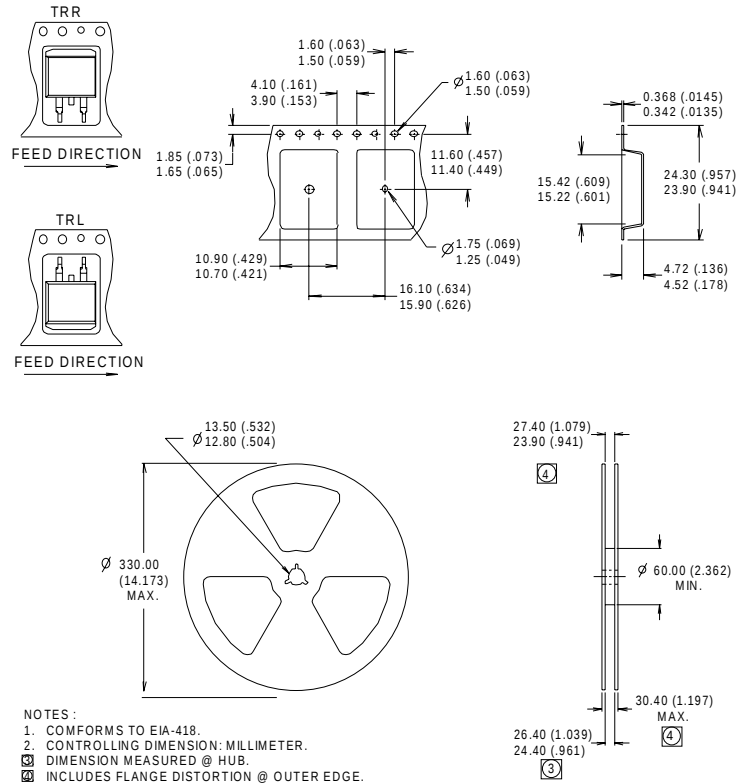
Part Marking Information

D²Pak



Tape & Reel Information

D²Pak



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 4.5\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 11\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 11\text{A}$, $di/dt \leq 140\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Uses IRFB11N50A data and test conditions