

INTERNATIONAL RECTIFIER

Preliminary Data Sheet No. PD-9.479A

T-39-13

INTERNATIONAL RECTIFIER **IR**

HEXFET® TRANSISTORS

IRH450

RAD HARD

500 Volt, 0.6Ω, Rad Hard HEXFET

International Rectifier's RAD HARD HEXFETs demonstrate excellent threshold voltage stability and breakdown voltage stability at total radiation doses as high as 1 megarad. In addition, these devices are capable of surviving transient ionization pulses as high as 1×10^{12} rads (Si)/sec, and return to normal operation within a few microseconds. Single Event Upset (SEU) testing of International Rectifier RAD HARD HEXFETs has demonstrated virtual immunity to SEU failure. Since RAD HARD HEXFETs use International Rectifier's HEXFET technology, the user can expect the highest quality and reliability in the industry.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

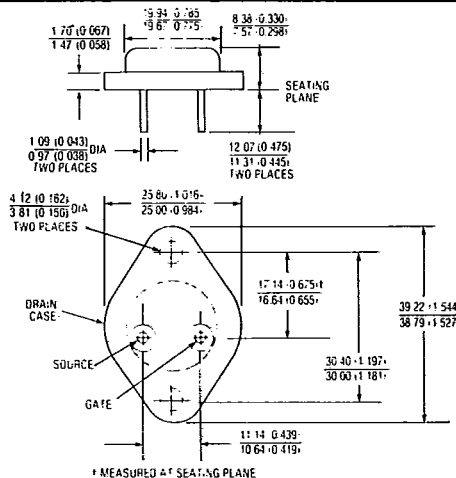
Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRH450	500V	0.6Ω	10A

FEATURES:

- Radiation Hard
- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling

CASE STYLE AND DIMENSIONS



Conforms to JEDEC Outline TO-204AA (Modified TO-3)
Dimensions in Millimeters and (Inches)

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IRH450 Device
INTERNATIONAL RECTIFIER
Pre-Radiation①
T-39-13
Pre-Radiation Absolute Maximum Ratings

Parameter	IRH450	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current	10
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current	6.4
I_{DM}	Pulsed Drain Current ②	40
$P_D @ T_C = 25^\circ\text{C}$	Max. Power Dissipation	150
	Linear Derating Factor	1.2
V_{GS}	Gate-to-Source Voltage	± 20
E_{AS}	Single Pulse Avalanche Energy ③	1100 (See Fig. 26)
I_{AR}	Repetitive Avalanche Current ②	10 (See Energy Limitations)
E_{AR}	Repetitive Avalanche Energy ②	15 (See Current Limitations)
dV/dt	Peak Commutating dV/dt ④	3.5 (See Fig. 29)
T_J	Operating Junction	-55 to 150
T_{STG}	Storage Temperature Range	
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)

Pre-Radiation Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions	
BV _{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} = 0V, I _D = 1 mA	
R _{DS(on)}	Static Drain-to-Source On-State Resistance ⑤	—	0.50	0.60	Ω	V _{GS} = 12V, I _D = 5.0A	
I _{D(on)}	On-State Drain Current ⑤	10	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} Max. V _{GS} = 12V	
V _{GS(th)}	Gate Threshold Voltage	2.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 1 mA	
g _{fs}	Forward Transconductance ⑤	3.0	4.6	—	S (⑥)	V _{DS} = 10V, I _D = 5A	
I _{DSS}	Zero Gate Voltage Drain Current	—	—	1	mA	V _{DS} = 500V, V _{GS} = 0V	
		—	—	1		V _{DS} = 400V V _{GS} = 0V, T _C = 125°C	
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V	
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	−100	nA	V _{GS} = 20V	
Q _g	Total Gate Charge	—	100	150	nC	V _{GS} = 12V, I _D = 10A	
Q _{gs}	Gate-to-Source Charge	—	20	30	nC	V _{DS} = 400V See Fig. 28	
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	41	62	nC	(Independent of operating temperature)	
t _{d(on)}	Turn-On Delay Time	—	24	—	ns	V _{DD} = 250V, I _D ≈ 10A, R _G = 6.2Ω	
t _r	Rise Time	—	32	—	ns	R _D = 24Ω	
t _{d(off)}	Turn-Off Delay Time	—	77	—	ns	See Fig. 27	
t _f	Fall Time	—	27	—	ns	(Independent of operating temperature)	
L _D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.	Modified MOSFET symbol showing the internal inductances.
L _S	Internal Source Inductance	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.	
C _{iss}	Input Capacitance	—	3600	—	pF	V _{GS} = 0V, V _{DS} = 25V	
C _{oss}	Output Capacitance	—	330	—	pF	f = 1.0 MHz	
C _{rss}	Reverse Transfer Capacitance	—	62	—	pF	See Fig. 22	

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	10	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier. 
I _{SM}	Pulse Source Current (Body Diode) ④	—	—	40	A	
V _{SD}	Diode Forward Voltage ⑤	—	—	1.4	V	T _C = 25°C, I _S = 10A, V _{GS} = 0V
t _{rr}	Reverse Recovery Time	—	530	1100	ns	T _J = 25°C, I _F = 10A, dI _F /dt = 100 A/μs
Q _{RR}	Reverse Recovery Charge	—	7.5	16	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	0.83	K/W	
R_{thCS}	Case-to-Sink	—	0.12	—	K/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	—	—	30	K/W	Typical socket mount

Radiation Performance of Rad Hard HEXFETs

International Rectifier Radiation Hard (Rad Hard) HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier uses two radiation environments. Every manufacturing lot is tested in low dose rate ("total dose") and high dose rate ("gamma dot") environments.

Low dose rate testing is performed following MIL-STD-750C, test method 1019. Refer to notes ⑥ and ⑦. The lot is evaluated with two different test circuits. Device performance is presented in table 1. The values in table 1 will be met for either of the two low dose rate test circuits that are used. In addition, Rad Hard HEXFETs have been characterized for their post radiation response. Typical curves showing radiation response as well as post radiation response appear in figures 1 through 8.

The two test circuits used during low dose rate exposures are shown in figure 11. The first test circuit biases the gate electrode at 12 volts with respect to the

drain and source electrodes (see fig. 11a). In general, a 12 volt V_{GS} steady state bias is a worst case condition for the "on-state" parameters of the device (eg. $V_{GS(th)}$, $R_{DS(on)}$, g_{fs} , etc.). The second test circuit biases the drain electrode with respect to the source and gate electrodes at 80% of the rated BV_{DSS} (pre-radiation) (fig. 11b). The steady state V_{DSS} bias equal to 80% of the rated BV_{DSS} (pre-radiation) is considered a worst case test condition for BV_{DSS} (post-radiation).

High dose rate (gamma-dot) testing is done using a dose rate set at $1.5-2.0 \times 10^{12}$ rads(Si)/sec. The device is exposed to this dose rate with specified percentage of the BV_{DSS} voltage applied. Characterization will be determined at a later date. The test circuit used for this test is shown in figure 12.

In addition to these tests, Radiation Hard HEXFETs have been characterized in neutron and heavy ion SEU environments (see fig 9 and table 3 respectively).

Table 1. Low Dose Rate

Parameter ⑥ ⑦		100K Rads (Si)		250K Rads (Si)	500K Rads (Si)	1000K Rads (Si)	Units	Test Conditions
		Min.	Max.					
V _{GS(th)}	Gate Threshold Voltage	1	6	See Fig. 1 & 6			V	V _{GS} = V _{DS} , I _D = 1 mA
R _{DS(on)}	Static Drain-to-Source On State Resistance	—	0.640	⑩			Ω	V _{GS} = 12V, I _D = 5A
g _{fs}	Forward Transconductance ⑤	2.60	—	See Fig. 2			S (⑩)	V _{DS} = 10V, I _D = 5A
I _{D(on)}	On-State Drain Current ⑤	9.5 Min. @ T _C = 25°C 5 Min. @ T _C = 100°C		See Fig. 3 & 7			A	V _{GS} = 12V, V _{DS} = V _{GS}
BV _{DSS}	Drain-to-Source Breakdown Voltage	400 Min.		See Fig. 4			V	V _{GS} = 0, I _D = 1 mA
I _{DSS}	Zero Gate Voltage Drain Current	1 Max.		See Fig. 5 & 8			mA	V _{DS} = 400V, V _{GS} = 0V
I _{GSS}	Gate-to-Source Leakage Forward	100 Max.		100 Max.			nA	V _{GS} = ±20V
V _{SD}	Diode Forward Voltage ⑤	1.4 Max.		1.4 Max.			V	T _C = 25°C, I _S = 9.5A, V _{GS} = 0V

Table 2. High Dose Rate

Parameter ⑧	10 ¹¹ (Rads (Si)/sec)			10 ¹² (Rads (Si)/sec)			Units	Test Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{DSS} Drain-to-Source Voltage	⑩			⑩			V	Applied drain-to-source voltage during gamma-dot
I_{PP}	⑩			⑩			A	Peak radiation induced photo-current
di/dt	⑩			⑩			A/ μ sec	Rate of rise of photo-current
L_1	⑩			⑩			μ H	Circuit inductance required to limit di/dt

Table 3. Single Event Upset

Parameter	Typ.	Units	Test Conditions		
			Ion	LET (Si) (MeV/mg/cm ²)	Range (μ m)
V_{DS} ⑨	210	V	Copper	30	~40

① See Figures 13 through 29 for pre-radiation curves.

② Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 17)

③ @ $V_{DD} = 50V$, Starting $T_J = 25^\circ C$, $L = 20$ mH, $R_G = 25\Omega$, Peak $I_L = 10A$.

④ $I_{SD} \leq 10A$, $di/dt \leq 130$ A/ μ s, $V_{DD} \leq BV_{DSS}$, Suggested $R_G = 6.2\Omega$

⑤ Pulse width $\leq 300 \mu$ s; Duty Cycle $\leq 2\%$

⑥ High Total Dose Irradiation with V_{GS} Bias. +12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750C, method 1019. (See figure 11a)

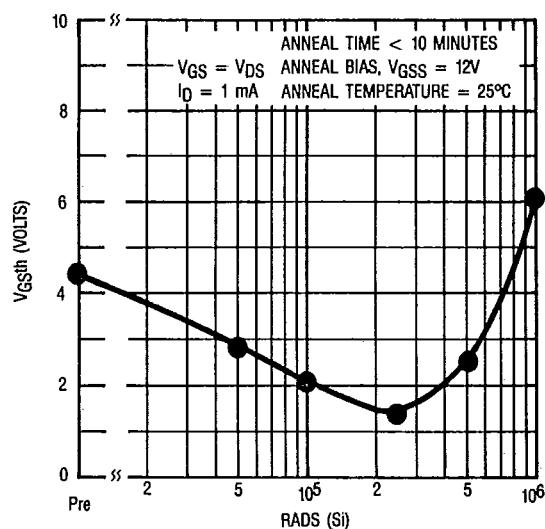
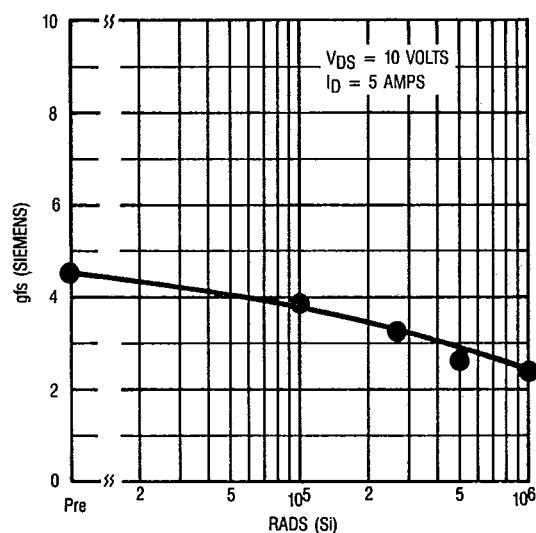
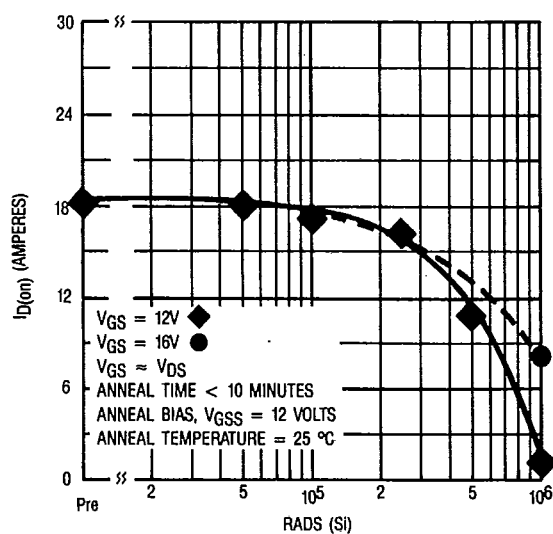
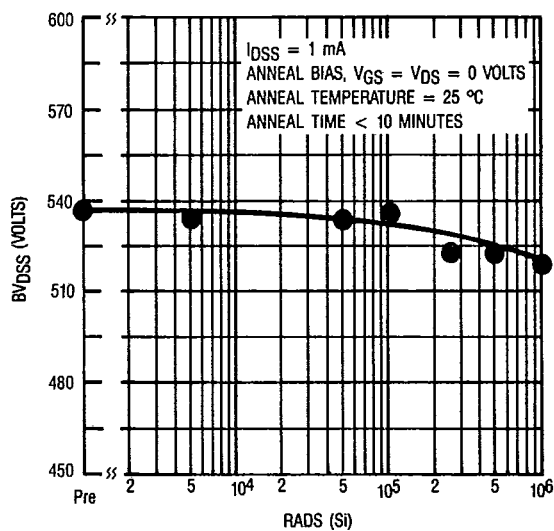
⑦ High Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 0.8$ rated BV_{DSS} (pre-radiation) applied and $V_{GS} = 0$ during irradiation per MIL-STD-750C, method 1019. (See figure 11b)

⑧ This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 MeV). See figure 12.

⑨ Study sponsored by NASA. 210 volts was the maximum available voltage source during the test.

⑩ To be determined



Fig. 1 — Typical Response of Gate Threshold Voltage Vs. Total Dose Exposure^⑤Fig. 2 — Typical Response of Transconductance Vs. Total Dose Exposure^⑤Fig. 3 — Typical Response of On-State Drain Current Vs. Total Dose Exposure^⑥Fig. 4 — Typical Response of Drain-to-Source Breakdown Vs. Total Dose Exposure^⑥

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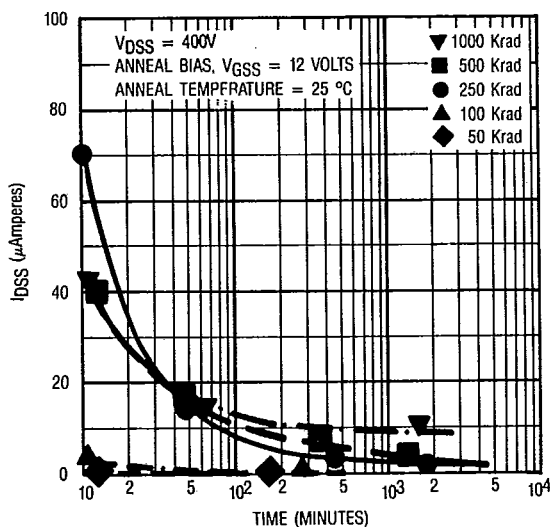
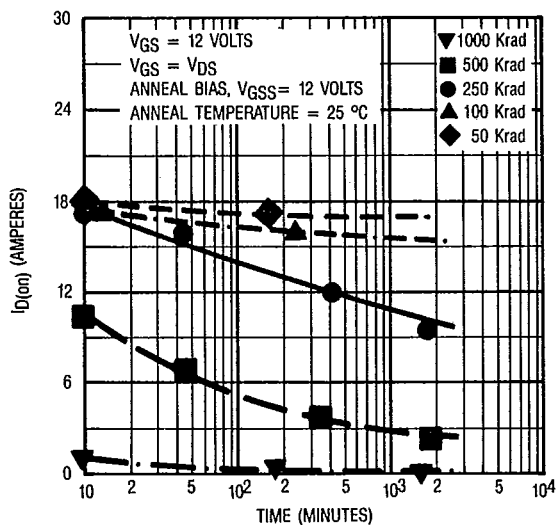
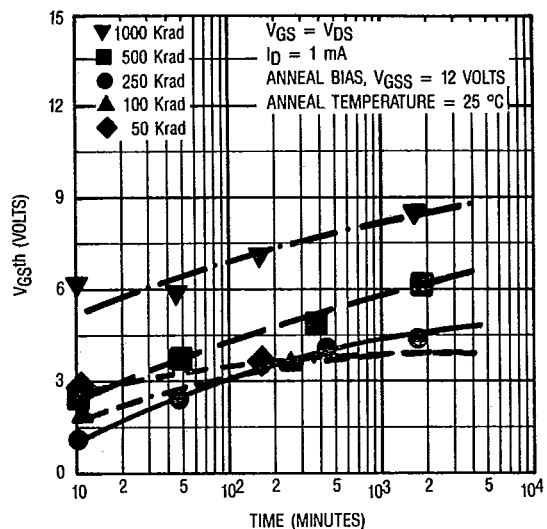
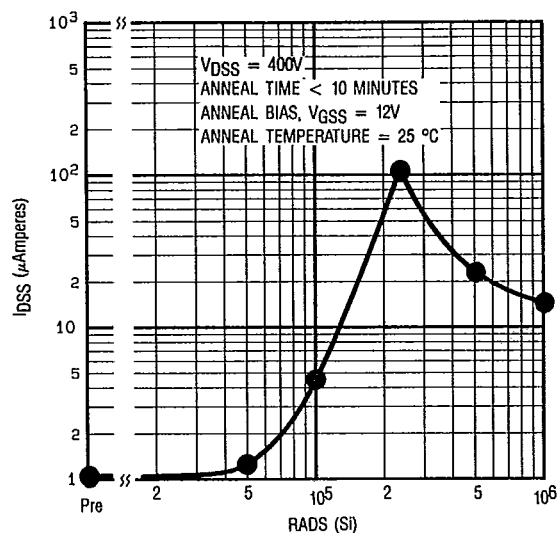


Fig. 7 — Typical Post Radiation Annealing Response of On-State Drain Current Vs. Time ⑤

Fig. 8 — Typical Post Radiation Annealing Response of Zero Gate Voltage Drain Current Vs. Time ⑤

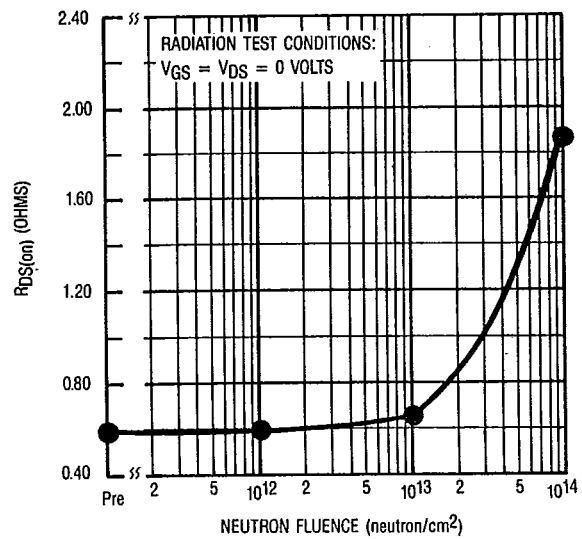


Fig. 9 — On Resistance Vs. Neutron Fluence Level

Data Not Yet Available

Fig. 10 — Typical Transient Response of Rad Hard HEXFET During 1×10^{12} Rad (Si)/Sec Exposure

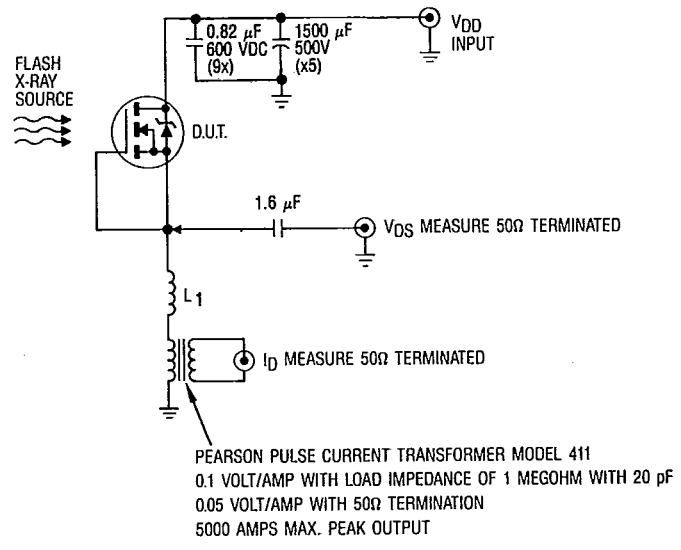
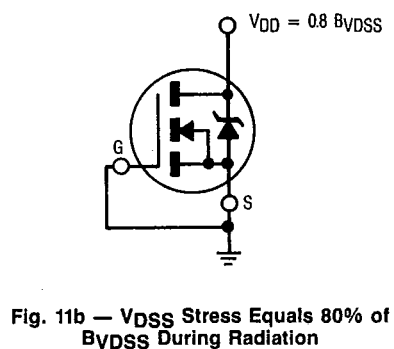
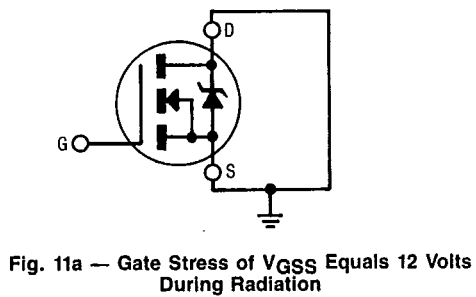


Fig. 12 — High Dose Rate (Gamma Dot) Test Circuit

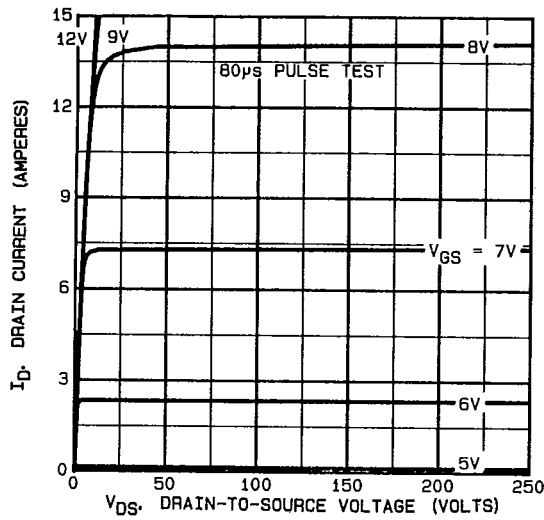


Fig. 13 — Typical Output Characteristics

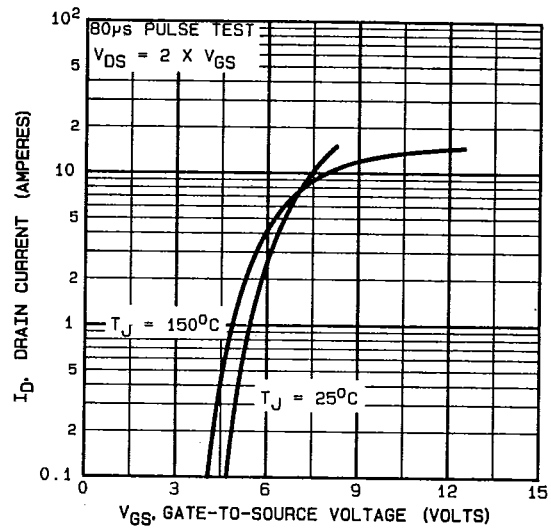


Fig. 14 — Typical Transfer Characteristics

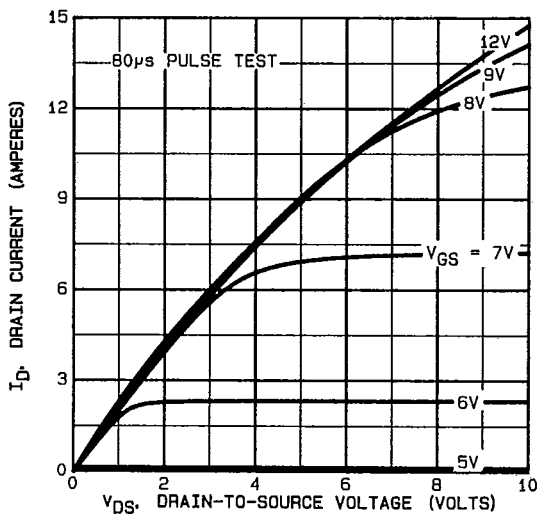


Fig. 15 — Typical Saturation Characteristics

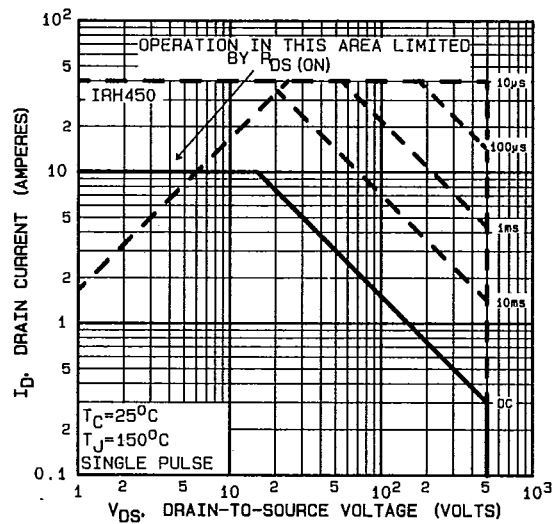


Fig. 16 — Maximum Safe Operating Area

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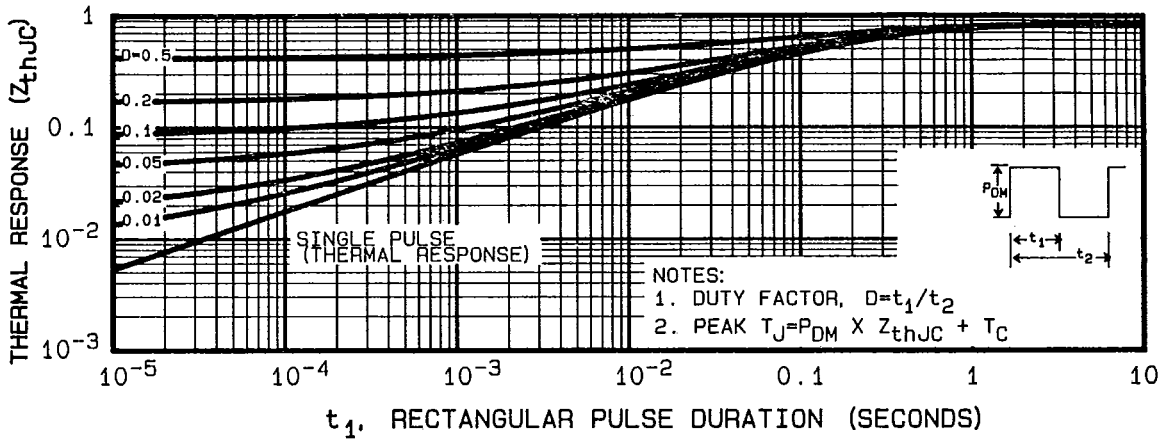


Fig. 17 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

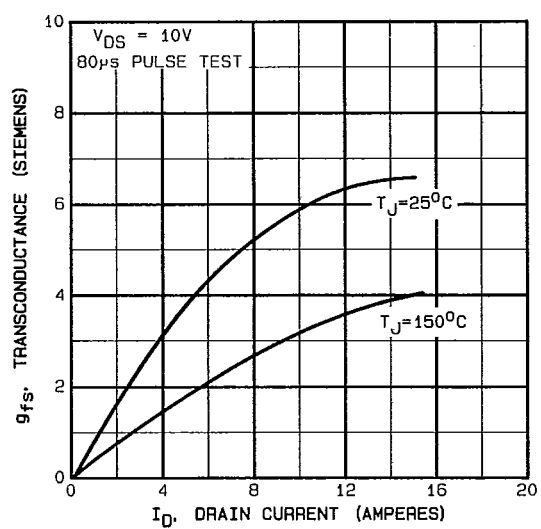


Fig. 18 — Typical Transconductance Vs. Drain Current

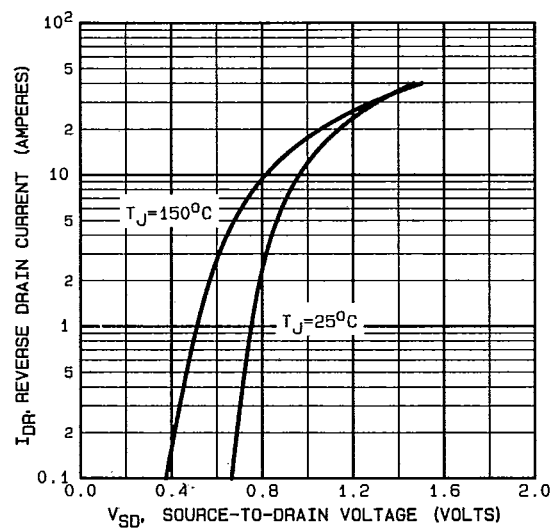


Fig. 19 — Typical Source-Drain Diode Forward Voltage

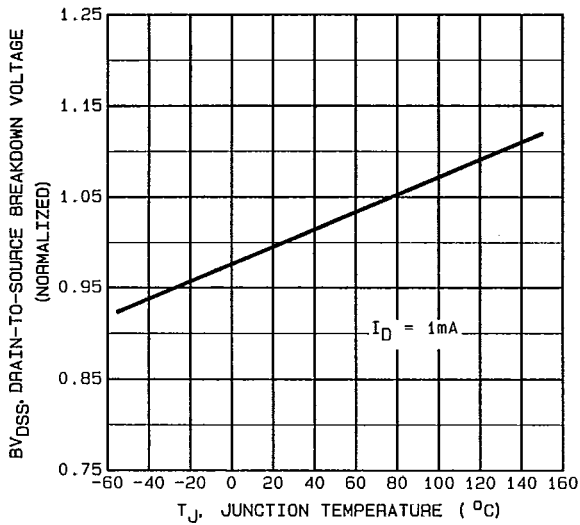


Fig. 20 — Breakdown Voltage Vs. Temperature

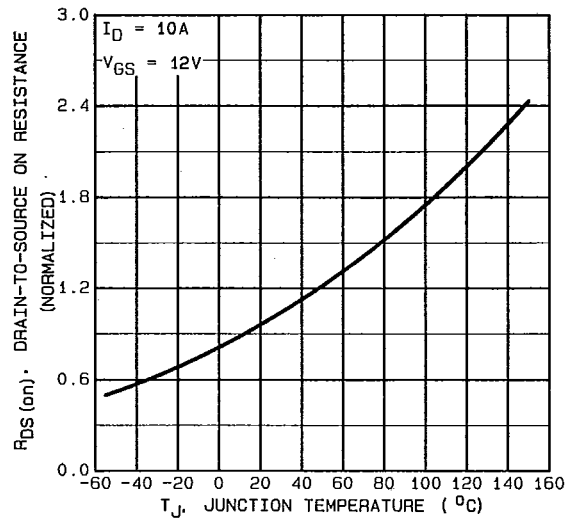


Fig. 21 — Normalized On-Resistance Vs. Temperature

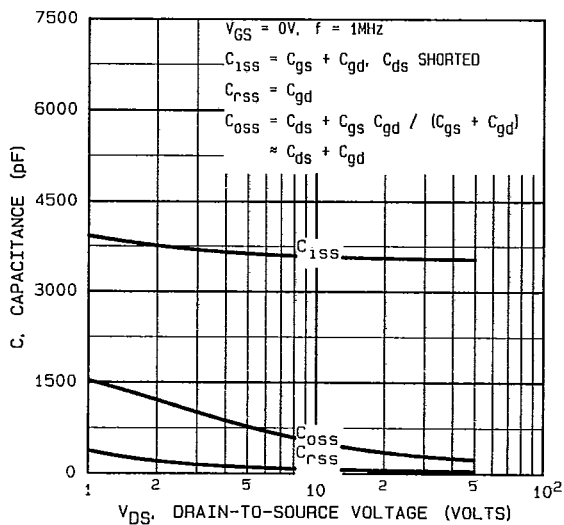


Fig. 22 — Typical Capacitance Vs. Drain-to-Source Voltage

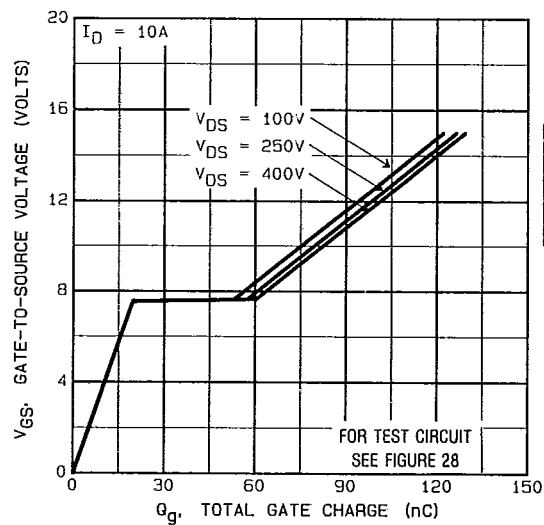


Fig. 23 — Typical Gate Charge Vs. Gate-to-Source Voltage

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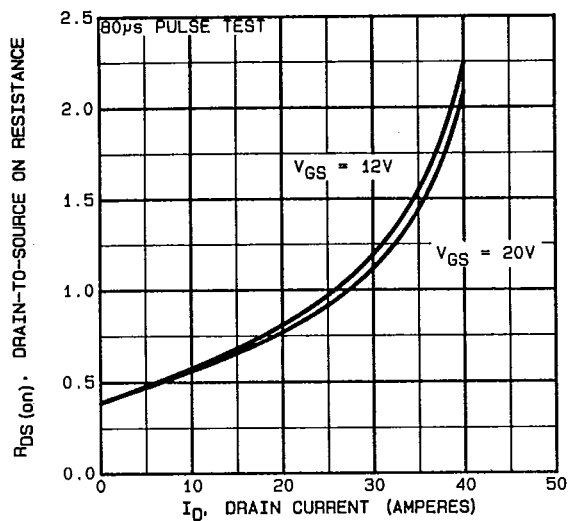


Fig. 24 — Typical On-Resistance Vs. Drain Current

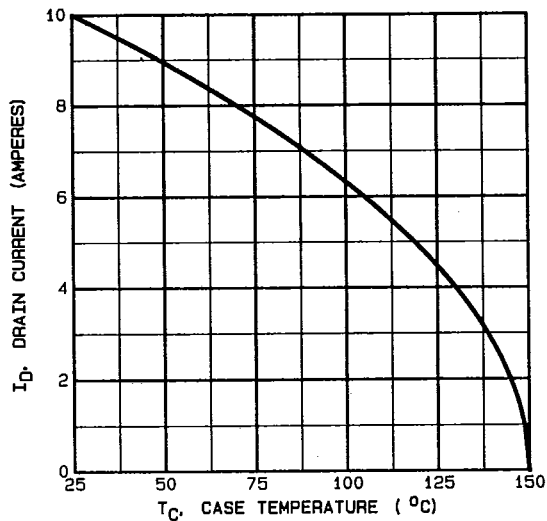


Fig. 25 — Maximum Drain Current Vs. Case Temperature

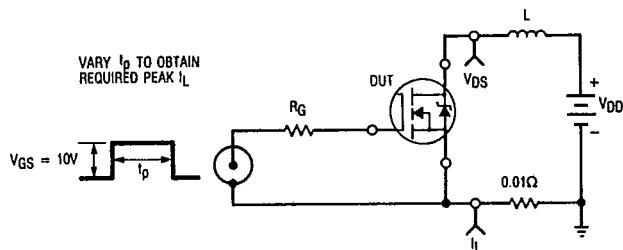


Fig. 26a — Avalanche Inductive Test Circuit

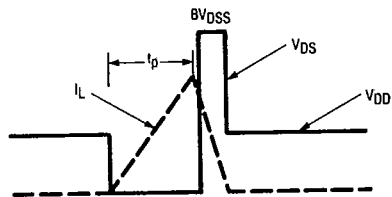


Fig. 26b — Avalanche Inductive Load Test Waveforms

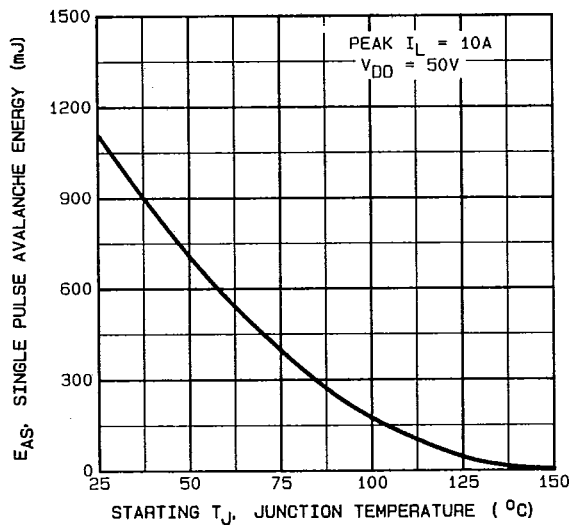


Fig. 26c — Typical Avalanche Vs. Starting Junction Temperature

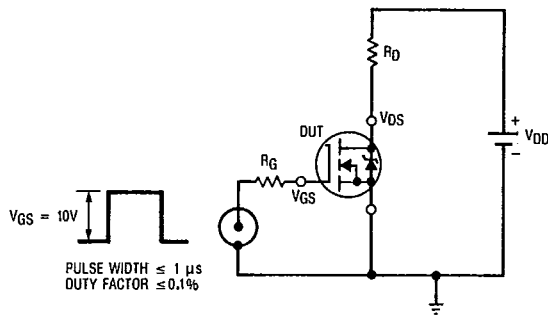


Fig. 27a — Switching Time Test Circuit

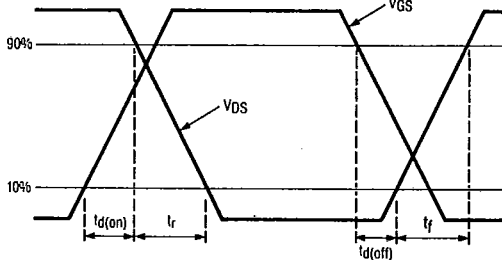


Fig. 27b — Switching Time Waveforms

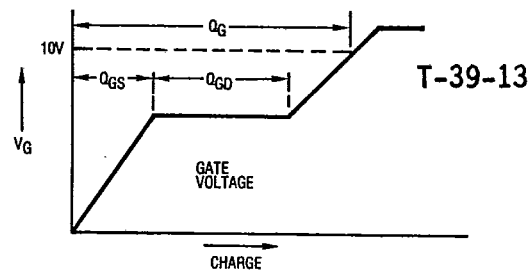


Fig. 28a — Basic Gate Charge Waveform

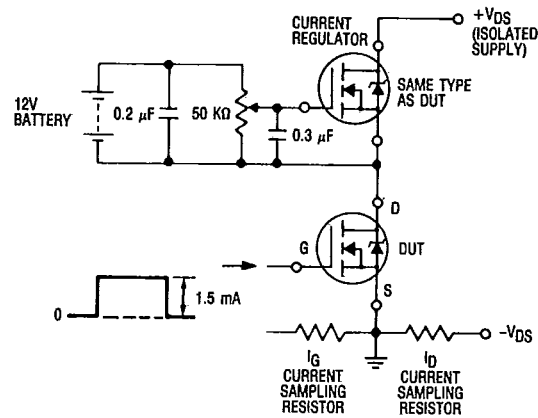
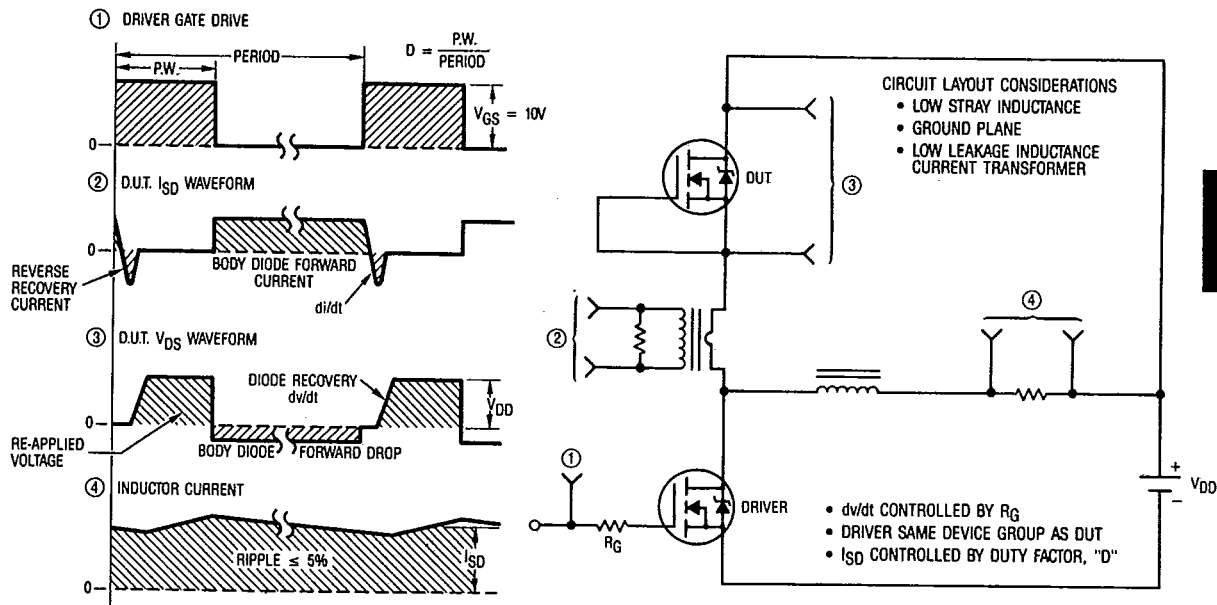


Fig. 28b — Gate Charge Test Circuit

Fig. 29 — Peak Commutating dv/dt Test Circuit