

US5U1

Silicon N-channel MOSFET /
Schottky barrier diode

- 1) Nch MOSFET and schottky barrier diode are put in TUMT5 package.
- 2) High-speed switching, Low On-resistance.
- 3) Low voltage drive (2.5V drive).
- 4) Built-in Low V_F schottky barrier diode.

Technical drawing of the TUMT5 microswitch showing top and side views with dimensions.

Top View Dimensions:

- Overall width: 2.0
- Distance from left edge to center of pin (1): 0.65
- Distance from center of pin (1) to center of pin (2): 1.3
- Distance from center of pin (2) to center of pin (3): 0.65
- Distance from center of pin (3) to right edge: 0.62
- Pin diameter: 0.3
- Pin (1) is located 0.2 from the bottom edge.
- Pin (2) is located 0.3 from the bottom edge.
- Pin (3) is located 0.3 from the bottom edge.

Side View Dimensions:

- Maximum height: 0.85 Max.
- Distance from top edge to center of pin (4): 0.77
- Pin (4) diameter: 0.28 Max.
- Pin (4) height: 0 - 0.1
- Base thickness: 0.17

Switching

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US5U1		○

(1) Gate
(2) Source
(3) Anode
(4) Cathode
(5) Drain

*1 ESD protection diode
*2 Body diode

<MOSFET>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V _{DSS}	30	V
Gate-source voltage		V _{GSS}	12	V
Drain current	Continuous	I _D	±1.5	A
	Pulsed	I _{DP} ^{*1}	±6.0	A
Source current (Body diode)	Continuous	I _S	0.75	A
	Pulsed	I _{SP} ^{*1}	6.0	A
Power dissipation		P _D ^{*2}	0.7	W / ELEMENT
Channel temperature		T _{ch}	150	°C

*1 $P_w \leq 10 \mu s$, Duty cycles $\leq 1\%$
*2 Mounted on a ceramic board

Parameter	Symbol	Limits	Unit
Repetitive peak reverse voltage	V_{RM}	30	V
Reverse voltage	V_R	20	V
Forward current	I_F	0.5	A
Forward current surge peak	I_{FSM}^{*1}	2.0	A
Power dissipation	P_D^{*2}	0.5	W / ELEMENT
Junction temperature	T_J	150	°C

*1 60Hz・1cycle
*2 Mounted on ceramic board

Transistors

<MOSFET and Di>

Parameter	Symbol	Limits	Unit
Total power dissipation	P_D *1	1.0	W / TOTAL
Range of storage temperature	Tstg	-55 to +150	°C

*1 Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<MOSFET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	10	μA	$V_{GS}=12V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR) DSS}$	30	—	—	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.5	—	1.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	170	240	mΩ	$I_D=1.5A, V_{GS}=4.5V$
		—	180	250	mΩ	$I_D=1.5A, V_{GS}=4V$
		—	240	340	mΩ	$I_D=1.5A, V_{GS}=2.5V$
Forward transfer admittance	$ Y_{fs} $ *	1.5	—	—	S	$V_{DS}=10V, I_D=1.5A$
Input capacitance	C_{iss}	—	80	—	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	—	14	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	12	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	7	—	ns	$V_{DD} \doteq 15V$ $I_D=0.75A$
Rise time	t_r *	—	9	—	ns	$V_{GS}=4.5V$
Turn-off delay time	$t_{d(off)}$ *	—	15	—	ns	$R_L=20\Omega$
Fall time	t_f *	—	6	—	ns	$R_G=10\Omega$
Total gate charge	Q_g *	—	1.6	2.2	nC	$V_{DD} \doteq 15V, V_{GS}=4.5V$
Gate-source charge	Q_{gs} *	—	0.5	—	nC	$I_D=1.5A$
Gate-drain charge	Q_{gd} *	—	0.3	—	nC	$R_L=10\Omega, R_G=10\Omega$

*Pulsed

<Body diode characteristics (Source-drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	—	—	1.2	V	$I_S=0.75A, V_{GS}=0V$

<Di>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_F	—	—	0.36	V	$I_S=0.1A$
		—	—	0.47	V	$I_S=0.5A$
Reverse current	I_R	—	—	100	μA	$I_S=20V$

Transistors

●Electrical characteristics curves

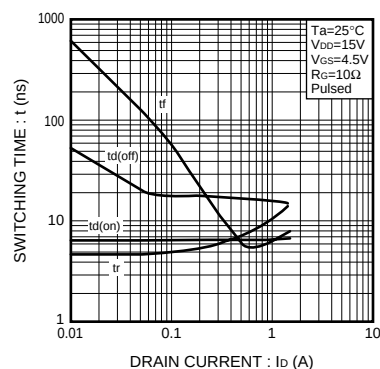


Fig.1 Switching Characteristics

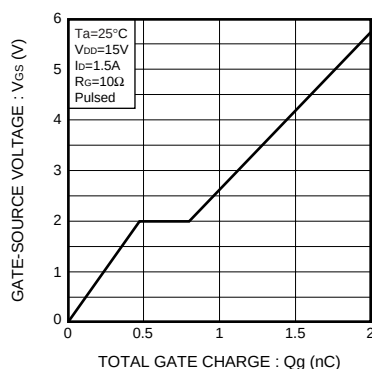


Fig.2 Dynamic Input Characteristics

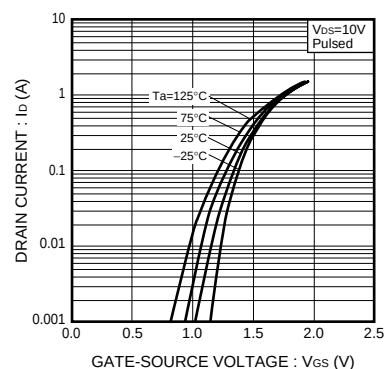


Fig.3 Typical Transfer Characteristics

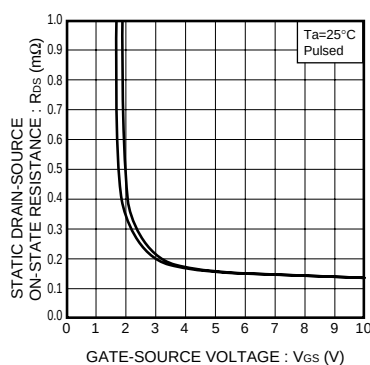


Fig.4 Static Drain-Source On-State Resistance vs. Gate source Voltage

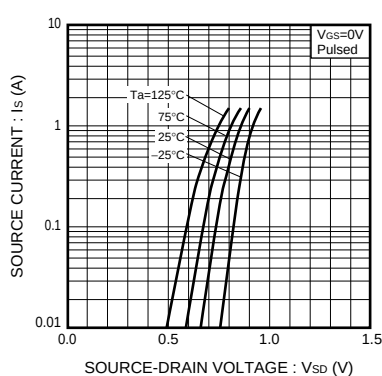


Fig.5 Source Current vs. Source-Drain Voltage

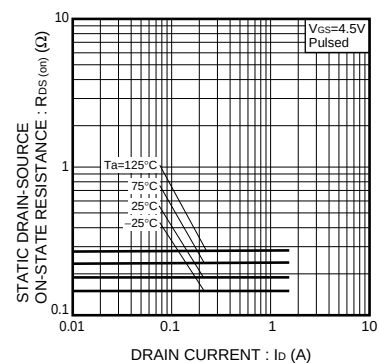


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (I)

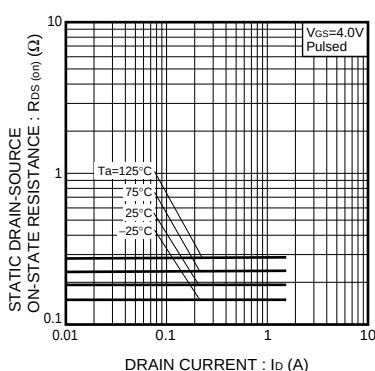


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (II)

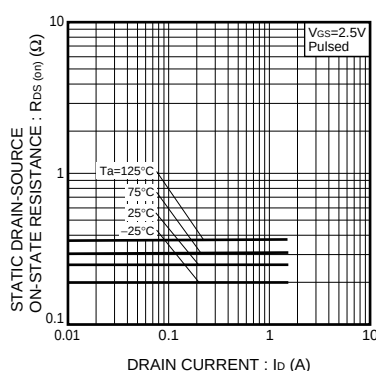


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (III)

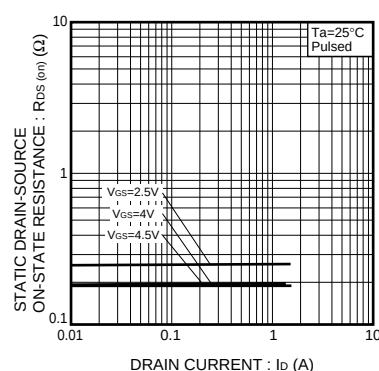


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (IV)

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