IS61C256AH
IS61M256

32K x 8 HIGH-SPEED CMOS STATIC RAM

MARCH 1998

FEATURES

- High-speed access time: 8, 10, 12, 15, 20, 25 ns
- Low active power: 400 mW (typical)
- Low standby power
  - — 250 µW (typical) CMOS standby
  - — 55 mW (typical) TTL standby
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V power supply
- Mix-mode outputs on IS61M256

DESCRIPTION

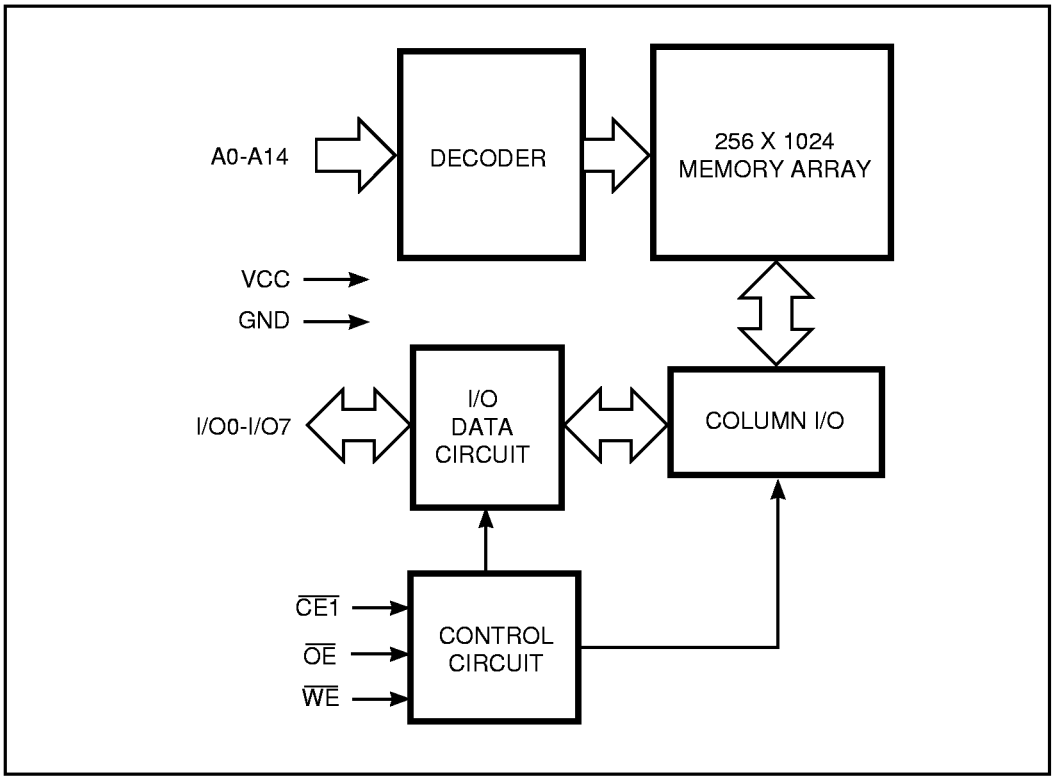
The *ISSI* IS61C256AH and IS61M256 are very high-speed, low power, 32,768 word by 8-bit static RAMs. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns maximum.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) with CMOS input levels.

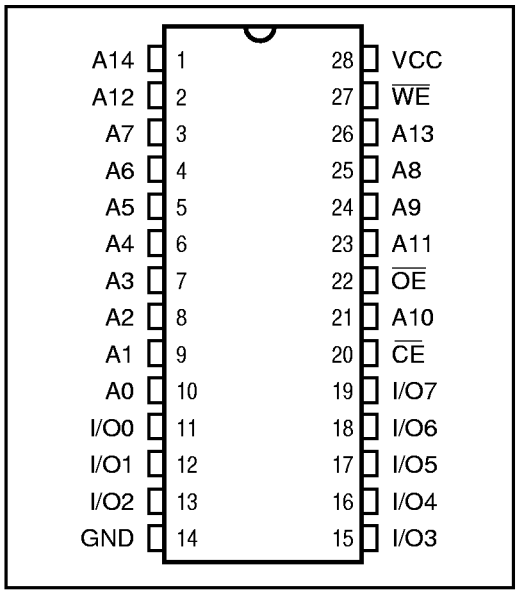
Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$) input and an active LOW Output Enable ($\overline{OE}$) input. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61C256AH and IS61M256 are pin compatible with other 32K x 8 SRAMs and are available in 28-pin PDIP, SOJ, and TSOP (type 1) packages.

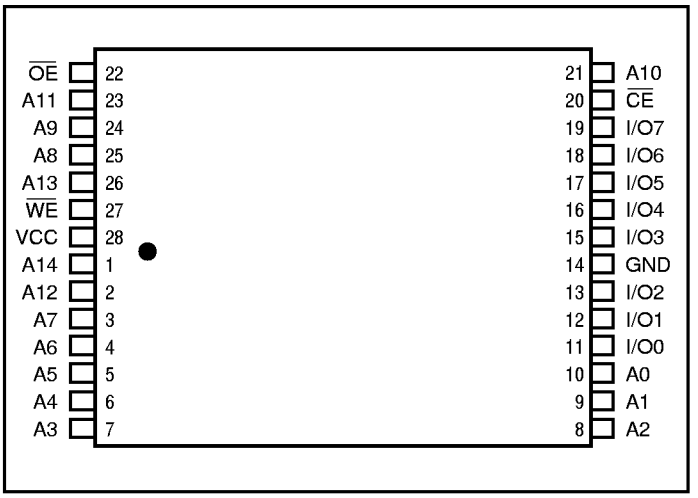
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin DIP and SOJ



PIN CONFIGURATION
28-Pin TSOP



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed	Vcc
Commercial	0°C to +70°C	-8[1], -10, -12	5V ± 5%
		-15, -20, -25	5V ± 10%
Industrial	–40°C to +85°C	-12	5V ± 5%
		-15, -20, -25	5V ± 10%

Note:
1. 8 ns is preliminary.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.5	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	Com.	–5	5	µA
			Ind.	–10	10	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}, Outputs Disabled	Com.	–5	5	µA
			Ind.	–10	10	

Notes:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8[2] Min.	-8[2] Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
I_{CC}	Vcc Dynamic Operating Supply Current	V_{CC} = Max., $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	200	—	120	—	135	—	125	—	120	—	120	mA
			Ind.	—	—	—	—	—	170	—	160	—	150	—	140	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f = 0	Com.	—	80	—	25	—	25	—	25	—	25	—	25	mA
			Ind.	—	—	—	—	—	30	—	30	—	30	—	30	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	—	5	—	5	—	2	—	2	—	2	—	2	mA
			Ind.	—	—	—	—	—	10	—	10	—	10	—	10	

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. 8 ns is preliminary.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8[4] Min.	-8[4] Max.	-10 Min.	-10 Max	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	—	20	—	25	ns
t_{OHA}	Output Hold Time	2	—	2	—	2	—	2	—	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	—	12	—	15	—	20	—	25	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	5	—	5	—	7	—	8	—	9	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	5	—	6	—	7	—	9	—	10	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	2	—	2	—	3	—	3	—	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	—	5	—	5	—	7	—	8	—	9	—	10	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	8	—	10	—	12	—	15	—	18	—	20	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.
4. 8 ns is preliminary.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

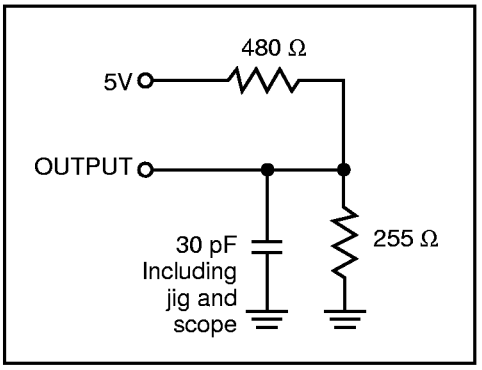


Figure 1

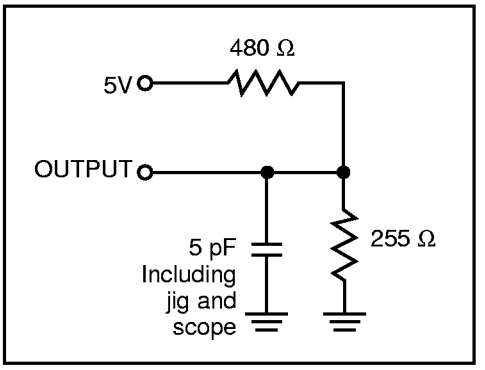
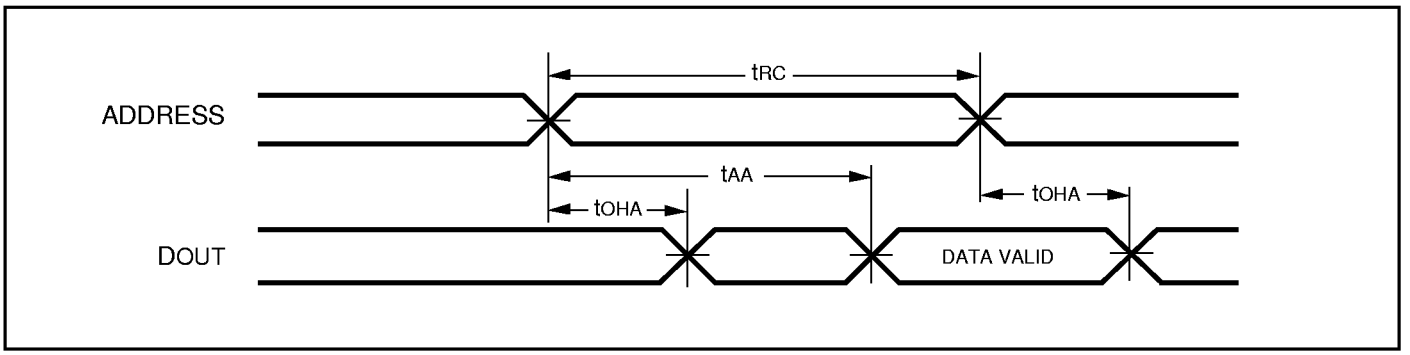


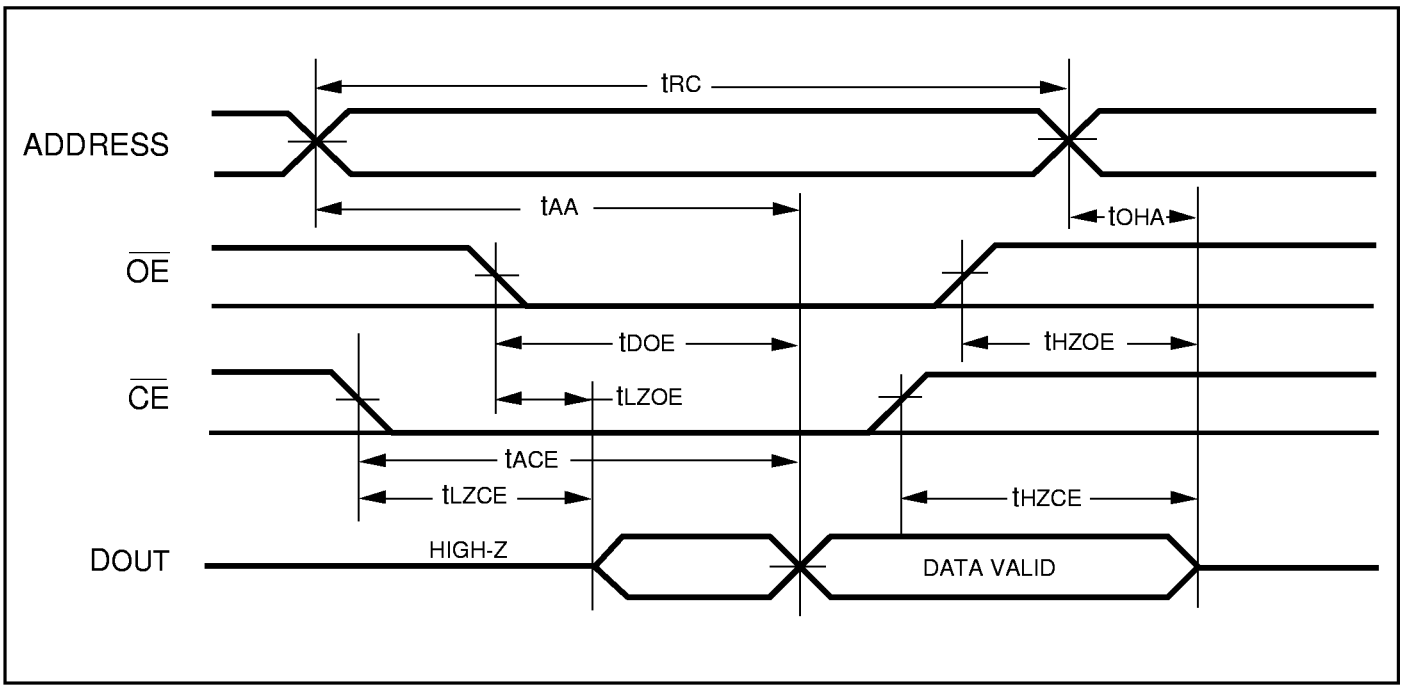
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

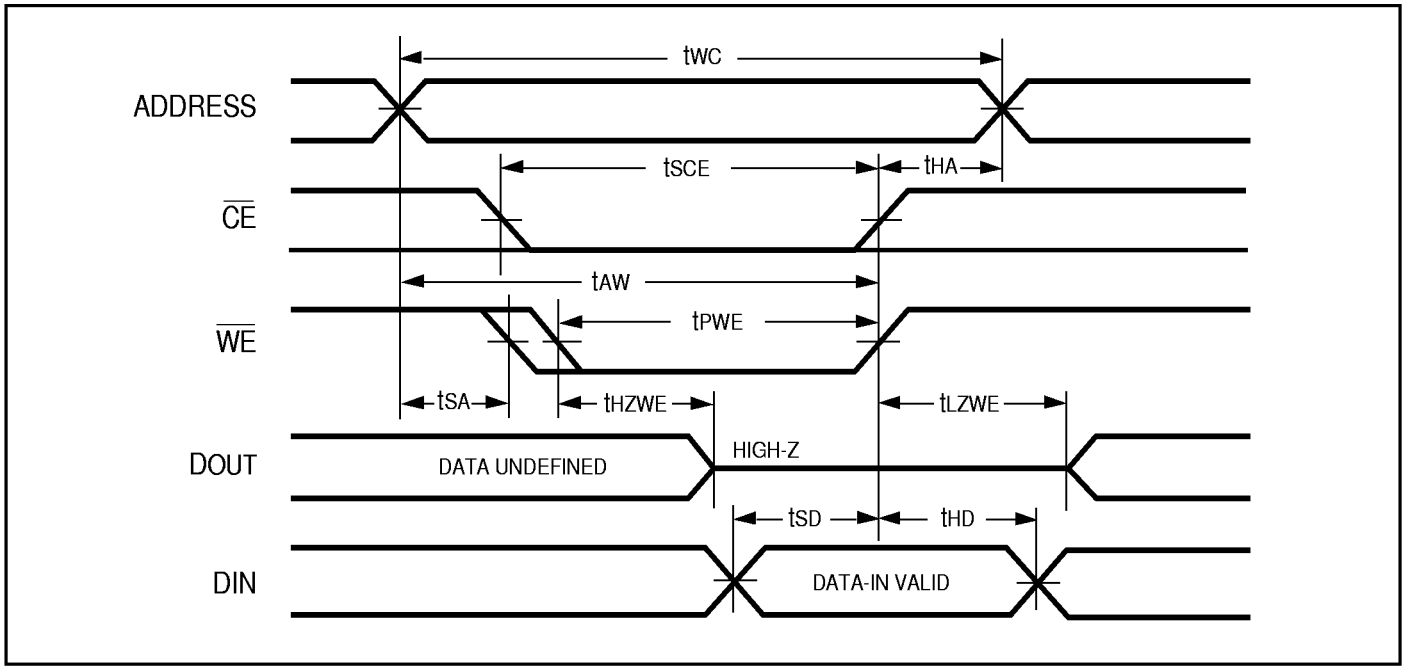
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8[5] Min.	-8[5] Max.	-10 Min.	-10 Max	-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	25	—	ns
t_{SCE}	$\overline{CE}$ to Write End	8	—	9	—	10	—	10	—	13	—	15	—	ns
t_{AW}	Address Setup Time to Write End	8	—	9	—	10	—	12	—	15	—	20	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	8	—	8	—	8	—	10	—	13	—	15	—	ns
t_{SD}	Data Setup to Write End	7	—	7	—	7	—	9	—	10	—	12	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	6	—	6	—	6	—	7	—	8	—	10	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	0	—	0	—	ns

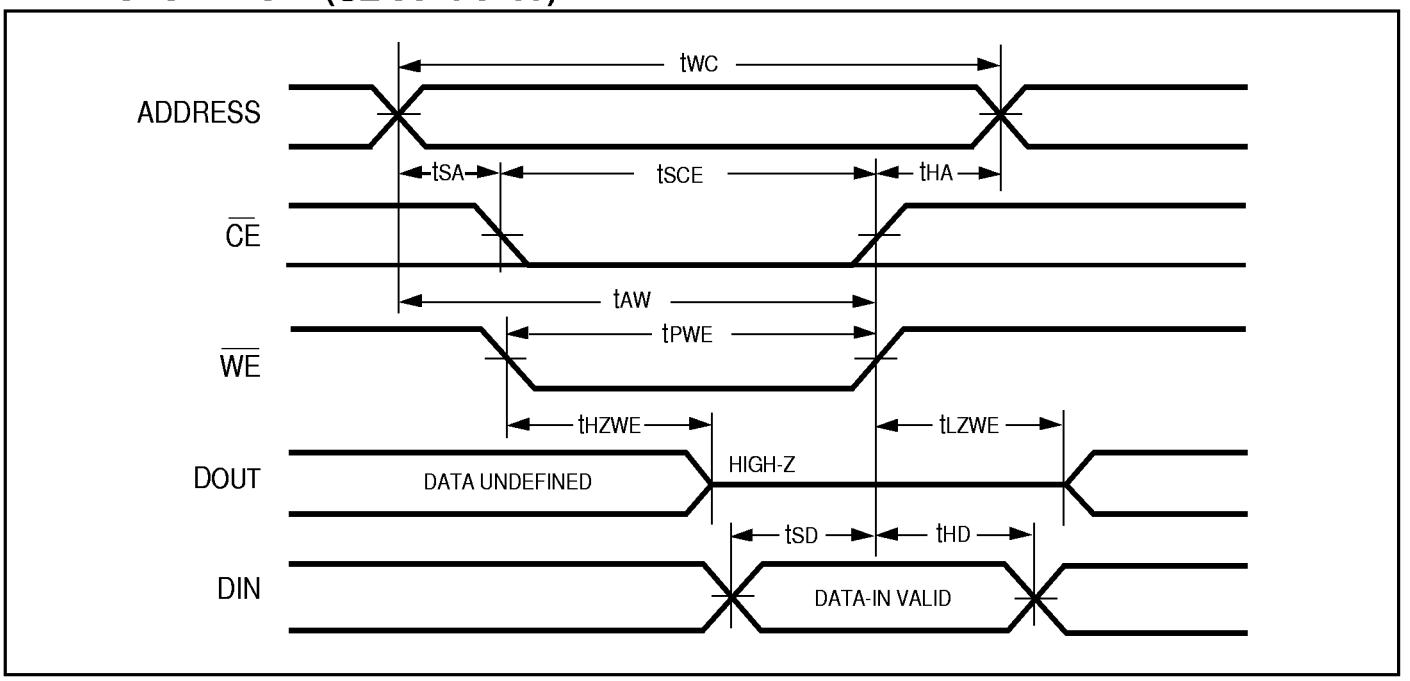
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ HIGH.
5. 8 ns is preliminary.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]



WRITE CYCLE NO. 2 ($\overline{CE}$ Controlled)[1,2]



Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

ORDERING INFORMATION: IS61C256AH
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part Number	Package
8	IS61C256AH-8N	300-mil Plastic DIP
8	IS61C256AH-8J	300-mil Plastic SOJ
8	IS61C256AH-8T	TSOP Type I
10	IS61C256AH-10N	300-mil Plastic DIP
10	IS61C256AH-10J	300-mil Plastic SOJ
10	IS61C256AH-10T	TSOP (Type 1)
12	IS61C256AH-12N	300-mil Plastic DIP
12	IS61C256AH-12J	300-mil Plastic SOJ
12	IS61C256AH-12T	TSOP (Type 1)
15	IS61C256AH-15N	300-mil Plastic DIP
15	IS61C256AH-15J	300-mil Plastic SOJ
15	IS61C256AH-15T	TSOP (Type 1)
20	IS61C256AH-20N	300-mil Plastic DIP
20	IS61C256AH-20J	300-mil Plastic SOJ
20	IS61C256AH-20T	TSOP (Type 1)
25	IS61C256AH-25N	300-mil Plastic DIP
25	IS61C256AH-25J	300-mil Plastic SOJ
25	IS61C256AH-25T	TSOP (Type 1)

ORDERING INFORMATION: IS61C256AH
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part Number	Package
12	IS61C256AH-12NI	300-mil Plastic DIP
12	IS61C256AH-12JI	300-mil Plastic SOJ
12	IS61C256AH-12TI	TSOP (Type 1)
15	IS61C256AH-15NI	300-mil Plastic DIP
15	IS61C256AH-15JI	300-mil Plastic SOJ
15	IS61C256AH-15TI	TSOP (Type 1)
20	IS61C256AH-20NI	300-mil Plastic DIP
20	IS61C256AH-20JI	300-mil Plastic SOJ
20	IS61C256AH-20TI	TSOP (Type 1)
25	IS61C256AH-25NI	300-mil Plastic DIP
25	IS61C256AH-25JI	300-mil Plastic SOJ
25	IS61C256AH-25TI	TSOP (Type 1)

ORDERING INFORMATION: IS61M256
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part Number	Package
10	IS61M256-10N	300-mil Plastic DIP
10	IS61M256-10J	300-mil Plastic SOJ
12	IS61M256-12N	300-mil Plastic DIP
12	IS61M256-12J	300-mil Plastic SOJ
15	IS61M256-15N	300-mil Plastic DIP
15	IS61M256-15J	300-mil Plastic SOJ
20	IS61M256-20N	300-mil Plastic DIP
20	IS61M256-20J	300-mil Plastic SOJ
25	IS61M256-25N	300-mil Plastic DIP
25	IS61M256-25J	300-mil Plastic SOJ

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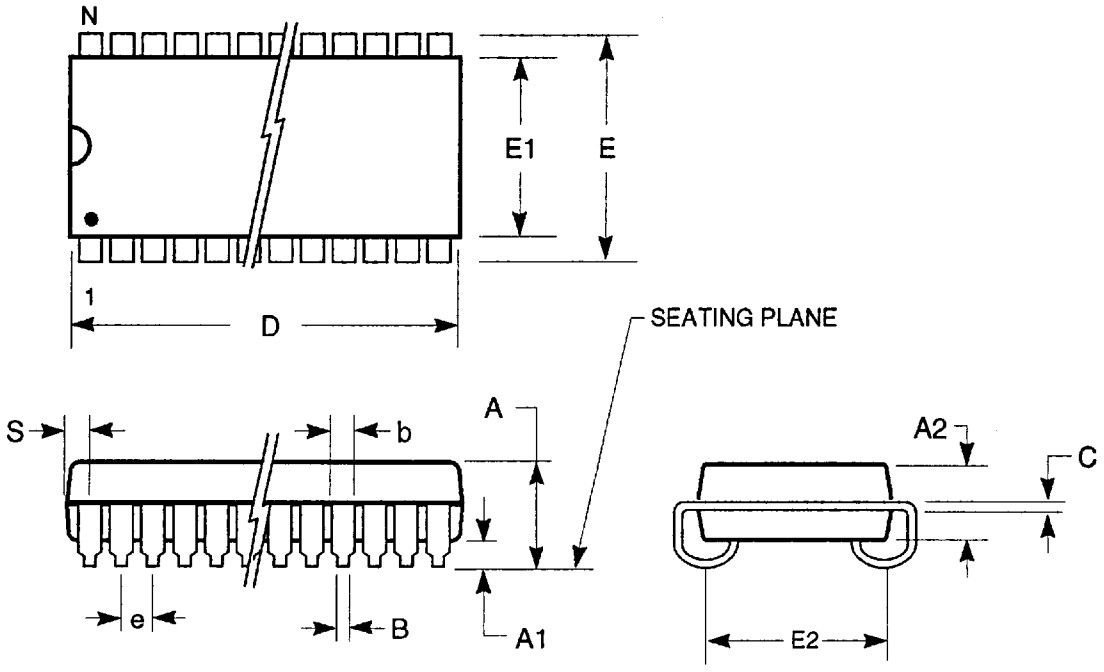
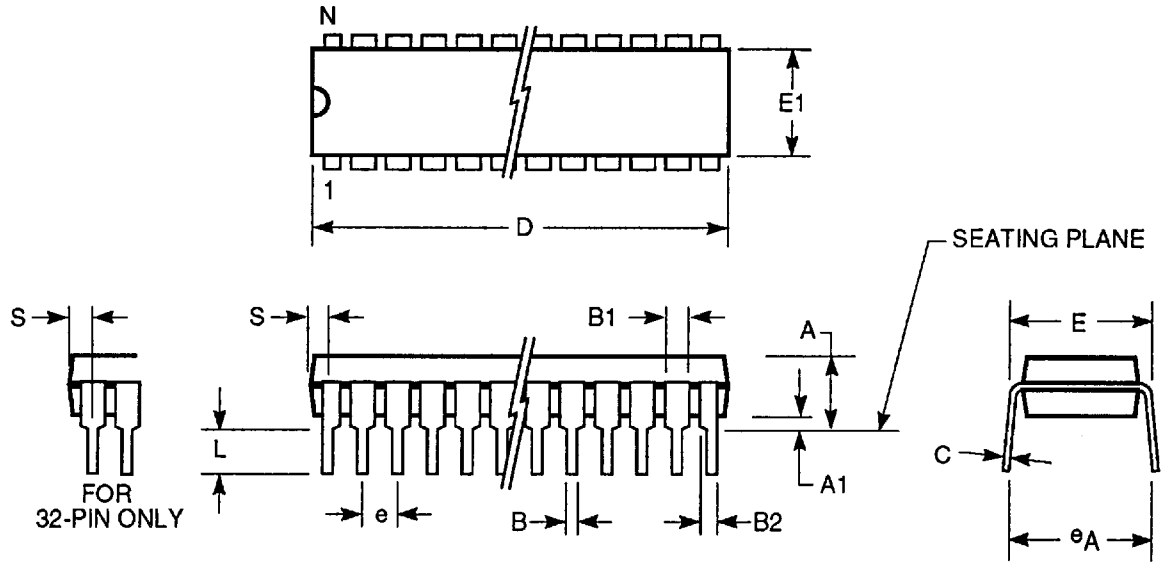
300-mil Plastic SOJ
Package Code: J



300-mil Plastic SOJ (J-bend) (J)				
	Inches			
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads	28		32	
A	—	0.140	—	0.140
A1	0.020	—	0.020	—
A2	0.095	0.105	0.095	0.105
B	0.016	0.022	0.016	0.022
b	0.026	0.032	0.026	0.032
C	0.008	0.014	0.008	0.014
D	0.710	0.730	0.815	0.835
E	0.327	0.347	0.325	0.345
E1	0.295	0.305	0.295	0.305
E2	0.245	0.285	0.247	0.287
e	0.050 BSC		0.050 BSC	
S	—	0.045	0.023	0.035

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

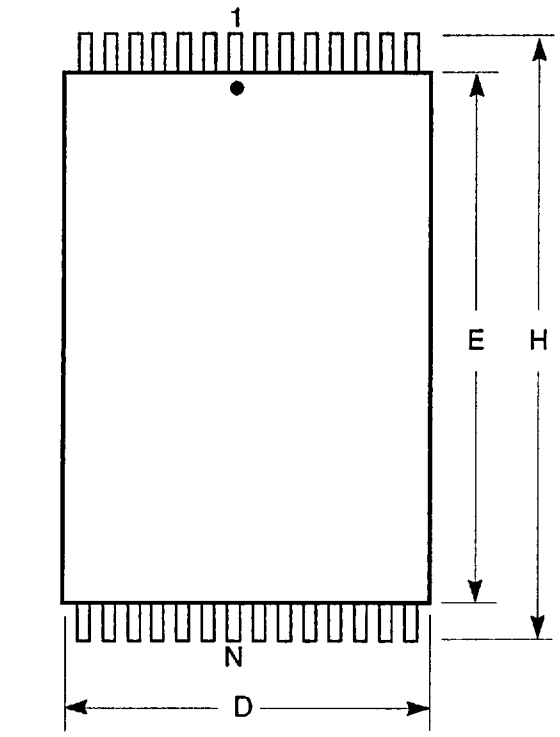
300-mil Plastic DIP
Package Code: N, P

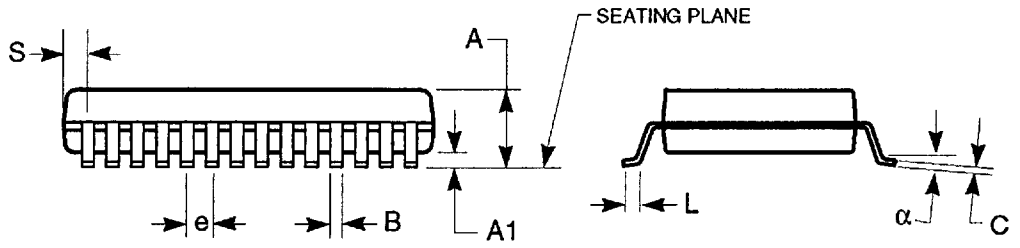


300-mil Plastic DIP (N, P)										
	Inches									
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.										
N	8		16		20		28		32	
A	0.145	0.180	0.145	0.180	0.145	0.180	0.145	0.180	0.140	0.180
A1	0.015	—	0.010	—	0.015	—	0.010	—	0.015	—
B	0.014	0.022	0.018 BSC		0.014	0.22	0.016	0.022	0.015	0.021
B1	0.045	0.060	0.060 BSC		0.045	0.070	0.050	0.070	0.040	0.070
B2	0.032	0.046	—	—	—	—	0.032	0.046	—	—
C	0.008	0.013	0.005	0.015	0.008	0.014	0.008	0.015	0.005	0.015
D	0.359	0.375	0.745	0.755	1.020	1.040	1.380	1.400	1.595	1.605
E	0.300	0.325	0.293	0.320	0.295	0.325	0.295	0.315	0.305	0.325
E1	0.244	0.260	0.245	0.255	0.240	0.280	0.275	0.295	0.285	0.292
e_A	0.320	0.380	0.320	0.380	—	0.430	0.310	0.400	0.330	0.370
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
L	0.125	—	0.120	0.140	0.120	0.150	0.120	0.150	0.120	0.150
S	0.025	0.030	0.015	0.035	0.04	0.06	0.020	0.042	0.065	0.085

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

Plastic TSOP - 28-pins
Package Code: T (Type I)





Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		28		
A	1.00	1.20	0.037	0.047
A1	0.05	0.20	0.002	0.008
B	0.16	0.27	0.006	0.011
C	0.10	0.20	0.004	0.008
D	7.90	8.10	0.308	0.316
E	11.70	11.90	0.456	0.465
H	13.20	13.60	0.515	0.531
e	0.55 BSC		0.022 BSC	
L	0.30	0.70	0.011	0.027
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.