QLogic Corporation

ISP1240 Intelligent, Dual SCSI Processor

Data Sheet

Features

- 64-bit PCI host bus interface, complaint with *PCI Local Bus Specification* revision 2.1
- Compliance with ANSI Fast-20 standard X3T10/1071D
- Compliance with ANSI X3T10/855D SCSI-3 parallel interface (SPI) standard
- Supports fast, wide, and Ultra (Fast-20) SCSI data transfer rates
- Two concurrently operating wide, Ultra SCSI channels
- Supports single-ended and differential SCSI
- SCSI initiator and target modes of operation
- Onboard RISC processor to execute operations at the I/O control-block level from the host memory
- Supports PCI dual-address cycle (64-bit addressing)
- SCSI operations executed from start to finish without host intervention
- Simultaneous, multiple logical threads
- Supports JTAG boundary scan

Product Description

The ISP1240 adds dual channel, Ultra SCSI support to the expanding functionality of the ISP product family. The ISP1240 is a single-chip, highly integrated, bus master, dual-channel SCSI I/O processor for SCSI initiator and target applications. This device interfaces the 64-bit PCI bus to two Ultra SCSI buses and contains an onboard RISC processor. The ISP1240 is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers simultaneously on two SCSI channels from start to finish without host intervention. The ISP1240 is host-software compatible with the QLogic single channel ISP1040, requiring only a minor input/output control block (IOCB) change to select the additional channel. The ISP1240 block diagram is illustrated in figure 1.

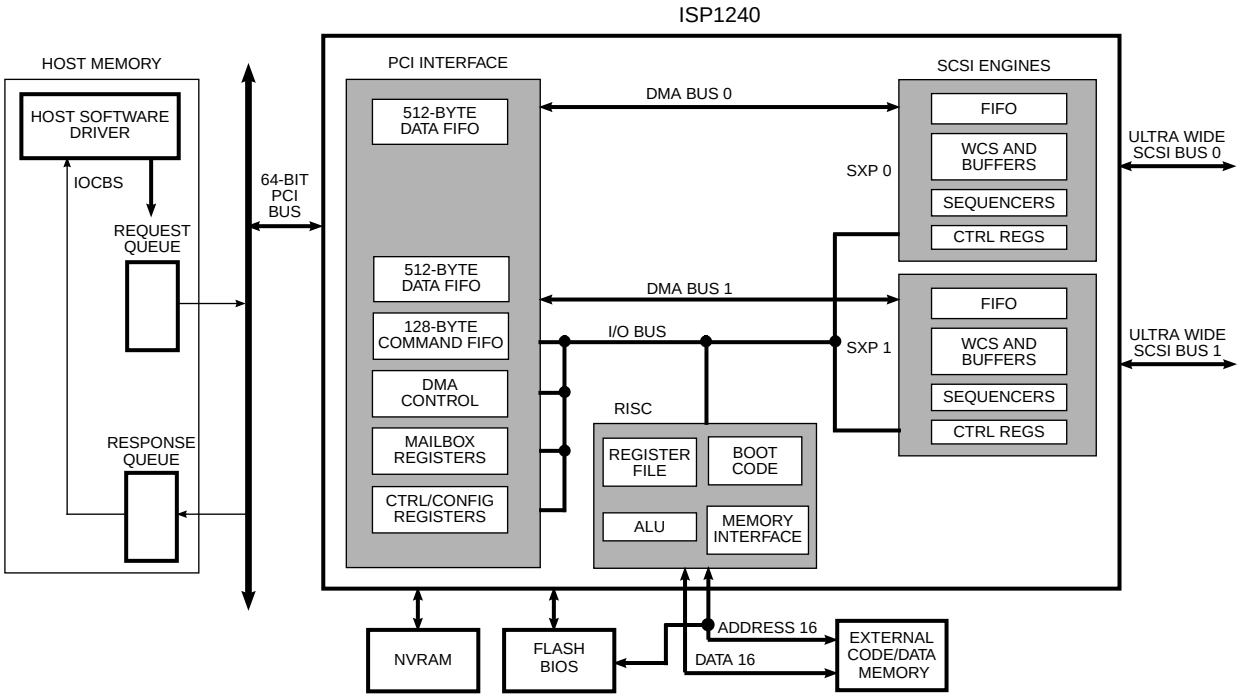

Figure 1. ISP1240 Block Diagram

ISP Initiator and Target Firmware

The ISP1240 firmware implements a cooperative, multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI bus protocol. The firmware provides two interfaces to the host system: the command interface and the SCSI transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery. The multithreaded SCSI transport interface maximizes use of the SCSI and host buses. The ISP1240 can switch between initiator and target modes.

Software Drivers

BIOS firmware is available for the ISP1240. Software drivers are available for the following operating systems:

- AIX
- I_2O
- DOS/Windows
- Novell NetWare
- OS/2
- SCO UNIX
- UnixWare
- Windows 95
- Windows NT

Subsystem Organization

To maximize I/O throughput and improve host and SCSI bus utilization, the ISP1240 incorporates a high-speed, proprietary RISC processor; two intelligent SCSI bus controllers (SCSI executive processor [SXP]); and a host bus, three-channel, first-party DMA controller. The SCSI bus controllers and the host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance. The ISP1240 RISC interface requires external program data memory.

The complete I/O subsystem solution using the ISP1240 and associated supporting memory devices is shown in figure 2.

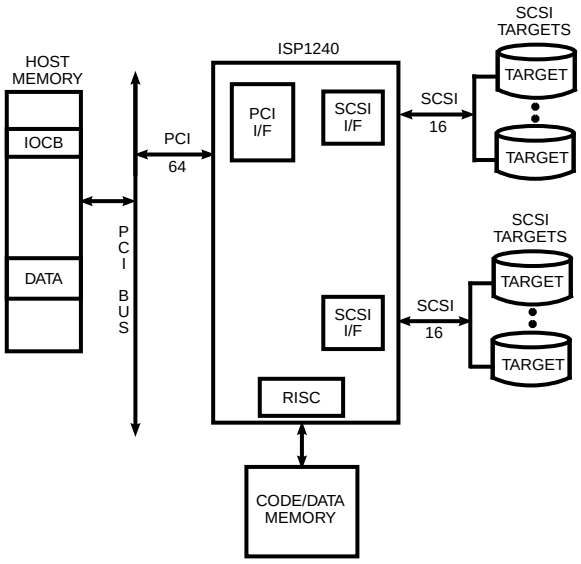

Figure 2. I/O Subsystem Design Using the ISP1240

Interfaces

The ISP1240 interfaces consist of the 64-bit PCI bus interface, two SCSI interfaces, and the RISC interface. Pins that support these interfaces and other chip operations are shown in figure 3.

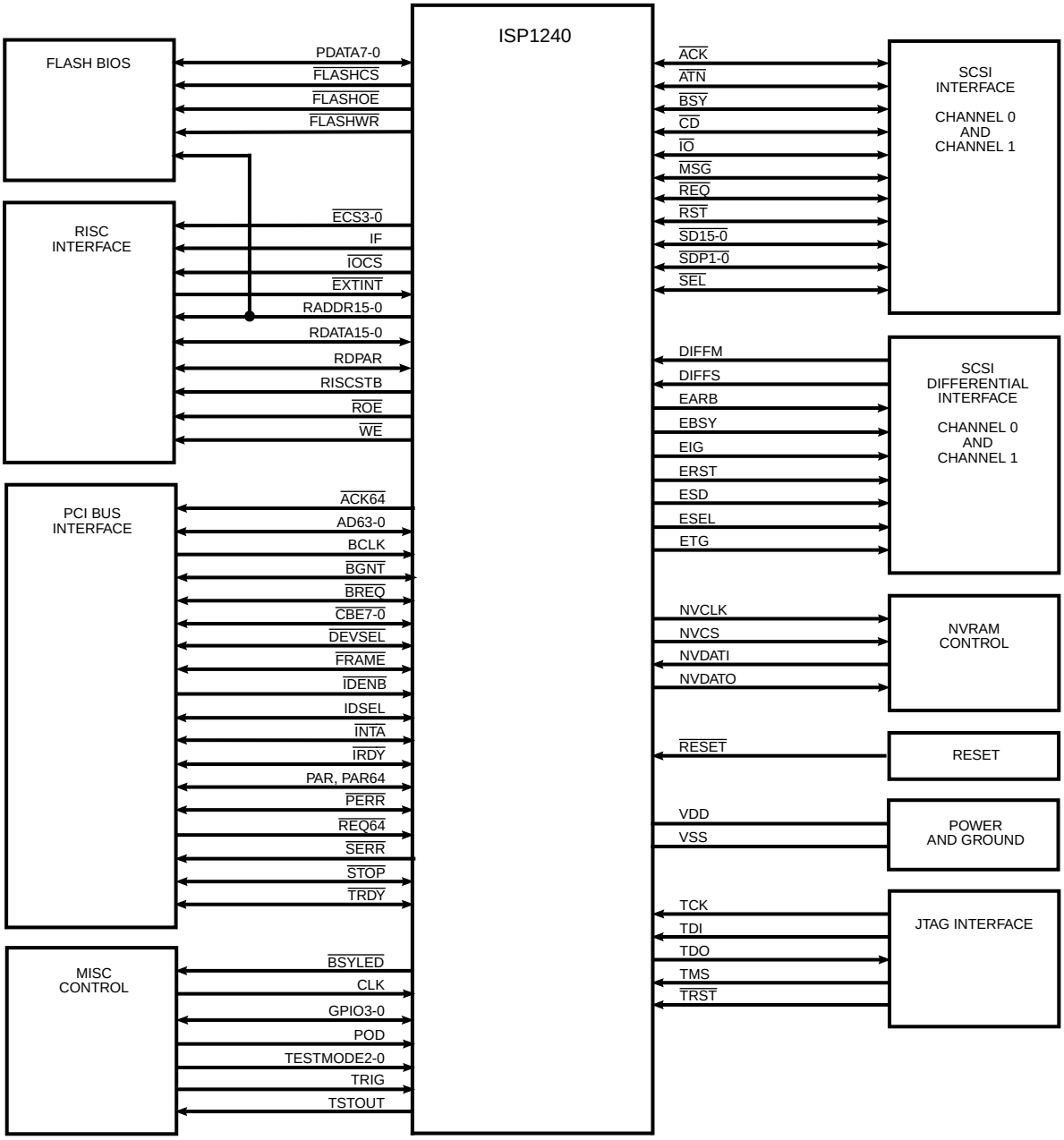

Figure 3. ISP1240 Functional Signal Grouping

PCI Interface

The ISP1240 PCI interface supports the following:

- 64-bit, intelligent bus master, burst DMA host interface for fetching I/O control blocks and data transfers
- 64-bit host memory addressing (dual address cycle)
- Backward compatible to 32-bit PCI
- Three-channel DMA controller
- 512-byte data DMA FIFO per channel and 128-byte command DMA FIFO with threshold control
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit DMA transfer counter for I/O transfer lengths of up to four gigabytes

- Support for subsystem ID
- Support for flash BIOS PROM
- Support for PCI cache commands
- 3.3V and 5.0V tolerant PCI I/O buffers

The ISP1240 is designed to interface directly to the PCI bus and operate as a 64-bit, DMA bus master. This operation is accomplished through a PCI bus interface unit (PBIU) that contains an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard DMA FIFO. It also allows the host to access the ISP1240 internal registers and communicate with the onboard RISC processor through the PCI target mode operation.

The ISP1240 onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and DMA FIFO. The three DMA channels consist of the command DMA channel and two data DMA channels. The command DMA channel is used mainly by the RISC processor for small transfers such as fetching commands from and writing status information to the host memory over the PCI bus. The data DMA channels transfer data between two SCSI buses and the PCI bus.

The PBIU internally arbitrates between the data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

SCSI Executive Processors

Each ISP1240 SXP supports the following:

- 8- or 16-bit data transfers
- Ultra SCSI (Fast-20) synchronous data transfer rates up to 40 Mbytes/sec
- Asynchronous SCSI data transfer rates up to 12 Mbytes/sec
- Programmable SCSI processor
  - Specialized instruction set with 16-bit microword
  - 384-bit by 16-bit internal RAM control store
- 32-bit, configurable SCSI transfer counter
- Command, status, message in, and message out buffers
- Device information storage area
- On-chip, single-ended SCSI transceivers (48-mA drivers)
- Programmable active negation

The SXP provides an autonomous, intelligent SCSI interface capable of handling complete SCSI operations. The SXP interrupts the RISC processor only to handle higher level functions such as threaded operations or error handling.

RISC Processor

The ISP1240 RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

The onboard RISC processor enables the ISP1240 to handle complete I/O transactions with no intervention from the host. The ISP1240 RISC processor controls the chip interfaces; executes simultaneous, multiple input/output control blocks (IOCB) for both SCSI channels; and maintains the required thread information for each transfer.

Packaging

The ISP1240 is available in a 352-pin thermally enhanced ball grid array (TE BGA) package.