QLogic Corporation

ISP2100A Intelligent Fibre Channel Processors

Data Sheet

Features

- Available in two versions:
  - 66-MHz, 64-bit PCI host bus interface
  - 33-MHz, 64-bit PCI host bus interface
- Compliance with *PCI Local Bus Specification* revision 2.1
- Compliance with ANSI SCSI standard X3.131-1994
- Supports all Fibre Channel topologies and classes of service
- Compliance with *Fibre Channel Arbitrated Loop (FC-AL) Direct Disk Attach Profile* and *Fibre Channel Public Loop (FC-PL) Fabric Loop Attach Profile*, class 2 and class 3 service
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.0 (PC97)
- Supports 100 Mbytes/sec sustained Fibre Channel data transfer rate
- Initiator or target mode
- Onboard RISC processor to execute operations at the I/O control-block (IOCB) level from the host memory
- Onboard gigabit serial transceivers
- Supports external transceivers with a 10-bit interface
- Supports PCI dual-address cycle (64-bit addressing) and cache commands
- No host intervention required to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads
- Full duplex frame buffer architecture
- Supports JTAG boundary scan

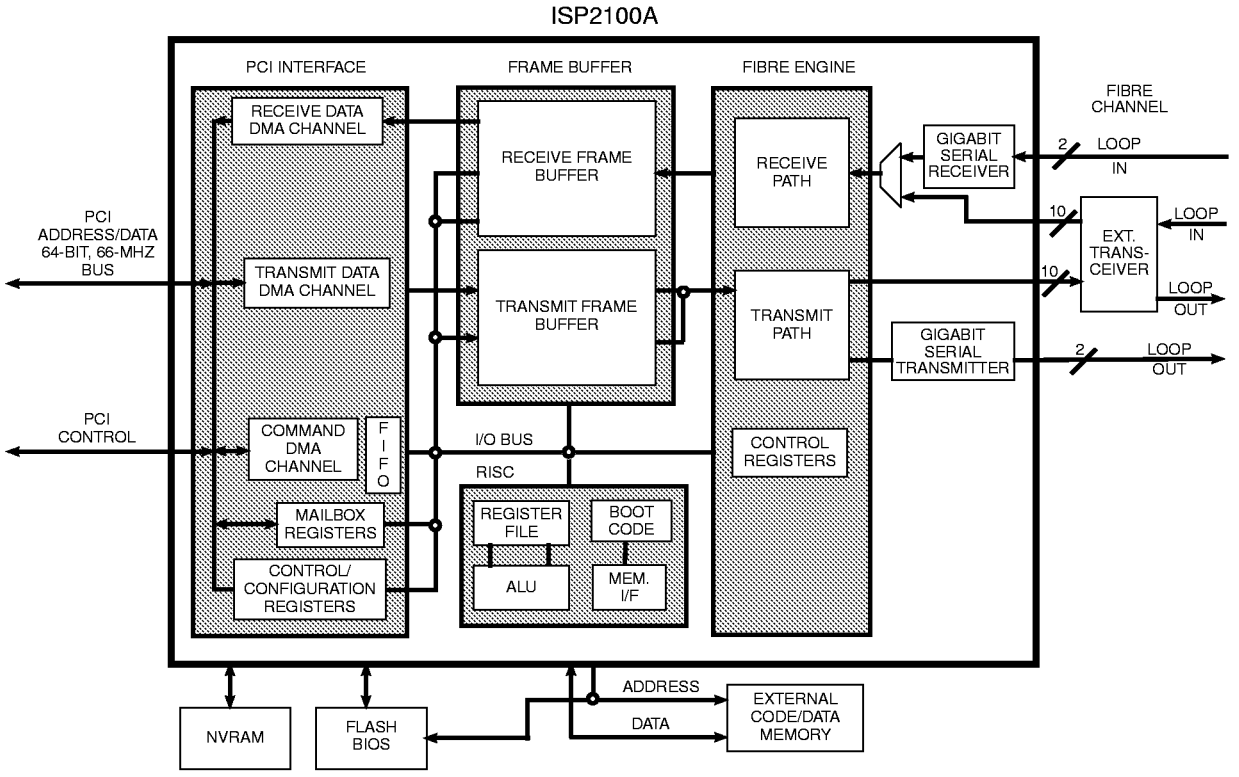

Figure 1. ISP2100A Block Diagram

Product Description

The ISP2100A is a single-chip, highly integrated, bus master, FC-AL processor that targets SCSI applications. This chip connects the PCI bus to a Fibre Channel loop and contains an onboard RISC processor. The ISP2100A is pin compatible with the ISP2100. Like the ISP2100, the ISP2100A is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention.

The ISP2100A provides power management support in accordance with the *PCI Bus Power Management Interface Specification*. The ISP2100A block diagram is illustrated in figure 1.

ISP Initiator and Target Firmware

The ISP2100A firmware implements a multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI Fibre Channel protocol (FCP). The firmware provides two interfaces to the host system: the command interface and the Fibre Channel transport interface. The single-threaded command interface facilitates debugging, configuration, and recovering errors. The multithreaded transport interface maximizes use of the Fibre Channel and host buses.

The ISP2100A can switch between initiator and target modes.

Software Drivers

The ISP2100A supports a host software interface similar to the ISP1020/1040 family. Existing 1020/1040 software drivers are easily modified to support the ISP2100A.

BIOS firmware is available for the ISP2100A. Software drivers are available for the following operating systems:

- AIX
- I_2O
- DOS/Windows
- Novell NetWare
- OS/2
- SCO UNIX
- UnixWare
- Windows 95; x86 and Alpha systems
- Windows NT; x86 and Alpha systems
- Solaris; x86 and SPARC systems

Subsystem Organization

To maximize I/O throughput and improve host and loop utilization, the ISP2100A incorporates a high-speed, proprietary RISC processor; a Fibre Channel protocol manager (FPM); integrated frame buffer memory; and a host bus, three-channel, bus master DMA controller. The FPM and host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance.

The complete I/O subsystem solution using the ISP2100A and associated supporting memory devices is shown in figure 2.

Interfaces

The ISP2100A interfaces consist of the FC-AL interface, PCI bus interface, RISC interface, flash BIOS interface, and NVRAM control. Pins that support these interfaces and other chip operations are shown in figure 3.

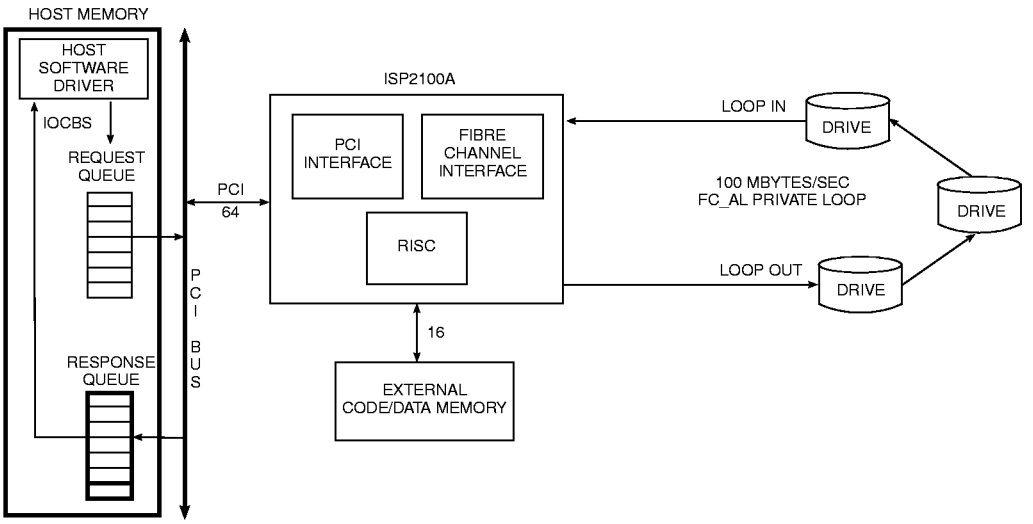

Figure 2. I/O Subsystem Design Using the ISP2100A

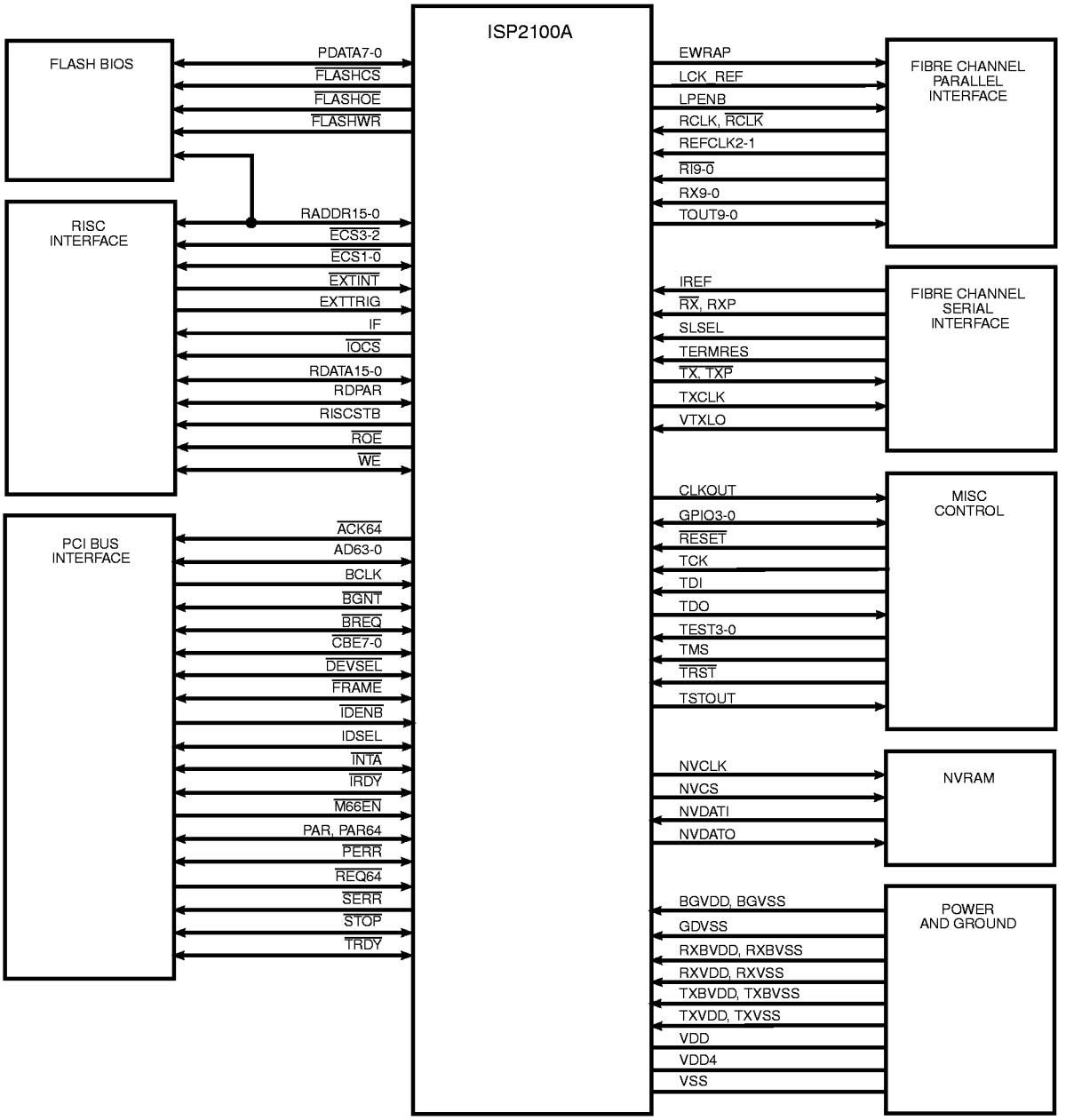

Figure 3. ISP2100A Functional Signal Grouping

Fibre Channel Interface

The ISP2100A provides on-board gigabit transceivers for direct connection to the Fibre Channel loop on copper media. A standard 10-bit interface is also provided to connect to external transceivers, if desired.

Fibre Channel Protocol Manager

The ISP2100A FPM supports the following:

- Support for one Fibre Channel loop
- 100 Mbytes/sec sustained data transfer rate
- 10-bit interface to external transceivers
- Gigabit serial interface
- Integrated frame buffer that supports up to 2-KB frame payload

The FPM includes an 8B/10B encoder and decoder, an elasticity buffer for clock skew management, and an FC-AL state machine. The FPM transmits and receives at the full Fibre Channel rate of 106.25 Mbytes/sec. The on-chip frame buffer includes separate areas for received data and transmit data, as well as areas for managing special frames such as command and response. The FPM receive

path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer. The transmit path transmits frames from the frame buffer to the Fibre Channel. The FPM automatically handles frame delimiters and frame control.

PCI Interface

The ISP2100A PCI interface supports the following:

- 33-MHz or 66-MHz, 64-bit, intelligent bus master interface for fetching IOCBs and data transfers
- 64-bit host memory addressing (dual address cycle)
- Backward compatible to 32-bit PCI
- Three-channel DMA controller
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit DMA transfer counter for I/O transfer length of up to four gigabytes
- Support for PCI cache commands
- Support for flash BIOS PROM
- Support for subsystem ID
- 3.3V and 5.0V tolerant PCI I/O buffers

The ISP2100A is designed to interface directly to the PCI bus and operate as a 64-bit, DMA bus master, which is backward compatible to 32-bit operation. This function is accomplished through a PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard frame buffer. It also allows the host to access the ISP2100A internal registers and communicate with the onboard RISC processor.

The ISP2100A supports the minimum power management capabilities specified in revision 1.0 of the *PCI Bus Power Management Interface Specification*, which defines power states D0-D3, where D0 provides maximum power consumption and D3 provides minimal power consumption. The D1 and D2 power states provide intermediate power consumption. The D3 power state is entered by either software (D3 *hot*) or by physically removing power (D3 *cold*). Hot and cold refer to the presence or absence of VCC, respectively.

The ISP2100A supports power states D0, D3 hot, and D3 cold.

The ISP2100A onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and frame buffer. The command DMA channel is used mainly by the RISC processor for small transfers, such as fetching commands from and writing status information to the host memory over the PCI bus. The two data DMA channels, one for transmit and one for receive, transfer data between the FC-AL and the PCI bus, allowing for fast context switching.

The PBIU internally arbitrates between the two data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

RISC Processor

The ISP2100A RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

One of the major features of the ISP2100A is its ability to handle complete I/O transactions from start to finish with no intervention from the host. This high level of integration is accomplished with an onboard RISC processor. The ISP2100A RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs; and maintains the required thread information for each transfer.

Packaging

The ISP2100A is available in a 256-pin ball grid array (BGA) package.