QLogic Corporation

ISP2300 Intelligent Fibre Channel Processor 2-Gigabit Fibre Channel to 66-MHz PCI

Features

- 66-MHz, 64-bit PCI host bus interface
- Backward compatible to standard 33-MHz PCI
- Compliance with *PCI Local Bus Specification* revision 2.2
- Supports Fibre Channel-arbitrated loop (FC-AL), FC-AL-2, point-to-point, and switched fabric topologies
- Supports full-duplex communications in all Fibre Channel topologies
- Compliance with ANSI SCSI standards for class 1, class 2, class 3, and intermix Fibre Channel service:
  - *Fibre Channel-Arbitrated Loop (FC-AL-2*) working draft, rev 6.4, August 28, 1998
  - *Fibre Channel-Fabric Loop Attachment (FC-FLA)* working draft, rev 2.7, August 12, 1997
  - *Fibre Channel-Private Loop SCSI Direct Attach (FC-PLDA)* working draft, rev 2.1, September 22, 1997
  - *Fibre Channel-Tape (FC-TAPE)* profile, T11/98-124vD, rev 1.13, February 3, 1999
- Supports Fibre Channel protocol-SCSI (FCP-SCSI), Fibre Channel Internet Protocol (IP), and Fibre Channel-virtual interface (FC-VI) protocol
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.1 (PC99)
- Supports up to 400 Mbytes/sec sustained Fibre Channel data transfer rate
- Supports SCSI initiator, initiator/target, and target modes
- Onboard, enhanced RISC processor
- Onboard 2-gigabit serial transceivers
- Automatically negotiates the Fibre Channel bit rate (1 or 2 gigabits)
- Supports PCI dual-address cycle and cache commands
- No host intervention required to execute complete SCSI, IP, or VI operations
- Supports multi-ID aliasing in target mode
- Supports external frame buffering for performance scalability over long distances (up to 100 km)
- Supports JTAG boundary scan and full scan

Product Description

The ISP2300 is a single-chip, highly integrated, bus master, Fibre Channel processor that targets storage, clustering, and networking applications. This chip connects a conventional PCI bus to a 2-gigabit Fibre Channel loop or to a point-to-point Fibre Channel port.

The ISP2300 is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention.

The ISP2300 balances the advanced bus speeds and efficiency of PCI with exceptional 2-gigabit Fibre Channel performance. Fibre Channel support for SCSI, IP, and VI allows the ISP2300 to target a wide spectrum of storage and system area networks (SANs). The ISP2300 block diagram is illustrated in figure 1.

ISP Initiator/Target SCSI, IP, and VI Firmware

The ISP2300 firmware implements a multitasking host adapter that provides the host system with IP communications, complete SCSI command and data transport capabilities, and VI communications, thus freeing the host system from simultaneous execution of SCSI, IP, and VI traffic. The firmware provides two interfaces to the host system: the command interface and the Fibre Channel transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery. The multithreaded transport interface maximizes use of the Fibre Channel and host buses.

The ISP2300 can operate simultaneously in SCSI initiator and target modes, and supports SCSI, IP, and VI protocols concurrently.

Software Drivers

The ISP2300 supports a host software interface similar to the QLogic parallel SCSI and 1-gigabit Fibre Channel processor families. Existing ISP2100A/2200A software drivers for all major operating systems are easily modified to support the ISP2300. The ISP2300 also supports FCP-SCSI, IP, and VI software drivers for most major operating systems.

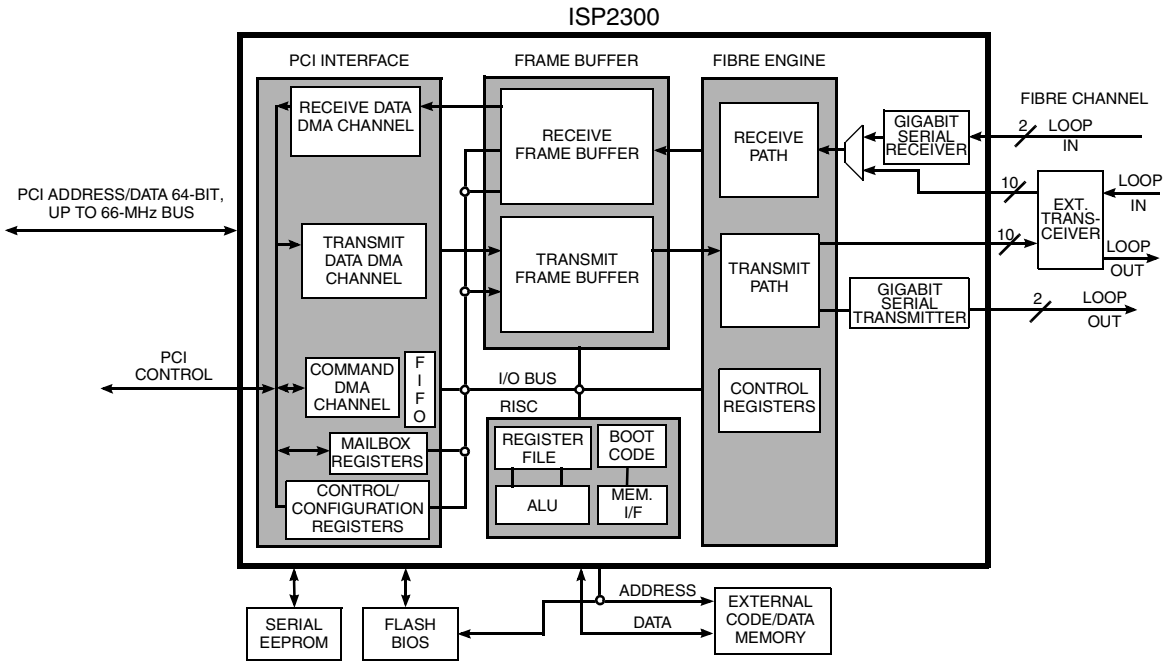

Figure 1. ISP2300 Block Diagram

Subsystem Organization

To maximize I/O throughput and improve host and Fibre Channel utilization, the ISP2300 incorporates a high-speed, proprietary RISC processor; a Fibre Channel protocol manager (FPM); integrated frame buffer memory; and a host bus, five-channel, bus master DMA controller. The FPM and host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance.

The complete I/O subsystem solution using the ISP2300 and directly connected hard drives is shown in figure 2.

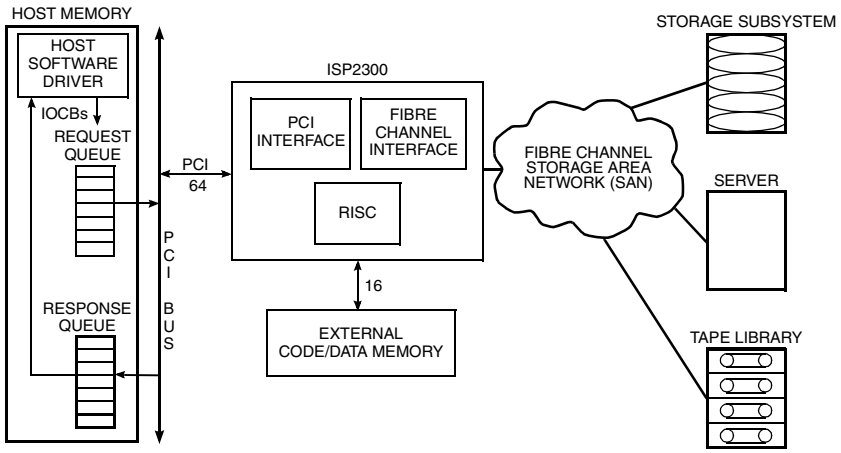

Figure 2. I/O Subsystem Design Using the ISP2300

Interfaces

The ISP2300 interfaces consist of the Fibre Channel interface, PCI bus interface, RISC interface, flash BIOS interface, and NVRAM interface. Pins that support these interfaces and other chip operations are shown in figure 3.

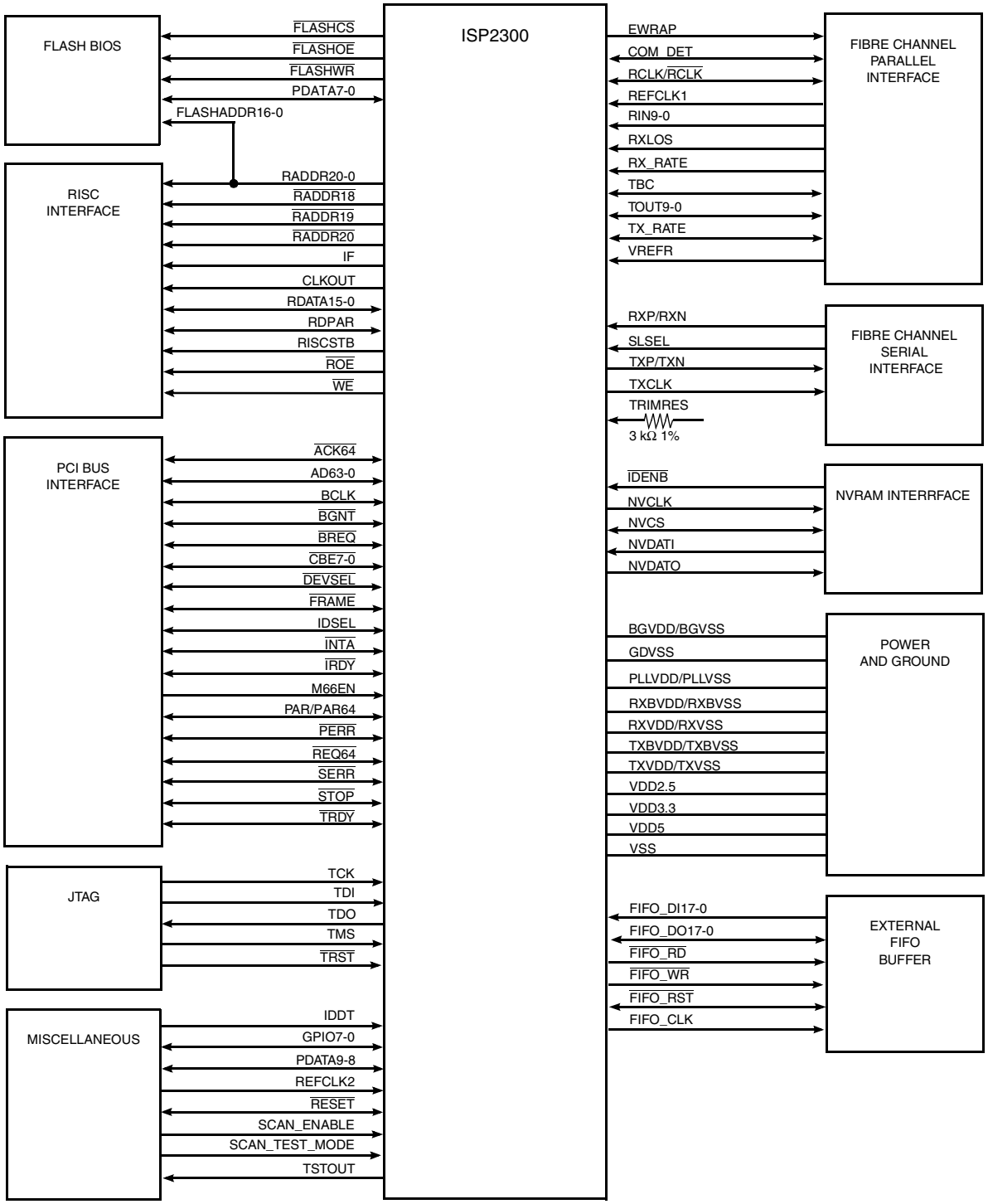

Figure 3. ISP2300 Functional Signal Grouping

Fibre Channel Interface

The ISP2300 provides onboard gigabit transceivers for direct connection to the Fibre Channel ports on copper media. A standard 10-bit interface is also provided to connect to external transceivers, if desired.

Fibre Channel Protocol Manager

The ISP2300 FPM has the following features:

- Support for one Fibre Channel port
- Support for 1-gigabit and 2-gigabit serial interfaces
- Full-duplex data transfer rate up to 400 Mbytes/sec
- 10-bit interface to external transceivers
- Integrated frame buffer that supports up to a 2112-byte frame payload
- 8B/10B encoder and decoder with clock skew management
- Support for an external frame buffer

The FPM transmits and receives data at the full Fibre Channel rate of 106.25 or 212.50 Mbytes/sec. The on-chip frame buffer includes separate areas for received data and transmit data, as well as areas for managing special frames such as command and response. The FPM receive path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer. The transmit path transmits frames from the frame buffer to the Fibre Channel. The FPM automatically handles frame delimiters and frame control.

The external buffer supports additional receive buffering for 10-km optical Fibre Channel links to eliminate dead time and allow a remote transmitter to send frames continuously. Enough initial buffer credit can then be issued by the ISP2300 to keep a remote transmitter busy until one or more R_RDYs are received.

PCI Interface

The ISP2300 PCI interface has the following features:

- 33-MHz and 66-MHz 64-bit intelligent bus master conventional PCI interface (PCI 2.2)
- 64-bit host memory addressing (dual-address cycle)
- Five-channel DMA controller
- 32-bit PCI target mode for communication with the host
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit DMA transfer counter for I/O transfer length of up to four gigabytes
- Support for PCI power management
- Support for the *message signaled interrupt* function
- Support for flash BIOS PROM
- Support for subsystem ID
- 3.3-V and 5.0-V tolerant PCI I/O buffers

The ISP2300 is designed to interface directly to the PCI bus and operate as a 64-bit DMA bus master. This function is accomplished through a PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard frame buffer. It also allows the host to access the ISP2300 internal registers and communicate with the onboard RISC processor.

The ISP2300 supports the minimum power management capabilities specified in revision 1.1 of the *PCI Bus Power Management Interface Specification*, which defines power states D0-D3, where D0 provides maximum power consumption and D3 provides minimal power consumption. The D3 power state is entered by either software (D3 *hot*) or by physically removing power (D3 *cold*). Hot and cold refer to the presence or absence of VCC, respectively.

The ISP2300 supports power states D0, D3 hot, and D3 cold.

The ISP2300 onboard DMA controller consists of five independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and frame buffer. The command DMA channel is used mainly by the RISC processor for small transfers. The two data DMA channels, one to transmit and one to receive, transfer data between the FC-AL and the PCI bus. The auto-DMA request channel fetches commands from host memory over the PCI bus. The auto-DMA response channel posts status information to host memory.

The PBIU internally arbitrates between the five DMA channels and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

RISC Processor

The ISP2300 RISC processor has the following features:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

One of the major features of the ISP2300 is its ability to handle complete I/O transactions from start to finish with no host intervention. This high level of integration is accomplished with the onboard RISC processor. The ISP2300 RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs; and maintains the required thread information for each transfer.

Packaging

The ISP2300 is available in a 388-pin plastic ball grid array (PBGA) package. The ISP2300 power supply voltages are 2.5 and 3.3, with I/O voltages up to 5.

Specifications are subject to change without notice.

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