ISP2310 Data Sheet

2-Gb Fibre Channel to 100-MHz PCI-X Controller

The ISP2310 is a highly integrated single-chip, PCI-X, bus master, Fibre Channel processor that targets storage, clustering, and networking applications. This chip connects a conventional PCI bus or PCI-X bus to a 2-Gb Fibre Channel loop or to a point-to-point Fibre Channel port.

The ISP2310 is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention.

The ISP2310 balances the advanced bus speeds and efficiency of PCI-X with exceptional 2-Gb Fibre Channel performance. Fibre Channel support for SCSI, IP, and VI allows the ISP2310 to target a wide spectrum of storage and system area networks (SANs).

Features

- 66/100-MHz, 64-bit PCI-X host bus interface
- Backward compatible to standard 33/66-MHz PCI
- 5-V tolerant PCI interface
- Compliance with *PCI Local Bus Specification* revision 2.2 and *PCI-X Addendum* revision 1.0a
- Supports Fibre Channel-arbitrated loop (FC-AL), FC-AL-2, point-to-point, and switched fabric topologies
- Supports full-duplex communications in all Fibre Channel topologies
- Supports Fibre Channel protocol-SCSI (FCP-SCSI), Fibre Channel Internet Protocol (IP), and Fibre Channel-virtual interface (FC-VI) protocol
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.1 (PC99)
- Compliance with ANSI SCSI standards for class 1, class 2, class 3, and intermix Fibre Channel service:
  - *Second Generation FC Generic Services Definition* (FC-GS-2), NCITS 288.200x, Project 1134-D, revision 5.3
  - *Third Generation FC Generic Services Definition* (FC-GS-3) draft, revision 6.2
  - *Fibre Channel-Physical and Signaling Interface* (FC-PH), X2.230:1994
  - *SCSI-3 Fibre Channel Protocol* (SCSI-FCP), X3.269:1996
  - *Fibre Channel-Arbitrated Loop-2* (FC-AL-2), Project 1133-D, revision 6.5
  - *Fibre Channel-Private Loop Direct Attach Technical Report* (FC-PLDA), NCITS/TR-19:1998
  - *SCSI-3 Architecture Model* (SAM), X3T10/994D/Rev 18
  - *SCSI-3 Controller Command Set*, X3T10/Project 1047D/Rev 6c
- Supports up to 400 MBps sustained Fibre Channel data transfer rate
- Supports SCSI initiator, initiator/target, and target modes
- On-board, enhanced RISC processor
- On-board 2-Gb serial transceivers
- Automatically negotiates the Fibre Channel bit rate (1 or 2 Gb)
- Supports PCI dual-address cycle and cache commands
- No host intervention required to execute complete SCSI, IP, or VI operations
- Supports multi-ID aliasing in target mode
- Supports JTAG boundary scan and full scan

Subsystem Organization

To maximize I/O throughput and improve host and Fibre Channel utilization, the ISP2310 incorporates a high-speed, proprietary RISC processor; a Fibre Channel protocol manager (FPM); integrated frame buffer memory; and a host bus, five-channel, bus master DMA controller. The FPM and host bus DMA controller operate independently and concurrently under the control of the on-board RISC processor for maximum system performance.

The complete I/O subsystem solution using the ISP2310 and directly connected hard drives is shown in figure 1.

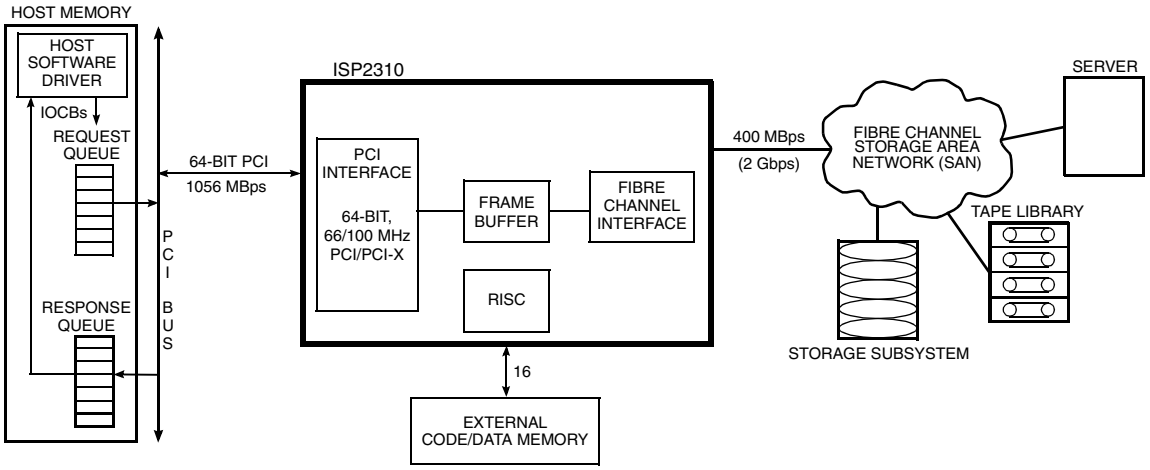

Figure 1. I/O Subsystem Design Using the ISP2310

PCI-X Interface

The ISP2310 PCI-X interface has the following features:

- 66-MHz or 100-MHz 64-bit intelligent bus master PCI-X interface
- 33-MHz and 66-MHz 64-bit intelligent bus master conventional PCI interface (PCI 2.2)
- 64-bit host memory addressing (dual-address cycle)
- Five-channel DMA controller
- 32-bit PCI target mode for communication with the host
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit DMA transfer counter for I/O transfer length of up to four gigabytes
- Support for PCI-X split transactions
- Support for PCI power management
- Support for the message signaled interrupt function
- Support for flash BIOS PROM
- Support for subsystem ID
- 3.3-V and 5.0-V tolerant PCI-X I/O buffers

The ISP2310 is designed to interface directly to the PCI or PCI-X bus and operate as a 64-bit DMA bus master. This function is accomplished through a PCI bus interface unit (PBIU) containing an on-board DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the on-board frame buffer. It also allows the host to access the ISP2310 internal registers and communicate with the on-board RISC processor.

The ISP2310 on-board DMA controller consists of five independent DMA channels that initiate transactions on the PCI-X bus and transfer data between the host memory and the frame buffer or RISC RAM.

The PBIU internally arbitrates between the five DMA channels and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

Fibre Channel Interface

The ISP2310 provides an on-board 2-Gb transceiver for direct connection to the Fibre Channel port on copper media.

Fibre Channel Protocol Module

The ISP2310 FPM has the following features:

- Support for one Fibre Channel port
- Support for 1-Gb and 2-Gb serial interfaces
- Auto-negotiation to support 1-Gb or 2-Gb devices
- Full-duplex data transfer rate up to 400 MBps
- Integrated frame buffer that supports up to a 2112-byte frame payload
- 8b/10b encoder and decoder with clock skew management
- Support for an external frame buffer

The FPM transmits and receives data at the full Fibre Channel rate of 106.25 or 212.50 MBps. The on-chip frame buffer includes separate areas for received data and transmit data, as well as areas for managing special frames such as command and response. The FPM receive path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer. The transmit path transmits frames from the frame buffer to the Fibre Channel. The FPM automatically handles frame delimiters and frame control.

The external buffer supports additional receive buffering for 10-km optical Fibre Channel links to eliminate dead time and allow a remote transmitter to send frames continuously. Enough initial buffer credit can then be issued by the ISP2310 to keep a remote transmitter busy until one or more R_RDYs are received.

RISC Processor

The ISP2310 RISC processor has the following features:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

One of the major features of the ISP2310 is its ability to handle complete I/O transactions from start to finish with no host intervention. This high level of integration is accomplished with the on-board RISC processor. The ISP2310 RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs; and maintains the required thread information for each transfer.

Multiprotocol Support

The ISP2310 firmware implements a multitasking host adapter that provides the host system with IP communications, complete SCSI command and data transport capabilities, and VI communications, thus freeing the host system from simultaneous execution of SCSI, IP, and VI traffic. The firmware provides two interfaces to the host system: the command interface and the Fibre Channel transport interface. The single-threaded command interface facilitates debugging, configuration, and error recovery. The multithreaded transport interface maximizes use of the Fibre Channel and host buses.

The ISP2310 can operate simultaneously in SCSI initiator and target modes, and supports SCSI, IP, and VI protocols concurrently.

Software Drivers

The ISP2310 supports a host software interface similar to the QLogic parallel SCSI and 1-Gb Fibre Channel processor families. Existing ISP2100A/2200A software drivers for all major operating systems are easily modified to support the ISP2310. The ISP2310 also supports FCP-SCSI, IP, and VI software drivers for most major operating systems.

Packaging

The ISP2310 is available in a 388-pin plastic ball grid array (PBGA) package. The ISP2310 power supply voltages are 2.5 and 3.3, with I/O voltages up to 5.

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