ITE 聯陽半導體 ITE Tech. Inc.

IT2646E

6 CHANNEL AC97 AUDIO CODEC

Preliminary Specification 0.3

INTEGRATED TECHNOLOGY EXPRESS, INC.

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Additional copies of this manual or other ITE literature may be obtained from:

ITE, Inc.
Marketing Department
8F, No. 233-1, Bao Chiao RD., Hsin Tien,
Taipei County 231, Taiwan, R.O.C.

Phone: (02) 29126889
Fax: (02) 2910-2551, 2910-2552

If you have any marketing or sales questions, please contact:

P.Y. Chang, at ITE Taiwan: E-mail: p.y.chang@ite.com.tw, Tel: 886-2-29126889 X6052, Fax: 886-2-29102551

To find out more about ITE, visit our World Wide Web at:

http://www.ite.com.tw

Or e-mail **itesupport@ite.com.tw** for more product information/services

Revision History

Section	Revision	Page No.
6	• In the Mixer Registers table, D9, D5 and D1 of Reg 5Ch and 78h was revised to "**X**" and the default value for Reg 78h was revised to "**0000h**".	11,12
	• For register MX5C, the description of bit 9, 5 and 1was revised to "**reserved**".	26
	• For register MX78, the description of bit 9, 5 and 1was revised to "**reserved**".	31
9	• In section 9.1, the parameter was revised to "**S/N ADC[1]**" and the value was revised to "**80min. 85tpy**". • In section 9.1, the parameter was revised to "**S/N ADC[2]**" and the value was revised to "**80min. 90tpy**".	43
	• Note 3 was revised to "**Full scale analog input, 20KHz baud width**".	44

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FIGURES

TABLES

1. Features

- **Single chip Audio Codec**
- **Supports 18-bit ADC and DAC resolution**
- **Compliant with AC'97 2.3 specification**
- **Meets the audio performance requirements of PC2001**
- **Supports 1Hz resolution variable sampling rates**
- **Line output with headphone driving capability**
- **Provides 4 analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, VIDEO and AUX**
- **Provides the following two analog line-level mono inputs: PC_BEEP, PHONE_IN**
- **Provides 1 analog line-level mono output: MONO_OUT**
- **Stereo output with 5-bit volume control**
- **6 channel slot selectable DAC output for multi-channel applications**
- **One standard MIC1 input, and one dedicated MIC3 input for front panel applications (software selectable)**
- **LINE Inputs shared with surround output; MIC1 and MIC2 shared with Center and LFE output**
- **2 MIC inputs, which are software selectable**
- **Power management capabilities**
- **3D Stereo adjustable**
- **Embedded 50mW/20ohm OP at front LINE output**
- **External amplifier power down capability**
- **Digital S/PDIF output**
- **Digital S/PDIF input**
- **No external crystal/clock required**
- **Supports 1 general purpose I/O pin**
- **Power supply:**
  Digital: 3.3V; Analog: 5V
- **Standard 48-Pin LQFP Package**

2. General Description

The IT2646E is an AC97 compatible Audio Codec for PC multimedia that delivers high quality audio.

The device contains 18-bit full-duplex stereo Codec with independent variable sampling rate in 1Hz resolution ranging from 8k to 48k, and provides 4 analog stereo inputs: LINE IN, CD, VIDEO, and AUX. Also included are ITE's 3D stereo adjustable, the headphone driver and an extra true line-level out for speaker amplifiers. The CD input is pseudo-differential for high signal quality. Two separate mono inputs are also provided for the down-line speakerphone and PC beep, and a mono microphone input is switchable from MIC 1 and MIC 3.

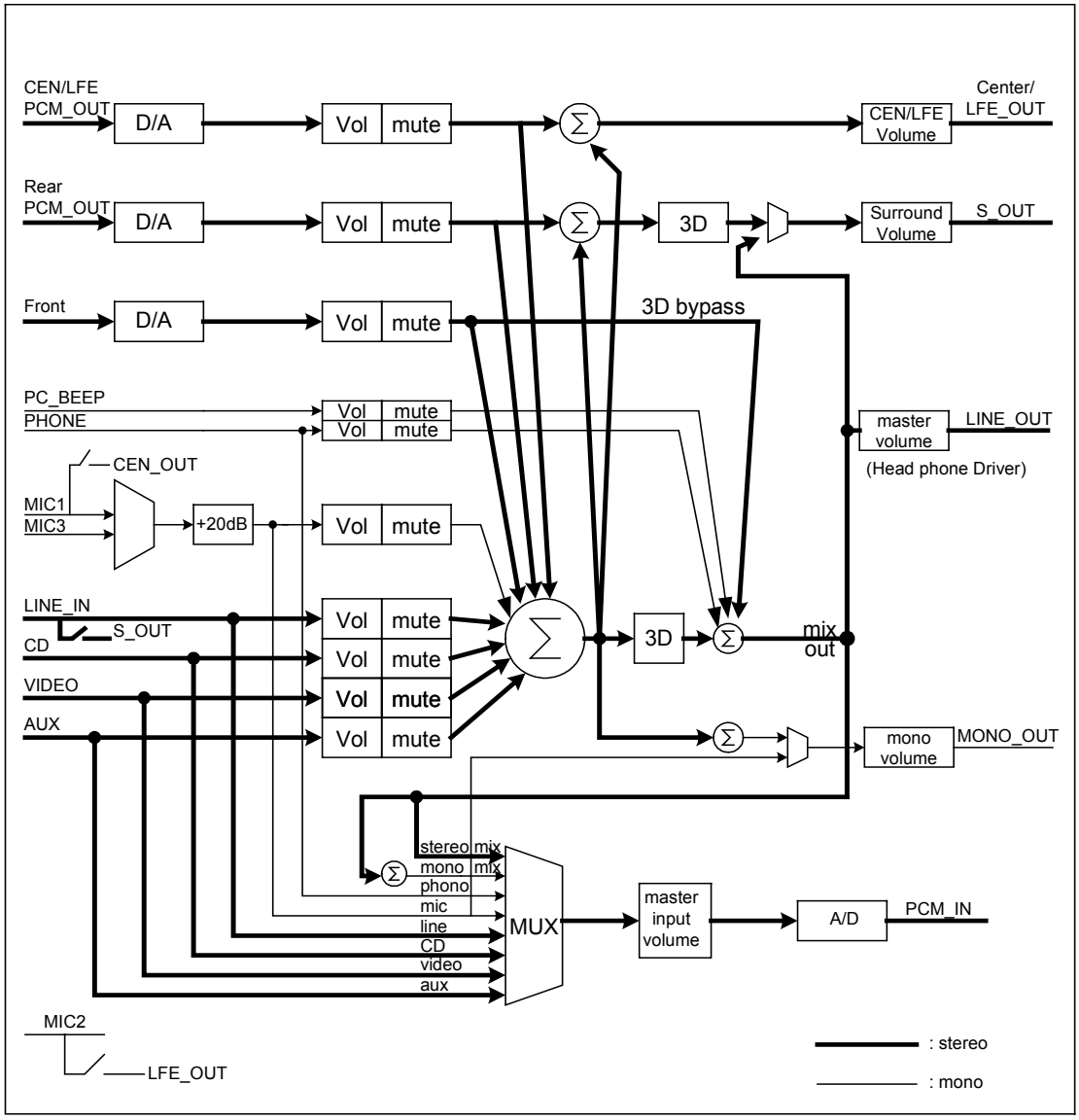
A line out mixer stage is used to mix any combination of the 4 analog stereo inputs, the selected MIC input, the two mono inputs, and the 6-channel DAC playback output. The line output level is controlled by Master Volume Attenuators, where the output signal can be attenuated from 0 dB to -46.5 dB in 1.5 dB steps, plus mute. The line out can drive the headphone directly.

Each of the analog inputs is equipped with programmable gain amplifier from +12 to -34.5 dB in 1.5 dB steps, plus mute. Together with the control registers, digital audio samples (record and playback) are accessible via an AC link serial bus interface. Record level can be amplified from 0 dB to +22.5 dB, or muted.

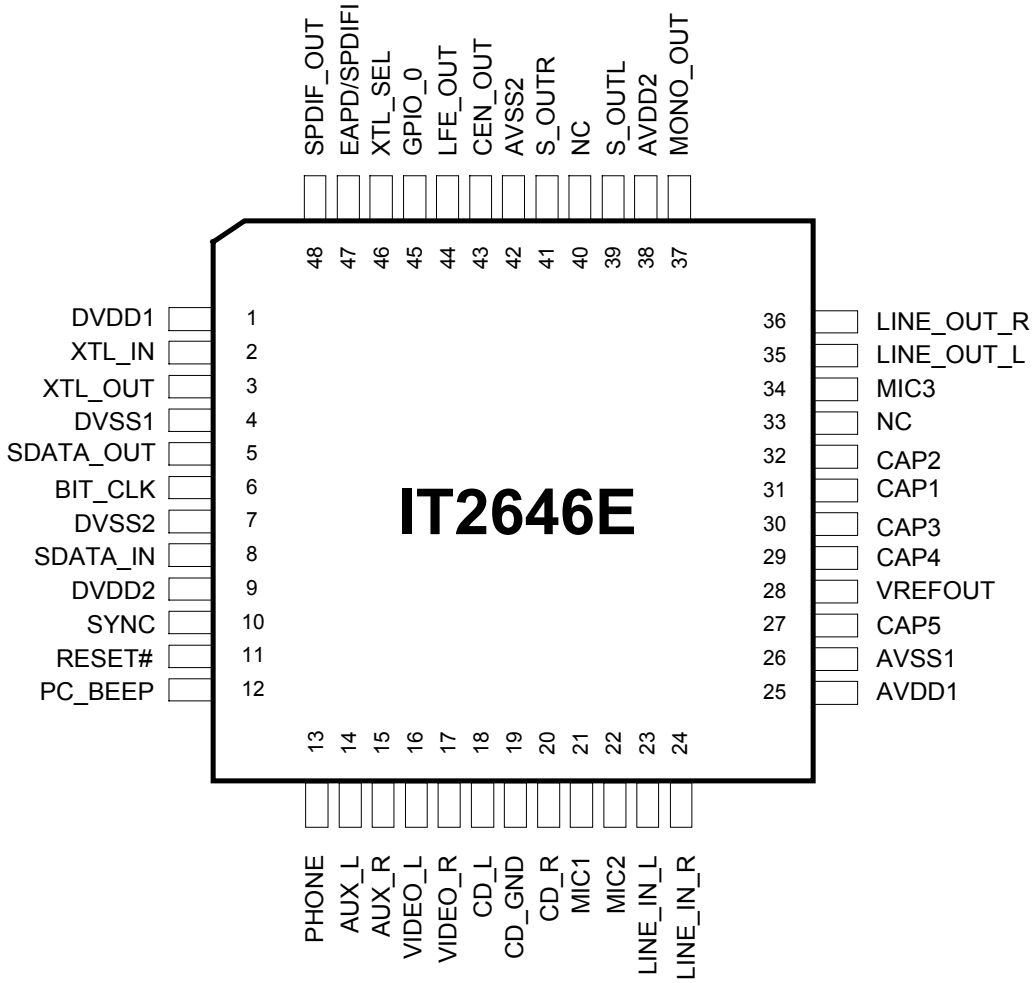
The IT2646E operates from a single external 24.576 MHz crystal or 14.318MHz clock source. Additionally, when the platform is not actively in use, the device's power management supports the low power mode, which reduces the overall system power consumption.

The device is available in a standard 48-pin LQFP (Low Profile Flat Package).

3. Block Diagram



4. Pin Configuration



5. IT2646E Pin Descriptions and Pinout Table

Table 5-1. IT2646E Pin Descriptions

Pin #	Symbol	Attribute	A/D	Description
11	RESET#	I	D	*AC97 Master H/W Reset#.*
2	XTL_IN	I	D	*24.576 MHz/14.318MHz Crystal input or clock source input.*
3	XTL_OUT	O	D	*24.576 MHz/14.318MHz clock output.*
10	SYNC	I	D	*48 kHz Fixed Rate Sample Sync.*
6	BIT_CLK	I/O	D	*12.288 MHz Serial Data Clock.*
5	SDATA_OUT	I	D	*Serial, Time Division Multiplexed.* AC97 Input Stream.
8	SDATA_IN	O	D	*Serial, Time Division Multiplexed.* AC97 Output Stream.
12	PC_BEEP	I	A	*PC Speaker Beep Pass Through.*
13	PHONE	I	A	*From Telephony Sub-system Speakerphone. (or DLP-Down Line Phone).*
21	MIC1	I/O	A	*Desktop Microphone Input/CENTER-OUT*
22	MIC2	O	A	*Alternative LFE-OUT*
23	LINE_IN_L	I/O	A	*Line In Left Channel/S-OUT-L*
24	LINE_IN_R	I/O	A	*Line In Right Channel/S-OUT-R*
18	CD_L	I	A	*CD Audio Left Channel.*
19	CD_GND	I	A	*CD Audio Analog Ground.*
20	CD_R	I	A	*CD Audio Right Channel.*
16	VIDEO_L	I	A	*Video Audio Left Channel.*
17	VIDEO_R	I	A	*Video Audio Right Channel.*
14	AUX_L	I	A	*AUX Left Channel.*
15	AUX_R	I	A	*AUX Right Channel.*
35	LINE_OUT_L	O	A	*Left Channel of Line Out (Headphone driver).*
36	LINE_OUT_R	O	A	*Right Channel of Line Out (Headphone driver).*
39	SOUT_L	O	A	*Left channel of Surround Output*
40	NC	-	-	*NC*
41	SOUT_R	O	A	*Right channel of Surround Output*
37	MONO_OUT	O	A	*Speakerphone Output.*
27	CAP5	O	A	*Filter Cap 5.*
28	VREFOUT	O	A	*Reference Voltage Out 5mA Drive (intended for MIC bias).*
29	CAP 4	O	A	*Filter Cap 4.*
30	CAP 3	O	A	*Filter Cap 3.*
31	CAP 1	O	A	*Filter Cap 1.*
32	CAP 2	O	A	*Filter Cap 2.*
33	NC	-	-	*NC*
34	MIC3	I	A	*Second Microphone Input*
43	CEN-OUT	O	A	*Center Output.*
44	LFE-OUT	O	A	*LFE Output.*

Table 5-1. IT2646E Pin Descriptions [cont'd]

Pin #	Symbol	Attribute	A/D	Description
25	**AVDD1**	I	A	***Analog Vdd – 5.0V.***
38	**AVDD2**	I	A	***Analog Vdd – 5.0V.***
26	**AVSS1**	I	A	***Analog Gnd.***
42	**AVSS2**	I	A	***Analog Gnd.***
1	**DVDD1**	I	D	***Digital Vdd – 3.3V.***
9	**DVDD2**	I	D	***Digital Vdd – 3.3V.***
4	**DVSS1**	I	D	***Digital Gnd.***
7	**DVSS2**	I	D	***Digital Gnd.***
45	**GPIO 0**	I/O	D	***General Purpose Input/Output 0***
46	**XTLSEL**	I	D	***Select clock input frequency is 24.576MHz or 14.318MHz .***
47	**EAPD/SPDIFI**	O	D	***External Audio Amplifier Enabled or S/PDIF Input.***
48	**SPDIF_OUT**	O	D	***S/PDIF Output.***

I = Input, **O** = Output, **A** = Analog, **D** = Digital
XTLSEL:
XTLSEL=floating or pull high, the clock source is 24.576MHz crystal or external clock.
XTLSEL=pull low, the clock source is 14.318MHz crystal or external clock.

Table 5-2. IT2646E Pinout Table

Number	Name	Number	Name	Number	Name	Number	Name
1	**DVDD1**	**13**	**PHONE**	**25**	**AVDD1**	**37**	**MONO_OUT**
2	**XTL_IN**	**14**	**AUX_L**	**26**	**AVSS1**	**38**	**AVDD2**
3	**XTL_OUT**	**15**	**AUX_R**	**27**	**CAP1**	**39**	**SOUT_L**
4	**DVSS1**	**16**	**VIDEO_L**	**28**	**VREFOUT**	**40**	**NC**
5	**SDATA_OUT**	**17**	**VIDEO_R**	**29**	**CAP 2**	**41**	**SOUT_R**
6	**BIT_CLK**	**18**	**CD_R**	**30**	**CAP 3**	**42**	**AVSS2**
7	**DVSS2**	**19**	**CD_GND**	**31**	**CAP 4**	**43**	**CEN-OUT**
8	**SDATA_IN**	**20**	**CD_R**	**32**	**CAP 5**	**44**	**LFE-OUT**
9	**DVDD2**	**21**	**MIC1**	**33**	**NC**	**45**	**GPIO 0**
10	**SYNC**	**22**	**MIC2**	**34**	**MIC3**	**46**	**XTLSEL**
11	**RESET#**	**23**	**LINE_IN_L**	**35**	**LINE_OUT_L**	**47**	**EAPD/SPDIFI**
12	**PC_BEEP**	**24**	**LINE_IN_R**	**36**	**LINE_OUT_R**	**48**	**SPDIF_OUT**

6. System Configuration

6.1 Mixer Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0.

REG. (HEX)	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	7E80h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono-Out Volume	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PB3	PB2	PB1	PB0	X	8000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	X	X	X	20DB	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-InVolume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
14h	Video Volume	Mute	X	X	VL4	VL3	VL2	VL1	VL0	X	X	X	VR4	VR3	VR2	VR1	VR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG2	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
20h	General Purpose	POP	X	3D	X	DRSS1	DRSS0	MIX	MS	LPBK	LPBK_F	LPBK_S	LPBK_C	X	X	X	X	0070h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DP1	DP0	0000h
24h	Audio Interrupt and Paging Mechanism	I4	I3	I2	I1	I0	X	X	X	X	X	X	X	Pg3	Pg2	Pg1	Pg0	0000h
26h	Power Down Ctrl/Status	EAPD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	X	X	X	X	REV1	REV0	AMAP	LDAC	SDAC	CDAC	X	X	X	SPDIF	DRA	VRA	09C7h
2Ah	Extended Audio Status	X	X	PRK	PRJ	PRI	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	DRA	VRA	05F0h
2Ch	PCM front. Sample Rate	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR9	FSR8	FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0	BB80h
2Eh	PCM Surr. Sample Rate	SSR15	SSR14	SSR13	SSR12	SSR11	SSR10	SSR9	SSR8	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SSR1	SSR0	BB80h
30h	PCM LFE. Sample Rate	SSR15	SSR14	SSR13	SSR12	SSR11	SSR10	SSR9	SSR8	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SSR1	SSR0	BB80h
32h	PCM Input Sample Rate	ISR15	ISR14	ISR13	ISR12	ISR11	ISR10	ISR9	ISR8	ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0	BB80h
36h	Center/LFE Volume	Mute	X	X	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	X	X	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Surround Volume	Mute	X	X	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	X	X	RSR4	RSR3	RSR2	RSR1	RSR0	8080h
3Ah	S/PDIF Ctl	V	0	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	AUDIO	PRO	2000h
5Ah	Bit Stream Test Ctl ITE only	A2S	A2C	ST_EN	BTC12	BTC11	BTC10	BTC9	BTC8	BTC7	BTC6	BTC5	BTC4	BTC3	BTC2	BTC1	BTC0	0000h
5Bh	PLL Ctl ITE only	T3	M4	M3	M2	M1	M0	N7	N6	N5	N4	N3	N2	N1	N0	P1	P0	597Fh
5Ch	GPIO Status	X	X	X	X	X	X	X	G0OC	SP_I	X	X	G0I	X	X	X	G0IS	0000h
5Eh	Surr. DAC Volume	Mute	X	X	LSD4	LSD3	LSD2	LSD1	LSD0	X	X	X	RSD4	RSD3	RSD2	RSD1	RSD0	8808h
60h	Code class/rev	X	X	X	CI4	CI3	CI2	CI1	CI0	Rv7	Rv6	Rv5	Rv4	Rv3	Rv2	Rv1	Rv0	0000h
62h	PCI SVID	PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8	PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0	0000h
64h	PCI SID	PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	0000h
66h	Function Select	X	X	X	X	X	X	X	X	X	X	X	X	FC3	FC2	FC1	FC0	0000h
68h	Function Information	G4	G3	G2	G1	G0	INV	DL4	DL3	DL2	DL1	DL0	IV	X	X	X	FIP	0000h
6Ah	Sense details	ST2	ST1	ST0	S4	S3	S2	S1	S0	OR1	OR0	SR5	SR4	SR3	SR2	SR1	SR0	0000h

Mixer Registers [cont'd]

REG. (HEX)	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
6Ch	DAC Slot Mapping	FD3	FD2	FD1	FD0	SD3	SD2	SD1	SD0	CLD3	CLD2	CLD1	CLD0	X	FC	SC	CLC	3760h
6Eh	ADC slot Mapping	LIA3	LIA2	LIA1	LIA0		SY2	SY1	SY0	SPI3	SPI2	SPI1	SPI0	X	X	X	MV	3400h
70h	S/PDIF Input Channel Status [15:0]	LEVEL	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Mode1	Mode0	REF2	REF1	REF0	COPY	/Audio	PRO	0000h
72h	S/PDIF Input Status [29:15]	X	X	Ca1	Ca0	Fs3	Fs2	Fs1	Fs0	Cn3	Cn2	Cn1	Cn0	Sn3	Sn2	Sn1	Sn0	0200h
74h	GPIO	GP15	GP14	GP13	GP12	GP11	GP10	PLLPD	JDS	JDE	CSS	P47C	P45C	ANC3	ANC2	ANC1	ANC0	0000h
76h	Multi-Channel Control	SAI	HDS	FDAC	ADCS	PCM2AC	MICOC	LINEINOC	LPFC	LPFE1	LPFE0	AIPC	AIPS	X	CDMC	SCDMC	SOS	0000h
78h	GPIO Setup	GSI	X	X	X	X	X	X	G0IP	SP_IE	X	X	G0IE	X	X	X	G0PC	0000h
7Ah	CEN/LFE DAC Volume	Mute	X	X	LD4	LD3	LD2	LD1	LD0	X	X	X	CD4	CD3	CD2	CD1	CD0	8808h
7Ch	Vendor ID1	0	1	0	0	1	0	0	1	0	1	0	1	0	1	0	0	4954h
7Eh	Vendor ID2	0	1	0	0	0	1	0	1	0	1	1	0	0	0	0	0	4560h

X: reserved bit
*: MX36 is the master volume control of CENTER/LFE output.
MX38 is the master volume control of surround output.

6.1.1 MX00 Reset

Default: 7E80H

When a value is written to this register, a register reset is performed, which will cause all registers to revert to their default values. Reading this register returns the ID code of the part. For IT2646E, the ID codes are provided below:

Bit	R/W	Default	Description
15	RO	0	**Reserved**
14-10	RO	11111	**SE4 – SE0** **3D Stereo Enhancement Technique** When these bits are written by 1, it indicates the corresponding function exists.
9	RO	1	**ID9** **20-bit ADC Resolution** When this bit is written by 1, it indicates the corresponding function exists.
8	RO	0	**ID8** **18-bit ADC Resolution**
7	RO	1	**ID7** **20-bit DAC Resolution** When these bits are written by 1, it indicates the corresponding function exists.
6	RO	0	**ID6** **18-bit DAC Resolution**
5	RO	0	**ID5** **Loudness (Bass Boost) Support**
4	RO	0	**ID4** **Headphone Out Support, NOTE 1**
3	RO	0	**ID3** **Simulated Stereo (Mono or Stereo)**
2	RO	0	**ID2** **Bass & Treble Control**
1	RO	0	**ID1** **Modem Line Codec Support**
0	RO	0	**ID0** **Dedicated Mic PCM In Channel**

Note 1: Headphone driver is supported at Master Volume Control

6.1.2 MX02 Master Volume

Default: 8000H

These registers control the overall volume level of the output functions. Each step on the left and right channels corresponds to 1.5dB in increase/decrease in volume.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:13	-	0	**Reserved**
12:8	R/W	0	**Master Left Volume** ML[4:0] in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	0	**Master Right Volume** MR[4:0] in 1.5 dB steps

For MR/ML, 00h 0dB attenuation
1Fh 46.5dB attenuation

6.1.3 MX06 MONO_OUT Volume

Default: 8000H

Register 06H controls the mono volume output. Each step corresponds to 1.5dB in increase/decrease in volume.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:5	-	0	**Reserved**
4:0	R/W	0	**Mono Master Volume** MM[4:0] in 1.5 dB steps

For MM, 00h 0 dB attenuation
1Fh 46.5 dB attenuation

6.1.4 MX0A PC BEEP Volume

Default: 8000H

This register is responsible for controlling the level for the PC Beep input. Each step corresponds to 3 dB of attenuation. The MSB of the register is the mute bit. The default value is 0000h or 8000h, which corresponds to 0 dB of attenuation with mute off or on.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:5	-	0	**Reserved**
4:1	R/W	0	**PC Beep Volume** PB[3:0] in 3 dB steps
0	-	0	**Reserved**

For PB, 00h 0dB attenuation
0Fh 45dB attenuation

6.1.5 MX0C PHONE Volume
Default: 8008H

This register controls the gain/attenuation for the PHONE analog input. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:5	-	0	**Reserved**
4:0	R/W	01000	**Phone Volume** (PV[4:0]) in 1.5 dB steps

For PV, 00h +12dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.6 MX0E MIC Volume
Default: 8008H

This register controls the gain/attenuation for the MIC analog input. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. Register has an extra bit (bit 6) provided for a 20dB boost.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:7	-	0	**Reserved**
6	R/W	0	**20 dB Boost Control** 0: Normal 1: 20 dB boost
5	-	0	**Reserved**
4:0	R/W	01000	**Mic Volume** MV[4:0] in 1.5 dB steps

For MV, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.7 MX10 LINE_IN Volume
Default: 8808H

This register controls the gain/attenuation for the LINE_IN analog inputs. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:13	-	0	**Reserved**
12:8	R/W	01000	**Line-In Left Volume** NL[4:0] in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	01000	**Line-In Right Volume** NR[4:0] in 1.5 dB steps

For NL/NR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.8 MX12 CD Volume
Default: 8808H

This register controls the gain/attenuation for the CD_IN analog inputs. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:13	-	0	**Reserved**
12:8	R/W	01000	**CD Left Volume** CL[4:0] in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	01000	**CD Right Volume** CR[4:0] in 1.5 dB steps

For CL/CR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.9 MX14 VIDEO Volume
Default: 8808H

This register controls the gain/attenuation for the VIDEO_IN analog inputs. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:13	-	0	**Reserved**
12:8	R/W	01000	**Video Left Volume** VL[4:0] in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	01000	**Video Right Volume** VR[4:0] in 1.5 dB steps

For VL/VR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.10 MX16 AUX Volume
Default: 8808H

This register controls the gain/attenuation for the AUX_IN analog inputs. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:13	-	0	**Reserved**
12:8	R/W	01000	**AUX Left Volume** AL[4:0] in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	01000	**AUX Right Volume** AR[4:0] in 1.5 dB steps

For AL/AR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.11 MX18 FRONT PCM_OUT Volume
Default: 8808H

This register controls the gain/attenuation for the FRONT PCM_OUT analog outputs. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:13	-	0	**Reserved**
12:8	R/W	01000	**PCM Left Volume** PL[4:0] in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	01000	**PCM Right Volume** PR[4:0] in 1.5 dB steps

For PL/PR, 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.12 MX1A Record Select
Default: 0000H

This register is used to select the record source independently for the right and left channel.

Bit	R/W	Default	Description
15:11	-	0	**Reserved**
10:8	R/W	0	**SR2 – SR0**
7:3	-	0	**Reserved**
2:0	R/W	0	**SL2 – SL0**

SR2 – SR0	Right Record Source
000	Mic
001	CD in (R)
010	Video in (R)
011	Aux in (R)
100	Line in (R)
101	Stereo Mix (R)
110	Mono Mix
111	Phone

SL2 – SL0	Left Record Source
000	Mic
001	CD in (L)
010	Video in (L)
011	Aux in (L)
100	Line in (L)
101	Stereo Mix (L)
110	Mono Mix
111	Phone

6.1.13 MX1C Record Gain

Default: 8000H

The 1Ch register is used for the stereo input. Each step corresponds to 1.5 dB. The MSB of the registers is the mute bit. The default value is 8000h, which corresponds to 0 dB gain with mute on.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute - ∞ dB Attenuation
14:12	-	0	**Reserved**
11:8	R/W	0	**Left Record Gain Select** LRG[3:0] in 1.5 dB steps
7:4	-	0	**Reserved**
3:0	R/W	0	**Right Record Gain Select** RRG[3:0] in 1.5 dB steps

For LRG/RRG, 0Fh +22.5dB
00h 0 dB (No Gain)

6.1.14 MX20 General Purpose Register

Default: 0070H

This register is used to control several miscellaneous functions of the AC97 component.

Bit	R/W	Default	Description
15:14	-	0	**Reserved** Read as 0
13	R/W	0	**3D Control** 1: On 0: Off
12	-	0	**Reserved** Read as 0
11:10	R/W	00	**DRSS: Double Rate Slot Select**
9	R/W	0	**Mono Output Select** 0: MIX 1: MIC
8	R/W	0	**Mic Select** 0: MIC1 1: (MIC1+MIC3)/2 Both MX20.8 and MX76.10 configure MIC1/MIC3 inputs. Refer to MX76.10 for another information.
7	R/W	0	**LPBK: AD to DA Loop-Back Control** 0: Disable 1: Enable
6	R/W	1	**LPBK_F**
5	R/W	1	**LPBK_S**
4	R/W	1	**LPBK_C**
3:0	-	0	**Reserved**

LPBK=1, and
LPBK_F=1,then AD to 1st PCM (R&L)
LPBK_S=1,then AD to 2nd PCM (Surround)
LPBK_C=1,then AD to 3rd PCM (Center/LFE)
DRSS[1:0]: Double Rate Slot Select
00:PCM L,R,C n+1 data is on Slots 10-12(default)
01:PCM L,R n+1 data is on slots 7,8
Others: Reserved

6.1.15 MX22 3D Control
Default: 0000H

This register is used to control the 3D sound depth. The default value here is 0000H, which means the 3D stereo enhancement is variable. Only DP0 and DP1 are adjustable.

Bit	R/W	Default	Description
15-2	RO	0h	**Reserved**
1-0	R/W	0h	**DP1-DP0** 3D enhancement depth control 00: 25%, 01: 50%, 10: 75%, 11: 100%

6.1.16 MX24 Audio Interrupt and Paging Mechanism
Default: 0000H

The register is defined to support Audio interrupt and register paging mechanism.

Bit	R/W	Default	Description
15	R/W	0	**Interrupt Status:** 0 – Interrupt is clear 1 – Interrupt was generated
14-13	RO	0	**Interrupt Cause**
12	RO	0	**Sense Cycle**
11	RO	0	**Interrupt Enable**
10:4	-	0	**Reserved** Read as 0
3:0	RO	0	**Page Selector**

6.1.17 MX26 Power down Control/Status
Default: 000FH

This register is used to program the power down states and monitor sub-system readiness. The lower half of this register is in the read only status. A "1" indicates that the sub-section is ready (i.e. the sub-section is able to perform in its nominal state). Bits 0-7 are read only bits. The power down modes are shown in bit 15-8. Bits 10-8 are to be used individually rather than in combination with each other. Bit 11 PR3 can be used in conjunction with bit 10 PR2 or by itself.

Bit	R/W	Default	Description
15	R/W	0	**External Amplifier Power Down** (EAPD) 0: EAPD output low (enable external amplifier) 1: EAPD output high (shut down external amplifier)
14	-	0	**Reserved**
13	R/W	0	R/W PR5 0: Normal 1: Disable internal clock usage (BCLK still be output for modem CODEC)
12	R/W	0	PR4 0: Normal 1: Power down AC-Link
11	R/W	0	PR3 0: Normal 1: Power down Mixer (Vref off)
10	R/W	0	PR2 0: Normal 1: Power down Mixer (Vref still on)
9	R/W	0	PR1 0: Normal 1: Power down PCM DAC (front DAC)
8	R/W	0	PR0 0: Normal 1: Power down PCM ADC and input MUX
7:4	-	0	**Reserved** Read as 0
3	R	1	**Vref Status** 1: Vref is up to normal level 0: Not yet

[cont'd]

2	R	1	**Analog Mixer Status** 1: Ready 0: Not yet
1	R	1	**DAC Status** 1: Ready 0: Not yet
0	R	1	**ADC Status** 1: Ready 0: Not yet

6.1.18 MX28 Extended Audio ID

Default: 09C7H

The Extended Audio ID register is a read only register that identifies which extended audio feature is supported.

Bit	R/W	Default	Description
15:14	R	0	**ID** Always read as 0
13:12	-	0	**Reserve**d Read as 0
11:10	R	10	**REV** [1:0]=01 to indicate that the IT2646E is AC'97 rev2.3 compliant
9	R	0	**AMAP** Read as 1 (DAC mapping base on CODEC ID)
8	R	1	**LDAC** Read as 1 (LFE DAC is supported, according to AC'97 rev2.3)
7	R	1	**SDAC** Read as 1 (Surround DAC is supported according to AC'97 rev2.2)
6	R	1	**CDAC** Read as 1 (Center DAC is supported according to AC'97 rev2.3)
5:3	-	0	**Reserved** Read as 0
2	R	1	**SPDI**F Read as 1 (S/PDIF is supported)
1	R	1	**DRA** Read as 1 (Double Rate Audio is supported)
0	R	1	**VRA** Read as 1 (Variable Rate Audio is supported)

6.1.19 MX2A Extended Audio Status and Control Register

Default: 05F0H

The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

Bit	R/W	Default	Description
15:14	-	0	**Reserved**
13	R/W	0	**Power Down LFE DA**C. (PRK) 0: Normal 1: Power down LFE DAC
12	R/W	0	**Power Down Surround DA**C. (PRJ) 0: Normal 1: Power down Surround DAC
11	R/W	0	**Power Down Center DA**C. (PRI) 0: Normal 1: Power down Center DAC
10	R	1	**SPCV** (S/PDIF Configuration Valid) * 0: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is not valid. 1: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is valid.
9	-	0	**Reserved**
8	R	1	**LFE DAC Status** (LDAC). 0: Not yet 1: Ready
7	R	1	**Surround DAC Status** (SDAC). 0: Not yet 1: Ready
6	R	1	**Center DAC Status** (CDAC). 0: Not yet 1: Ready
5:4	R/W	11	**SPS**A[1:0] (S/PDIF Slot Assignment) 00: S/PDIF source data assigned to AC-LINK slot3/4 01: S/PDIF source data assigned to AC-LINK slot7/8 10: S/PDIF source data assigned to AC-LINK slot6/9 11: S/PDIF source data assigned to AC-LINK slot10/11 (default)
3	-	0	**Reserved**
2	R/W	0	**SPDIF Enable.** 1: Enable 0: Disable (Hi-Z)
1	R/W	0	**DRA Enable.** 1: Enable 0: Disable
0	R/W	0	**VRA Enable.** 1: Enable 0: Disable

6.1.20 MX2C PCM Front/Center Output Sample Rate

Default: BB80H

These R/W registers are used to set the sample rate for Front/Center DAC outputs.

Bit	R/W	Default	Description
15:0	R/W	BB80H	**FOSR** [15:0]Output sampling rate

The 16-bit unsigned value represents the sample rate in 1Hz resolution ranging from 8K to 48K. If MX2A.0=0 (VRA is disabled), this register is always BB80h.

6.1.21 MX2E PCM Surround Output Sample Rate

Default: BB80H

These R/W registers are used to set the sample rate for the Surround DAC outputs.

Bit	R/W	Default	Description
15:0	R/W	BB80H	**SOSR** [15:0]Output sampling rate

The 16-bit unsigned value represents the sample rate in 1Hz resolution ranging from 8K to 48K. If MX2A.0=0 (VRA is disabled), this register is always BB80h.

6.1.22 MX30 PCM LFE Output Sample Rate

Default: BB80H

These R/W registers are used to set the sample rate for LFE DAC output.

Bit	R/W	Default	Description
15:0	R/W	BB80H	**LOSR** [15:0]Output sampling rate

The 16-bit unsigned value represents the sample rate in 1Hz resolution ranging from 8K to 48K. If MX2A.0=0 (VRA is disabled), this register is always BB80h.

6.1.23 MX32 PCM Input Sample Rate

Default: BB80H

These R/W registers are used to set the sample rate for ADC output.

Bit	R/W	Default	Description
15:0	R/W	BB80H	**ISR** [15:0]Output sampling rate

The 16-bit unsigned value represents the sample rate in 1Hz resolution ranging from 8K to 48K. If MX2A.0=0 (VRA is disabled), this register is always BB80h.

6.1.24 MX36 LFE/Center Master Volume

Default: 8080

These registers control the LFE/Center volume level of the output functions. Each step on the left and right channels corresponds to 1.5dB in increase/decrease in volume. Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and read as x11111.

H

Bit Type Function

Bit	R/W	Default	Description
15	R/W	1	**LFE Mute Control** 0: Normal 1: Mute (-∞dB)
14:13	-	0	**Reserved**
12:8	R/W	0	**LFE Master Volume** (LFE[4:0]) in 1.5 dB steps
7	R/W	1	**Center Mute Control** 0: Normal 1: Mute (-∞dB)
6:5	-	0	**Reserved**
4:0	R/W	0	**Center Master Volume** (CNT[4:0]) in 1.5 dB steps

* For LFE/Center, 00h 0dB gain
1Fh -46.5dB gain

6.1.25 MX38 Surround Master Volume

Default: 8080H

These registers control the Surround volume level of the output functions. Each step on the left and right channels corresponds to 1.5dB in increase/decrease in volume. Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and read as x11111.

Bit Type Function

Bit	R/W	Default	Description
15	R/W	1	**Left Mute Control** 0: Normal 1: Mute (-∞dB)
14:13	-	0	**Reserved**
12:8	R/W	0	**Surround Master Left Volume** (LSR[4:0]) in 1.5 dB steps
7	R/W	1	**Right Mute Control** 0: Normal 1: Mute (-∞dB)
6:5	-	0	**Reserved**
4:0	R/W	0	**Surround Master Right Volume** (RSR[4:0]) in 1.5 dB steps

* For LSR/RSR, 00h 0dB gain
1Fh -46.5dB gain

6.1.26 MX3A S/PDIF Output Channel Status and Control

Default: 2000H

Bit	R/W	Default	Description
15	R/W	0	**Validity Control** (control V bit in Sub-Frame) 0: The V bit (valid flag) in sub-frame depends on whether the S/PDIF data is under-run or not. 1: The V bit in sub-frame is always sent as 1 to indicate the invalid data is not suitable for receiver.
14	R	0	**DRS** (Double Rate S/PDIF) The IT2646 does not support double rate S/PDIF and this bit is always 0.
13:12	R/W	01	**SPSR** [1:0] (S/PDIF Sample Rate) 00: Sample rate set to 44.1KHz. Fs[**0:**3]=0000 01: Reserved 10: Sample rate set to 48.0KHz. Fs[**0:**3]=0100 (default) 11: Sample rate set to 32.0KHz. Fs[**0:**3]=1100
11	R/W	0	**LEVEL** (Generation Level)
10:4	R/W	0	**CC** [6:0] (Category Code)
3	R/W	0	**PRE** (Preemphasis) 0: None 1: Filter preemphasis is 50/15 μsec
2	R/W	0	**COPY** (Copyright) 0: Asserted 1: Not asserted
1	R/W	0	**/AUDIO** (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	0	**PRO** (Professional or Consumer format) 0: Consumer format 1: Professional format IT2646E supports consumer channel status format. This bit is always 0

6.1.27 MX5A Bit Stream Test Control Register only for ITE users

This register is used to control the test bit stream.

Default: 0000H

Bit	R/W	Default	Description
15	R/W	0	**Analog input to Surround**
14	R/W	0	**Analog input to Center/LFE**
13	R/W	0	**Schmitt trigger input control for S/PDIF input**
12	R/W	0	**BIT1: Bitstream loopback (D/A2A/D) for digital**
11	R/W	0	**VCMMIX_CTL test mode for analog**
10:9	R/W	0	**Reserved**
8	R/W	0	**Test mode for FIR bypass to SINC**
7:6	R/W	0	**Test mode for data of sdata_in in A/D**
5-3	R/W	0	**Test mode for bit stream**
2	R/W	0	**BIT0: Bitstream loopback (D/A2A/D) for digital**
1	R/W	0	**Bitstream loopback for analog**
0	R/W	0	**Reserved**

6.1.28 MX5B PLL Control Register only for ITE users

Default: 597Fh (XTL_SEL = 0), 401Fh (XTL_SEL = 1)

This register is used to control our built-in PLL block to get the right clock signal.

Bit	R/W	Default	Description
15	R/W	0	**T3** **Connect to PLL Block T[3]**
14:10	R/W	0	**M4-M0** **Connect to Block M[4:0]**
9-2	R/W	0	**N7-N0** **Connect to PLL Block N[7:0]**
1-0	R/W	0	**P1-P0** **Connect to PLL Block P[1:0]**

6.1.29 MX5C GPIO Status

Default: 0000h

Bit	R/W	Default	Description
15:10	-	0	**Reserved**
9	R/W	0	**Reserved**
8	R/W	0	**GPIO0 Output Control** 0: Drive GPIO0 as low 1: Drive GPIO0 as high
7	R/W	0	**S/PDIF-In Valid Interrupt Status** (SPDIFIN_VIS) 0: No S/PDIF-In valid interrupt. 1: S/PDIF-In Valid Interrupt.
6	R	0	**Reserved**
5	R/W	0	**Reserved**
4	R/W	0	**GPIO0 Interrupt Status** (GPIO0_IS). (When GPIO0 is used as input) 0: No GPIO0 interrupt 1: GPIO0 interrupt
3:2	-	0	**Reserved**
1	R	0	**Reserved**
0	R	0	**GPIO0 Input Status** 0: GPIO0 is driven low by external device (input). 1: GPIO0 is driven high by external device (input).

6.1.30 MX5E Surround DAC Volume

Default: 8808H

This register controls the gain/attenuation for the Surround PCM_OUT analog outputs. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute (-∞dB)
14:13	-	0	**Reserved**
12:8	R/W	01000	**Surround DAC Left** Volume (SDL[4:0]) in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	01000	**Surround DAC Right Volume** (SDR[4:0]) in 1.5 dB steps

For SDL/SDR, 00h +12dB gain
08h 0dB gain
1Fh -34.5dB gain

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6.1.31 MX60, MX62, MX64, MX66, MX6A in ITE2646 are all read only and the values are always "0".

6.1.32 MX6C DAC slot Mapping

Default: 3760H

Bit	R/W	Default	Description
15:12	R/W	0011	**FD : 1st PCM slot mapping**
11:8	R/W	0111	**SD : 2nd PCM slot mapping**
7:4	R/W	0110	**CLD : 3rd PCM slot mapping**
3	-	0	**Reserved**
2	R/W	0	**FC : 1st PCM interchange**
1	R/W	0	**SC : 2nd PCM interchange**
0	R/W	0	**CLC : 3rd PCM interchange**

FC=1, R&L interchange.
SC=1, Surround R& surround L interchange.
CLC=1, Center&LFE interchange.

6.1.33 MX6E ADC slot Mapping

Default: 3400H

Bit	R/W	Default	Description
15:12	R/W	0011	**LIA: Line In ADC slot mapping**
11		0	**Reserved**
10:8	R/W	100	**SY for ITE only**
7:4	R/W	0110	**SPI: S/PDIF Input ADC slot mapping**
3:1	-	0	**Reserved**
0	R/W	0	**MV: Mapping Valid**

The MV bit indicates that 6Ch and 6Eh are valid.

Valid Values for Slot Mapping Registers	
Value	Slots used by DAC/ADC
3h	Slots 3,4
6h	Slots 6,9
7h	Slots 7,8
Ah	Slots 10,11
0h	Not implement
1,2,4,5,8,9,B,C,D,E,F	Reserved

6.1.34 MX70 S/PDIF Input Channel Status [15:0]

Default: 0000H

Bit	R/W	Default	Description
15	R	0	**LEVEL** (Generation Level)
14:8	R	0	**CC** [6:0] (Category Code)
7:6	R	0	**Mode** [1:0]
5:3	R	0	**PRE** [2:0] (Pre-Emphasis)
2	R	0	**COPY** (Copyright) 0: Asserted 1: Not asserted
1	R	0	**/AUDIO** (Non-Audio Data type) 0: PCM data 1: AC3 or other digital non-audio data
0	R	0	**PRO** (Professional or Consumer format) 0: Consumer format 1: Professional format

* The data in MX70 are captured from channel status [15:0] of SPDIFInput.

6.1.35 MX72 S/PDIF Input Channel Status [29:15]

Default: 0000H

Bit	R/W	Default	Description
15	R	0	**Vbit in Sub-frame of SPDIF-In** This bit reflects the Validity status of SPDIF-In, and is effective only when SPDIF-In is locked. 0: Data X and Y are valid. 1: At least one of data X and Y is invalid. This bit is real-time updated, and has meaning only when SPDIF-In is locked.
14	R	0	**SPDIFI Input Signal** Locked by hardware 0: Unlocked 1: Locked
13:12	R	0	**Ca** [1:0] (Clock Accuracy)
11:8	R	0	**Fs** [3:0]. (Sample Frequency in channel status) 0000: 44.1KHz 0010: 48 KHz 0011: 32 KHz Others: Reserved
7:4	R	0	**Cn** [3:0] (Channel Number)
3:0	R	0	**Sn** [3:0] (Source Number)

6.1.36 MX74 GPIO Register

Default: 0000H

The MSB 6 bits of this register are used for analog general purpose I/O and bit 9 is used for built-in PLL block power down control. Bit 8 is used for disable/enable function. Bit 6 shows the selected clock source. Bit 5 is used to select either EAPD output or SPDIF input at Pin 47. Bit 4 is used to select either JD function or GPIO0 function.

Bit	R/W	Default	Description
15-10	R/W	0	**GP15-10**
9	R/W	0	**PLL PD**
8	R/W	0	**JD select** **When JD input is high, the output will be muted.** 0 : Line_out 1 : LNLVLOUT
7	R/W	0	**JD Disable** 0 : Disable JD Function 1 : Enable JD Function
6	R	0	**Clock Source Selection** 0 : XTL_IN is 24.576M 1 : XTL_IN is 14.318M
5	R/W	0	**Pin47 control** 0 : EAPD 1 : S/PDIF Input
4	R/W	0	**Pin45 control** 0 : JD 1 : GPIO0
3-0	R/W	0	**ANCanalog input clock delay control**

6.1.37 MX76 Multi-Channel Control

Default: 0000h

This register is used to control various parts of the ITE2646 multi-channel functions.

Bit Type Function

Bit	R/W	Default	Description
15	R/W	0	**SPDIF input sampling rate information** **0:hardware detect** **1:from channel status**
14	R/W	0	**Hardware Detect assign about spdif input sampling** **0:disable** **1:enable** **enable: hardware assign sampling when reg76.12 or reg76.11 set .**
13	R/W	0	**Front DAC Source** 0: AC-LINK Slot-3/4 (default) 1: SPDIF Input If PCM data are from SPDIFI, software must keep concurrence of sample rate of DAC and SPDIF input.
12	R/W	0	**S/PDIF Output Source** 0: S/PDIF output data is from controller (default). 1: S/PDIF output data is from ADC.
11	R/W	0	**PCM Data to AC-LINK** 0: PCM Data is from ADC (default). 1: PCM Data is from SPDIF input.
10	R/W	0	**MIC1 & MIC2 / CENTER & LFE Output Control** 0: Pin-21 is MIC1-In and pin-22 is floating (default). 1: Pin-21 is CENTER-Out and pin-22 is LFE-Out.
9	R/W	0	**Line-In / Surround Output Control** 0: Pin-23 and pin-24 are analog input (Line-In). (Default) 1: Pin-23 and pin-24 are duplicated output of surround channel. (Surround-Out)
8:6	---	-	**Reserved only for ITE users**
5	R/W	0	**Analog Input Pass to Center/LFE Control** 0: Off 1: On
4	R/W	0	**Analog Input Pass to Surround Control** 0: Off 1: On
3		0	**Reserved**
2	R/W	0	**Center/LFE Channel Down Mix Control.** 0: Disable down mix (default) 1: Down mix Center/LFE DAC output into LINE-OUT
1	R/W	0	**Surround Channel Down Mix Control.** 0: Disable down mix (default) 1: Down mix surround DAC output into LINE-OUT
0	R/W	0	**Surround Output Source.** 0: S-OUT is the real surround output. (Default) 1: S-OUT is the duplicated output of LINE-OUT.

6.1.38 MX78 GPIO Setup
Default: 0000h

Bit	R/W	Default	Description
15	R/W	0	**GPIO Statue Indication in SDATA_IN** 0: The status of GPIO and its valid tag are not indicated in SDATA_IN. 1: The status of GPIO and its valid tag are indicated in SDATA_IN.
14:10	-	0	**Reserved**
9	R/W	0	**Reserved**
8	R/W	0	**GPIO0 Interrupt Polarity** 0: Low to high transition (default) 1: High to low transition
7	R/W	0	**S/PDIF-In Valid Interrupt Enable** 0: Disable 1: Enable
6		0	**Reserved**
5	R/W	0	**Reserved**
4	R/W	0	**GPIO0 Interrupt Enable** (when GPIO0 is used as input) 0: Disable 1: Enable.
3:2	-	0	**Reserved**
1	R/W	0	**Reserved**
0	R/W	0	**GPIO0 Primitiveness Control** 0: Set GPIO0 as input pin 1: Set GPIO0 as output pin

6.1.39 MX7A Center/LFE DAC Volume
Default: 8808H

This register controls the gain/attenuation for the Surround PCM_OUT analog outputs. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit.

Bit	R/W	Default	Description
15	R/W	1	**Mute Control** 0: Normal 1: Mute (-∞dB)
14:13	-	0	**Reserved**
12:8	R/W	01000	**LFE DAC Volume** (LD[4:0]) in 1.5 dB steps
7:5	-	0	**Reserved**
4:0	R/W	01000	**Center DAC Volume** CD[4:0]) in 1.5 dB steps

* For LD/CD, 00h +12dB gain
08h 0dB gain
1Fh -34.5dB gain

6.2 Vendor ID1&2 (7Ch,7Eh)

Version 0: These two registers will show ITE-60.(4954,4560)
There are some bugs in version 0 and they will be modified in version 1.

Bugs: In Register 36h, 38h, 5Eh and 7Ah , register[4:0] and register[12:8] are interchanged.

Version 1: These two registers will show ITE-61.(4954,4561)

7. DC Electrical Characteristics

(DVDD1, DVDD2 = 3.3V±0.3V. AVDD1, AVDD2= 5.0V± 0.5V. Ta= 0ºC to 70ºC)

Absolute Maximum Ratings

Applied Voltage of DVDD1, DVDD2 ..... -0.3V to 4.6V
Applied Voltage of AVDD1, AVDD2 ..... -0.3V to 7.0V
Input Voltage of 3.3V Interface -0.3V to VCC3 + 0.3V
Input Voltage of 5.0V Interface -0.3V to VCC5 + 0.3V
Tcase ..... 0°C to 70°C
Storage Temperature ..... -55°C to 150°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.1 Operating Conditions

Parameter	Value	Unit
Power supply	Analog: 5.0 +/- 5% Digital: 3.3+/- 5%	V
Ambient temperature	0 - 70	°C
Max. dissipation	tbd	mW
Power down dissipation	tbd	mW

7.2 DC Electrical Characteristics (Ta= 0°C to 70°C)

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{in}	Input voltage range	-0.3	-	Vdd+0.3	V
V_{il}	Low level input voltage	-	-	0.30xVdd	V
V_{ih}	High level input voltage	0.6xVdd	-	-	V
V_{oh}	High level output voltage	0.6xVdd	-	-	V
V_{ol}	Low level output voltage	-	-	0.2xVdd	V
-	Input leakage current (AC-link inputs)	-10	-	10	μA
-	Output leakage current (Hi-Z AC-link outputs)	-10	-	10	μA
-	Output buffer drive current	-	5	-	mA

8. AC Timing Characteristics

8.1 Cold Reset time

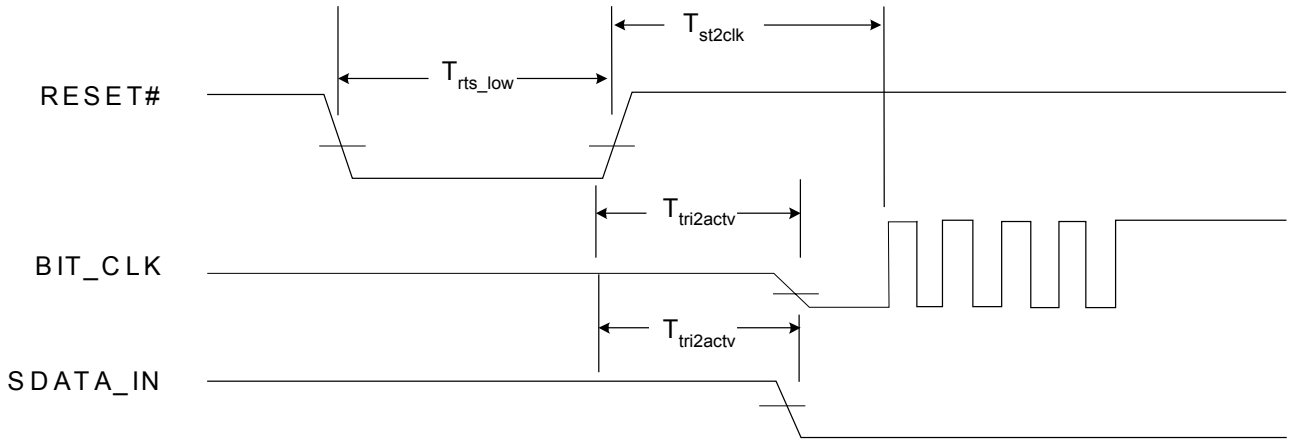


Figure 8-1. Cold Reset time Waveform

Table 8-1. Cold Reset time AC Table

Symbol	Parameter	Min	Typ	Max	Units
T_{rst_low}	RESET# active low pulse width	10	-	-	us
$T_{tri2actv}$	RESET# inactive to SDATA_IN or BIT_CLK active delay	-	-	25	ns
$T_{rst2clk}$	RESET# inactive to BIT_CLK startup delay	162.8	-	-	ns

8.2 Warm Reset time

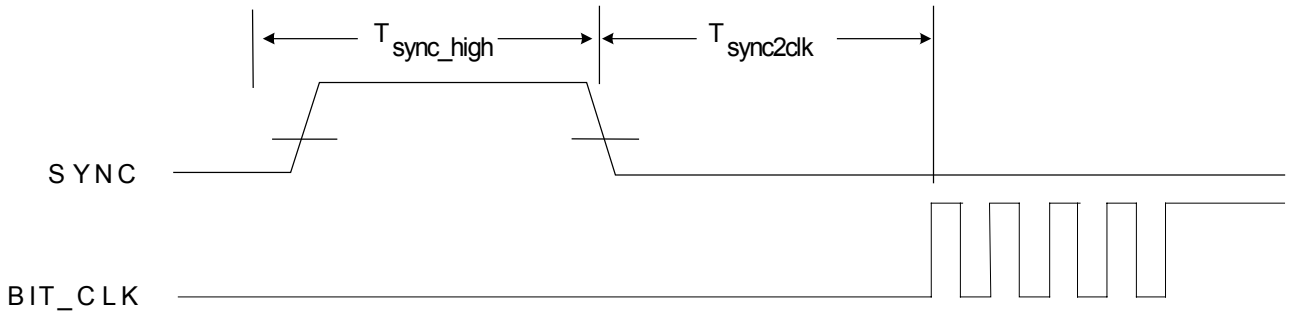


Figure 8-2. Warm Reset time Waveform

Table 8-2. Warm Reset time AC Table

Symbol	Parameter	Min	Typ	Max	Units
T_{sync_high}	SYNC active high pulse width	10	-	-	us
$T_{rst2clk}$	SYNC inactive to BIT_CLK startup delay	162.8	-	-	ns

8.3 AC_link Clocks

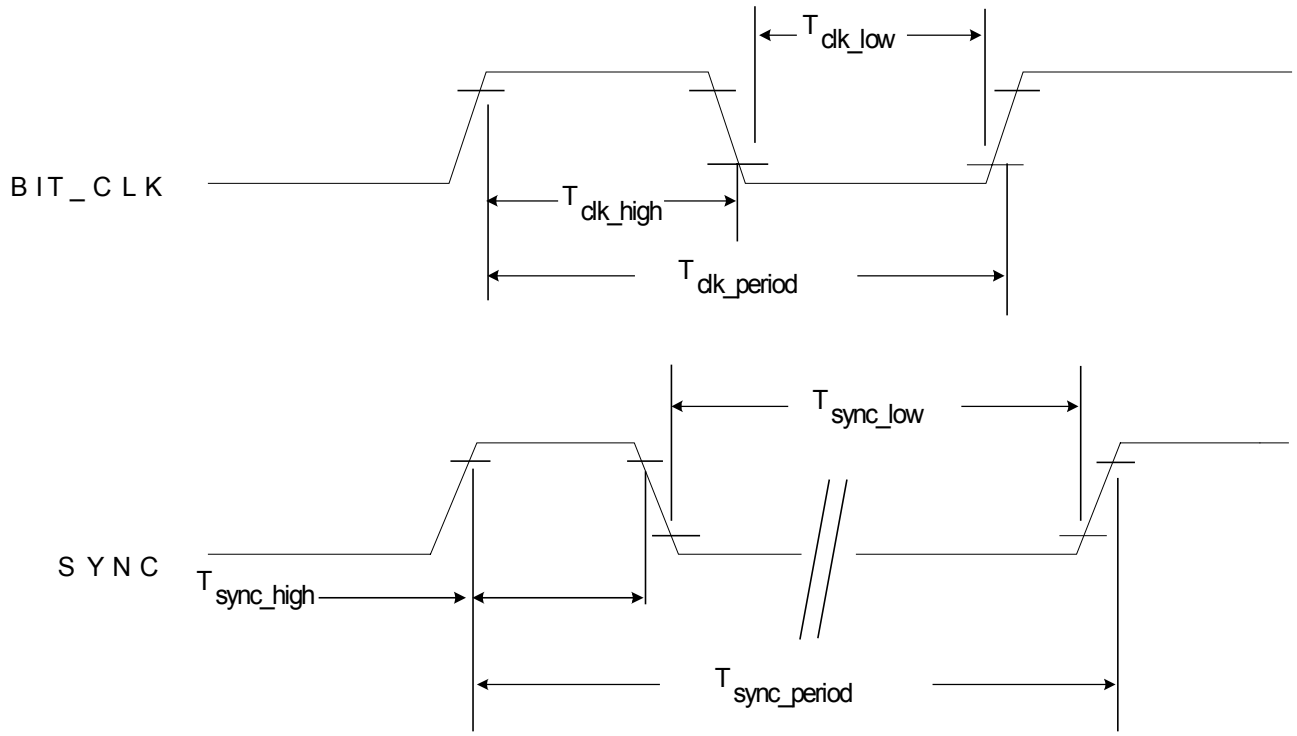


Figure 8-3. AC_link Clocks Waveform

Table 8-3. AC_link Clocks AC Table

Symbol	Parameter	Min	Typ	Max	Units
	BIT_CLK frequency	-	12.288	-	MHz
T_{clk_period}	BIT_CLK period	-	81.4	-	ns
	BIT_CLK output jitter	-	-	750	ps
T_{clk_high}	BIT_CLK high pulse width (note 2)	36	40.7	45	ns
T_{clk_low}	BIT_CLK low pulse width (note 2)	36	40.7	45	ns
	SYNC frequency	-	48	-	kHz
T_{sync_period}	SYNC period	-	20.8	-	us
T_{sync_high}	SYNC high pulse width	-	1.3	-	us
T_{sync_low}	SYNC low pulse width	-	19.5	-	us

Note 1: 47.5-75 pF
Note 2: The worst case duty cycle is restricted to 45/55.

8.4 Data Output and Input Times

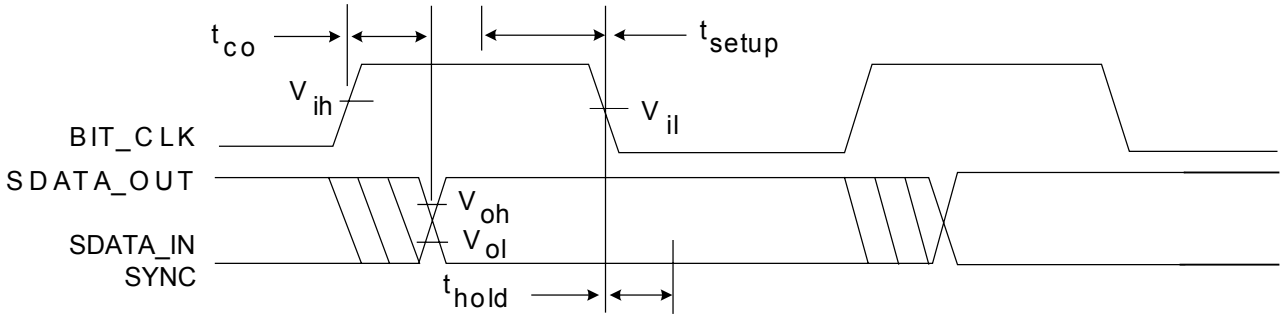


Figure 8-4. Data Output and Input Times Waveform

Table 8-4. Data Output and Input Times AC Table

Symbol	Parameter	Min	Typ	Max	Units
tco	Output Valid Delay from rising edge of BIT_CLK	-	-	15	ns
t_{setup}	Input Setup to falling edge of BIT_CLK	10	-	-	ns
t_{hold}	Input Hold from falling edge of BIT_CLK	10	-	-	ns

Note 1: 47.5-75 pF
Note 2: Combined rises or fall plus flight times are provided for the worst case scenario modeling purposes.

8.5 Signal Rise and Fall Times

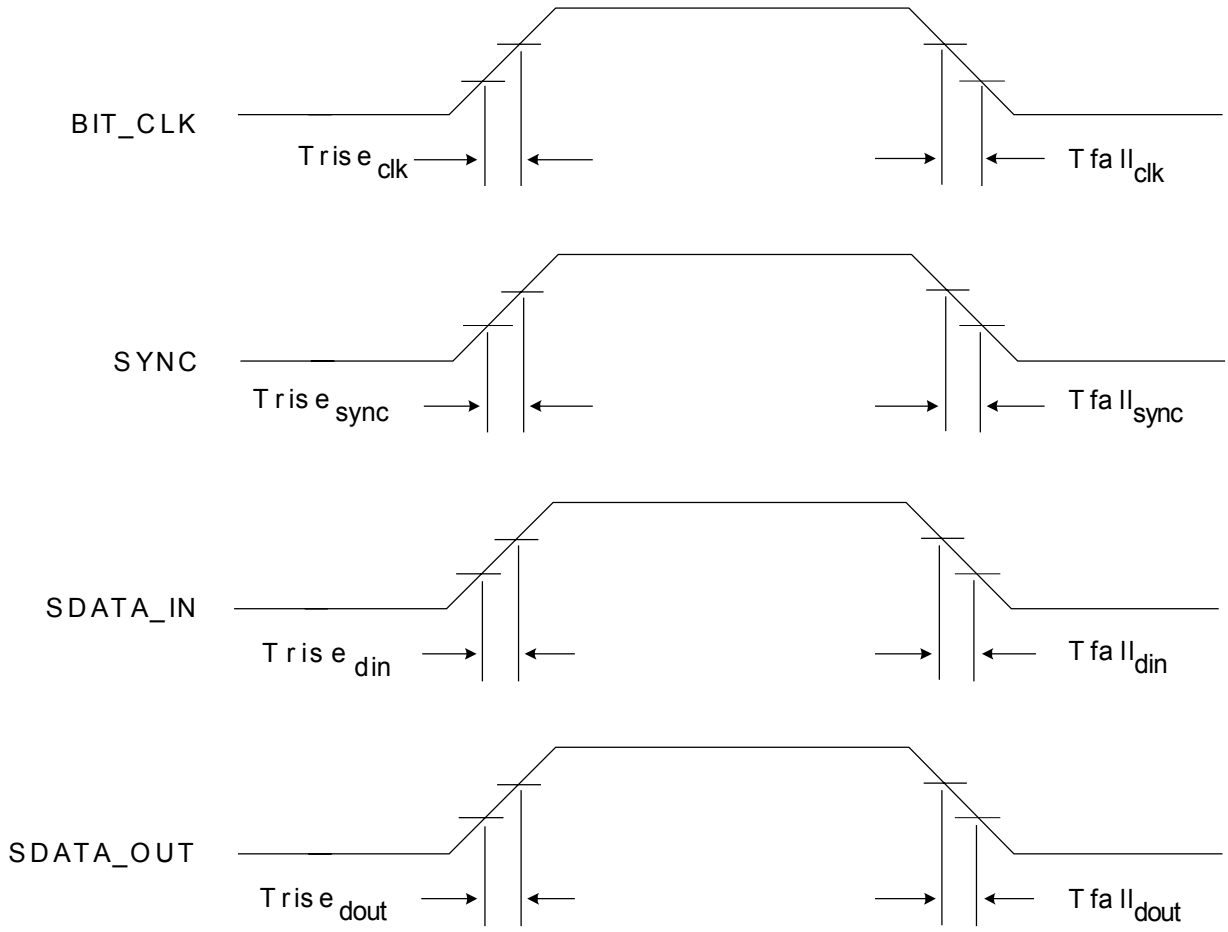


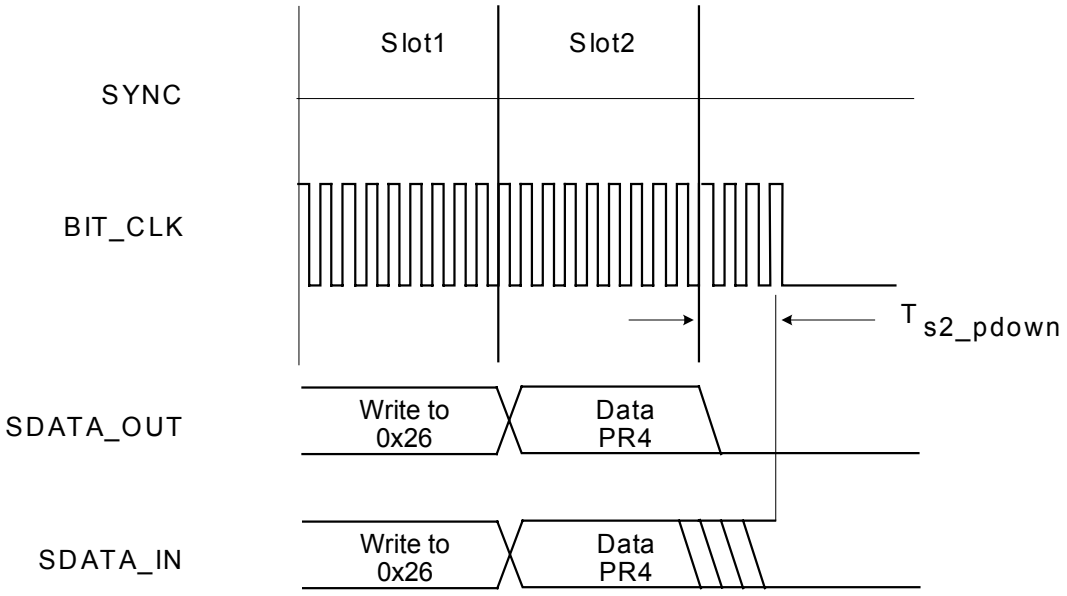
Figure 8-5 Signal Rise and Fall Times Waveform

Table 8-5. Signal Rise and Fall Times AC Table

Symbol	Parameter	Min	Typ	Max	Units
$Trise_{clk}$	BIT_CLK rise time (Note 1)	-	-	6	ns
$Tfall_{clk}$	BIT_CLK fall time (Note 1)	-	-	6	ns
$Trise_{sync}$	SYNC rise time (Note 2)	-	-	6	ns
$Tfall_{sync}$	SYNC fall time (Note 2)	-	-	6	ns
$Trise_{din}$	SDATA_IN rise time (Note 3)	-	-	6	ns
$Tfall_{din}$	SDATA_IN fall time (Note 3)	-	-	6	ns
$Trise_{dout}$	SDATA_OUT rise time (Note 2)	-	-	6	ns
$Tfall_{dout}$	SDATA_OUT fall time (Note 2)	-	-	6	ns

Note 1: BIT_CLK rise/fall times with an external load of 75 pF
Note 2: SYNC and SDATA_OUT rise/fall times with an external load of 75 pF
Note 3: SDATA_IN rise/fall times with an external load of 60 pF
Note 4: Rise is from 10% to 90% of Vdd (V_{ol} to V_{oh})
Note 5: Fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})

8.6 AC_link Low Power Mode Timing



Note:
BIT_CLK not to scale

Figure 8-6. AC_link Low Power Mode Timing Waveform

Table 8-6. AC_link Low Power Mode Timin AC Table

Symbol	Parameter	Min	Typ	Max	Units
T_{s2_pdown}	End of slot 2 to BIT_CLK, SDATA_IN low	-	-	1.0	us

8.7 ATE Test Mode

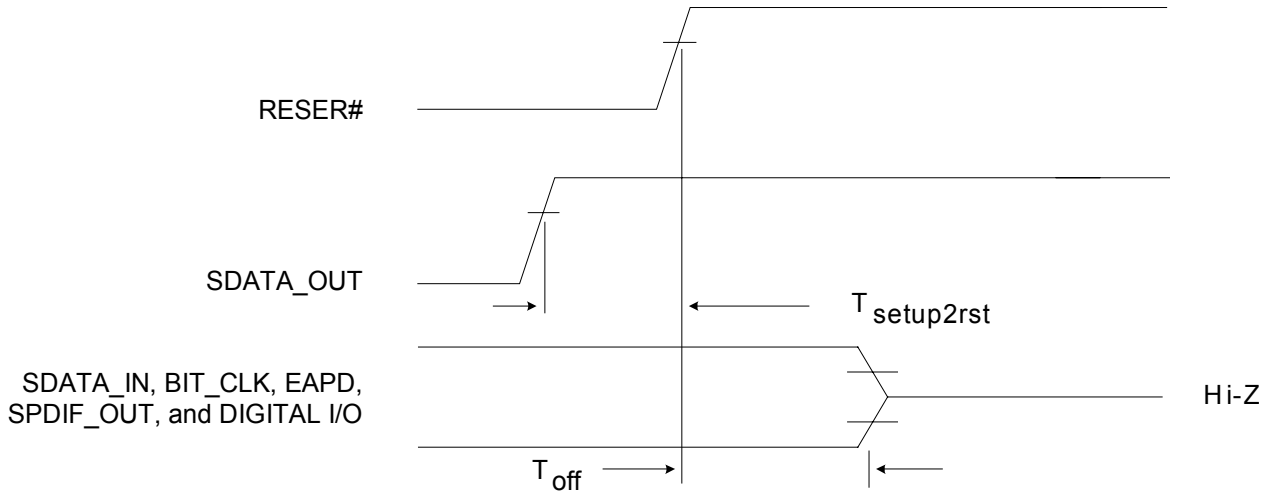


Figure 8-7. ATE Test Mode Waveform

Table 8-7. ATE Test Mode AC Table

Symbol	Parameter	Min	Typ	Max	Units
T_{s2_pdown}	Setup to trailing edge of RESET# (also applies to SYNC)	15.0	-	-	ns
T_{off}	Rising edge of RESET# to Hi-Z delay	-	-	25.0	ns

8.8 AC-link IO Pin Capacitance and Loading

Output Pin	1 Codec	2 Codecs	3 Codecs	4 Codecs
RESET, SYNC, & SDATA_OUT	47.5pF	62.5pF	75pF	85pF
BIT_CLK	47.5pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

9. Signal Performance

9.1 Digital Filter Characteristics

Parameter	Value	Unit
S/N ADC[1]	80 min. 85 tpy.	dB
S/N ADC[2]	85 min. 90 typ.	dB
Passband	20 – 19,200	Hz
Passband ripple	+/- 0.3	dB
Transition band	19,200 – 28,800	Hz
Stop band	28,800 – ∞	Hz
Stop band rejection	- 74	dB

Note 1: 1kHz, 0.95Vrms input, A-weighted
Note 2: 1kHz, A-weighted

9.2 Analog Characteristics

Parameter	Value	Unit
Full scale input voltage: Line inputs Mic inputs[1]	 1.0 typ. 0.1/1.0 typ.	V rms
Full scale output voltage: Line output	 1.0 typ.	V rms
Analog S/N: CD to LINE_OUT Other to LINE_OUT	 90 min. 95 typ 90 min. 95 typ	dB
Analog frequency response[2]	20 – 20,000	Hz
Total harmonic distortion: Line output[3]	-80 (0.01%) max for S_OUT/Center/LFE -74 (0.05%) max for Line Out with 32 ohm load -80 (0.1%) max for Line Out with 10K ohm load	dB
Out-of-band rejection[4]	- 60 typ.	dB
Group delay	1 max.	ms
Power supply rejection ratio	- 40 typ.	dB

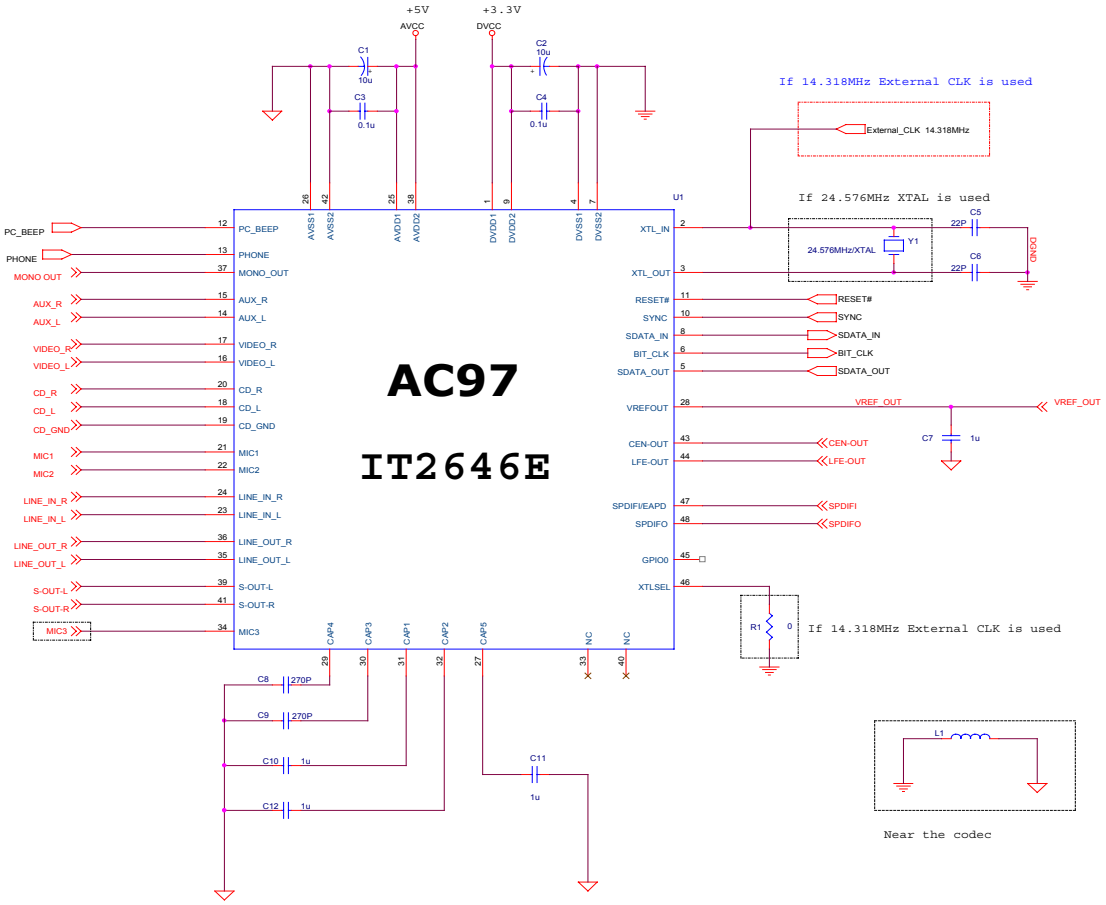
Analog Characteristics [cont'd]

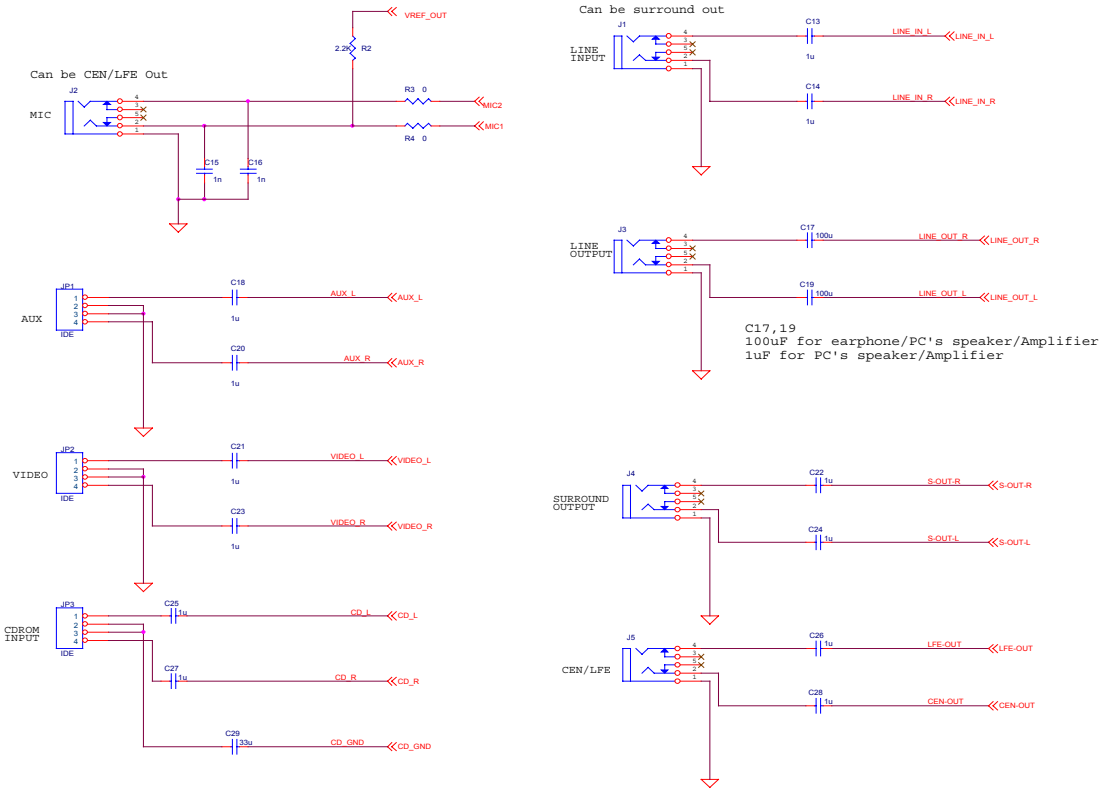
Parameter	Value	Unit
Crosstalk between input channels	- 70 max.	dB
Spurious tone reduction	- 100 typ.	dB
Attenuation & gain step size	1.5 typ.	dB
Input impedance	10 min.	kohm
Input capacitance	15 typ.	pF
Vrefout	2.25 – 2.75 typ.	V

Notes:

1. When +20 dB boosts on, Mic's full scale is 0.1Vrms and when +20dB boosts off, Mic's full scale is 1Vrms.
2. +/- 0.3 dB limits.
3. Full scale analog input, 20KHz baud width.
4. Integrated over 28.8 kHz to 100 kHz with respect to a 1V rms DAC output.

10. Application Circuit



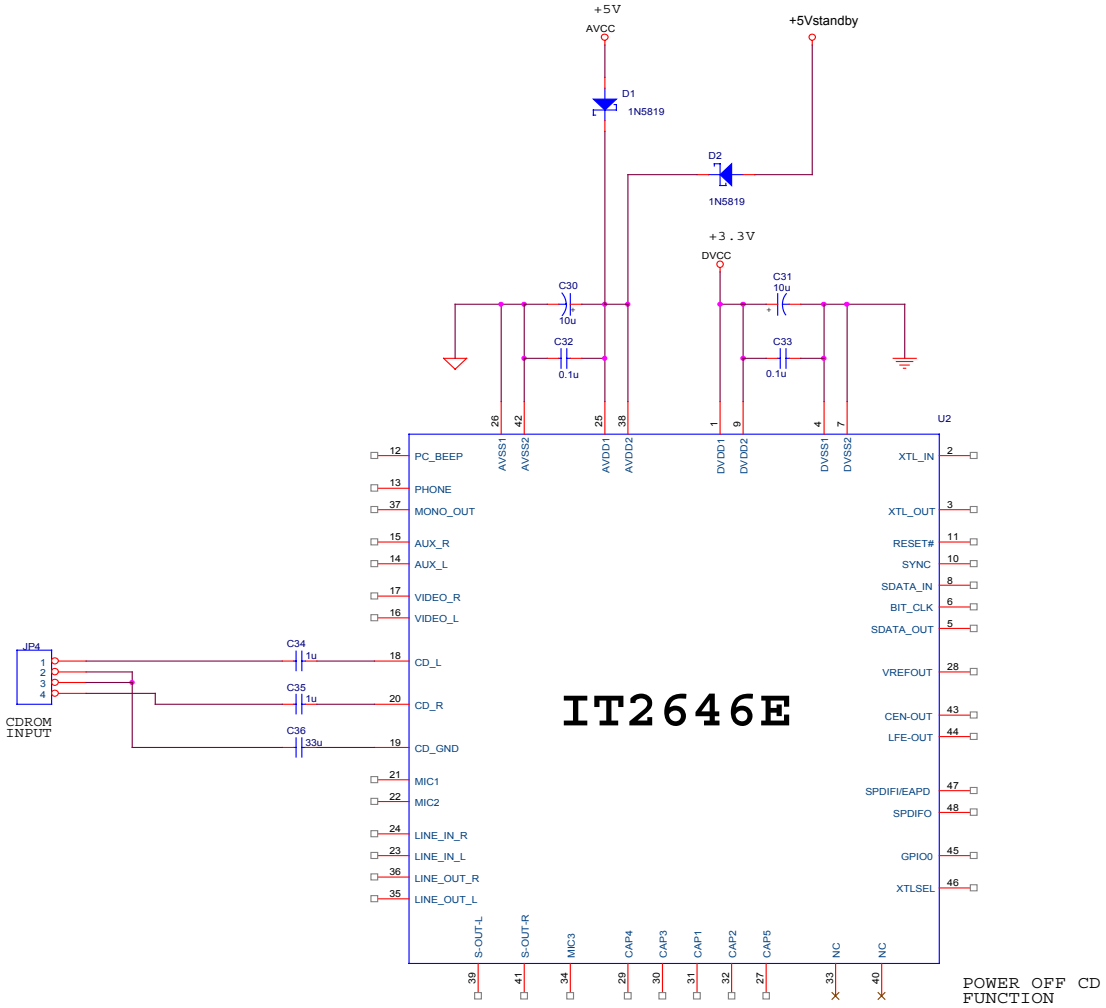

Can be CEN/LFE Out
MIC
J2
VREF_OUT
2.2K
R2
R3 0
R4 0
MIC2
MIC1
C15 1n
C16 1n
AUX
JP1
IDE
C18 1u
AUX_L
C20 1u
AUX_R
VIDEO
JP2
C21 1u
VIDEO_L
C23 1u
VIDEO_R
CDROM INPUT
JP3
C25 1u
CD_L
C27 1u
CD_R
C29 33u
CD_GND
Can be surround out
LINE INPUT
J1
C13 1u
LINE_IN_L
C14 1u
LINE_IN_R
LINE OUTPUT
J3
C17 100u
LINE_OUT_R
C19 100u
LINE_OUT_L
C17,19
100uF for earphone/PC's speaker/Amplifier
1uF for PC's speaker/Amplifier
SURROUND OUTPUT
J4
C22 1u
S-OUT-R
C24 1u
S-OUT-L
CEN/LFE
J5
C26 1u
LFE-OUT
C28 1u
CEN-OUT

Power Off CD function

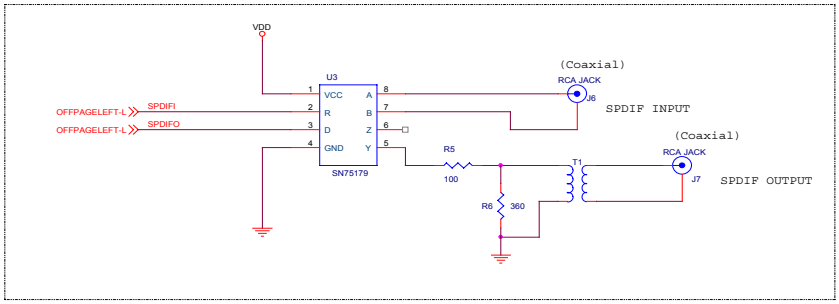
When “Power off CD” function is active, IT2646 will turn on CD inputs and front/surround outputs. Those volume control register will be at the default value.

The following table and schematics describe the system to support “Power off CD” function.

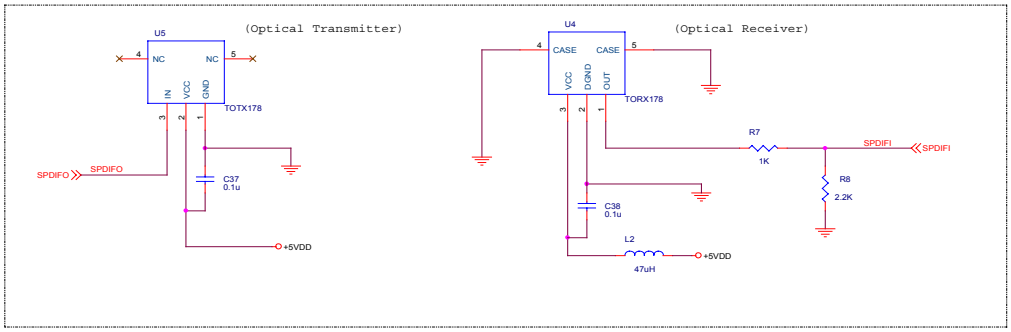
+5V	+5V standby	+3.3V	Function
OFF	OFF	OFF	No function
don’t care	ON	OFF	Power off CD
ON	don’t care	OFF	Power off CD
OFF	OFF	ON	Digital on, analog off
don’t care	ON	ON	Normal
ON	don’t care	ON	Normal



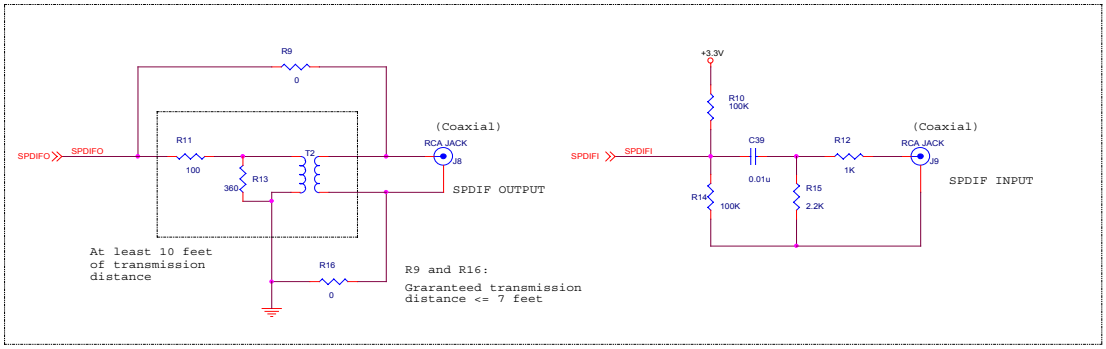
Option (I): S/PDIF signal use RCA connector + Line Driver/ Receiver (is suitable for long transmission line)



Option (II): S/PDIF signal use fiber optic tansmitter and receiver module

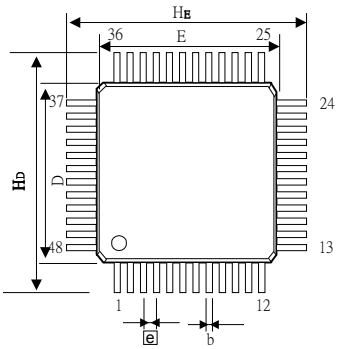


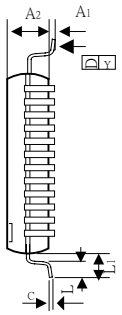
Option (III): Without Line Driver/ Receiver

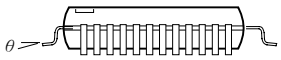


11. Package Information

48 Pin LQFP Outline Dimensions unit: inches/mm







Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	-	0.008	0.09	-	0.20
D	0.274	0.276	0.278	6.95	7.00	7.05
E	0.274	0.276	0.278	6.95	7.00	7.05
e	0.02BSC			0.50BSC		
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039REF			1.00REF		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D and E do not include mold protrusion.
2. Dimension b does not include dambar protrusion. Total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.

12. Ordering Information

Part No.	Package
IT2646	48LQFP