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IT8228E

Low Pin Count Media Interface (LPC Media I/F)

Preliminary Specification V0.2

INTEGRATED TECHNOLOGY EXPRESS, INC.

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Additional copies of this manual or other ITE literature may be obtained from:

ITE, Inc.
Marketing Department
8F, No. 233-1, Bao Chiao RD., Hsin Tien,
Taipei County 231, Taiwan, R.O.C.

Phone: (02) 29126889
Fax: (02) 2910-2551, 2910-2552

ITE (USA) Inc.
Marketing Department
1235 Midas Way
Sunnyvale, CA 94086
U.S.A.

Phone: (408) 530-8860
Fax: (408) 530-8861

ITE (USA) Inc.
Eastern U.S.A. Sales Office
896 Summit St., #105
Round Rock, TX 78664
U.S.A.

Phone: (512) 388-7880
Fax: (512) 388-3108

If you have any marketing or sales questions, please contact:

Lawrence Liu, at ITE Taiwan: E-mail: lawrence.liu@ite.com.tw, Tel: 886-2-26579896 X6071, Fax: 886-2-26578561
David Lin, at ITE U.S.A: E-mail: david.lin@iteusa.com, Tel: (408) 980-8168 X238, Fax: (408) 980-9232
Don Gardenhire, at ITE Eastern USA Office: E-mail: don.gardenhire@iteusa.com, Tel: (512) 388-7880, Fax: (512) 388-3108

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1. Features

- **Low Pin Count Interface**
  - Complies with Intel Low Pin Count Interface Specification Rev. 1.0
  - Supports LDRQ#, SERIRQ protocols

- **Memory Stick (MS) Interface**
  - Memory Stick V1.3 Specifications compliant
  - Up to 20MHz interface serial clock
  - Read speed 2.45MB/s
  - Supports DMA transmission
  - Supports interrupt polling transmission
  - Capacity 4MB~128MB
  - Supports up to 2 sets of MS I/F

- **Secure Digital (SD) Memory Card Interface**
  - Up to 25MHz interface serial clock
  - Forward compatibility to MultiMediaCard
  - Supports DMA transmission
  - 512byte data buffer
  - SD Memory/IO card Interface Supported
  - Supports up to 2 sets of SD I/F

- **SmartMedia™ Interface**
  - Supports voltage control circuit
  - Supports SmartMediaTM control circuit

- **Smart Card Reader**
  - Compliant with Personal Computer Smart Card (PC/SC) Working Group standard
  - Compliant with smart card (ISO 7816) protocols
  - Supports card present detect
  - Supports one programmable clock frequency, and 7.1 MHz and 3.5 MHz (Default) card clocks

- **35 General Purpose I/O Pins**
  - Supports Input and Output modes

- **Single 24/48 MHz Clock Input**

- **Single +3.3V Power Supply**

- **48-pin LQFP**

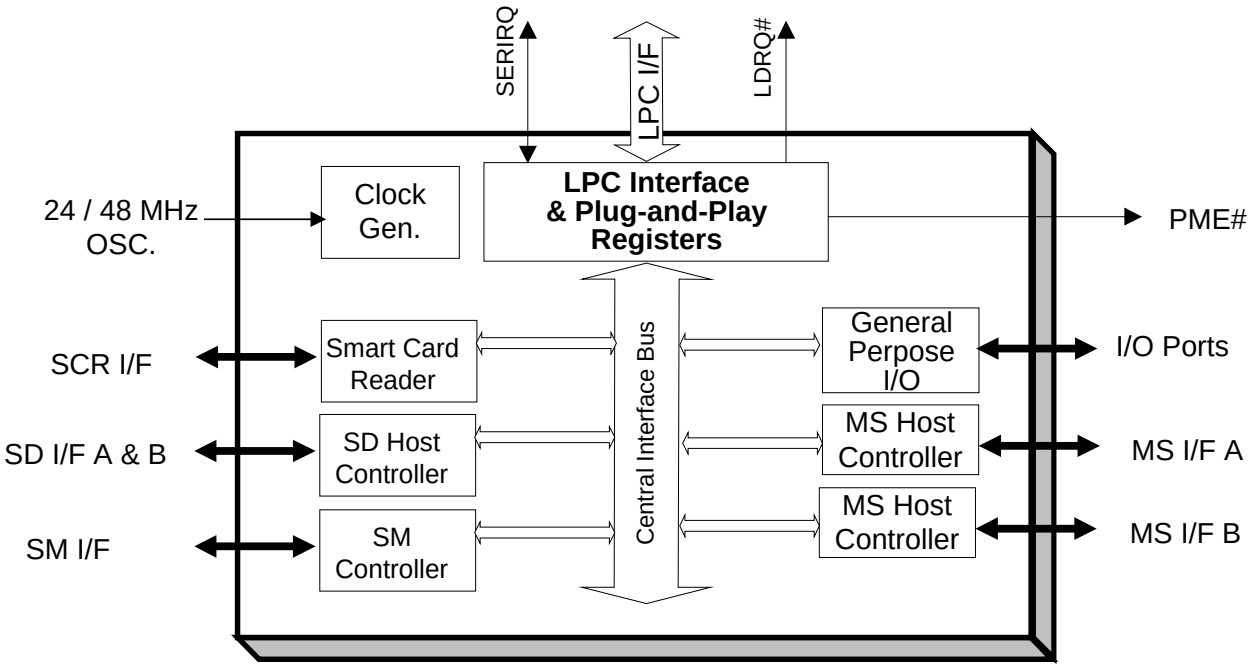
2. General Description

The IT8228E is a Low Pin Count Interface-based highly integrated media interface controller. The IT8228E provides the Smart Card Reader Interface, Memory Stick Interface and Secure Digital Interface. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.0".

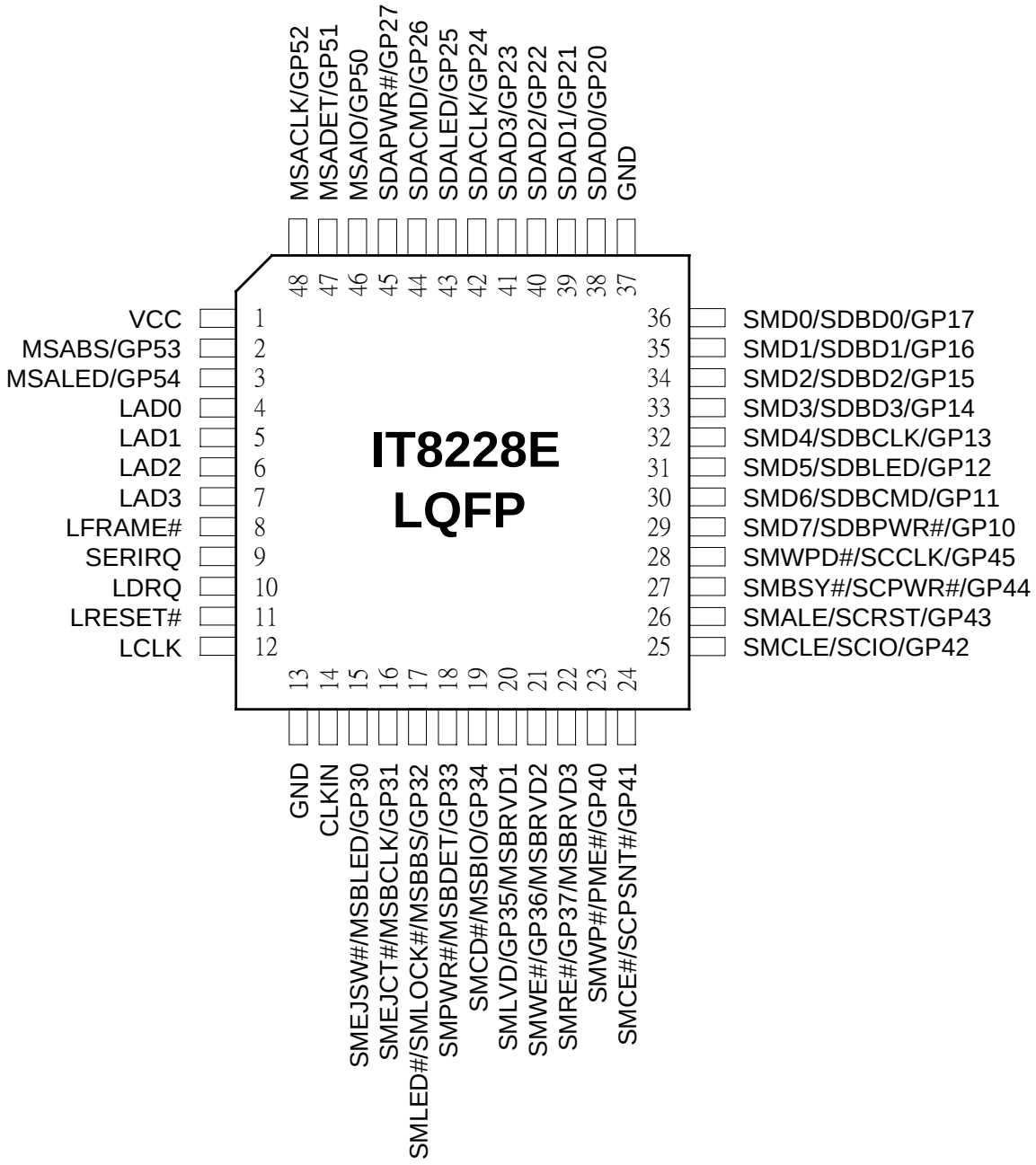
The Memory Stick Interface complies with Sony Memory Stick Standard Ver 1.3. It supports up to 20MHz clock and provides burst 2.45MB/s reading speed. The Secure Digital Interface complies with SD-Memory Card Specifications/Part1 Physical Layer Specification Ver. 1.0. It supports up to 24MHz. It also features a PC/SC and ISO 7816 compliant Smart Card Reader and a *SmartMedia™ Standard 2000* compliant SmartMedia™ I/F controller.

All the logical devices can be individually enabled or disabled via software configuration registers. The device requires a single 24/48 MHz clock input and operates with only single +3.3V power. In addition, all the pin buffers are powered by 3.3V with 5V tolerance. The IT8228E is available in 48-pin LQFP (Quad Flat Package).

3. Block Diagram



4. Pin Configuration



Top View

Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	13	GND	25	SMCLE/SCIO/ GP42	37	GND
2	MSABS/GP53	14	CLKIN	26	SMALE/SCRST/ GP43	38	SDAD0/GP20
3	MSALED/GP54	15	SMEJSW#/ MSBLED/GP30	27	SMBSY#/ SCPWR#/GP44	39	SDAD1/GP21
4	LAD0	16	SMEJCT#/ MSBCLK/GP31	28	SMWPD#/ SCCLK/GP45	40	SDAD2/GP22
5	LAD1	17	SMLED#/ SMLOCK#/ MSBBS/GP32	29	SMD7/SDBPWR# /GP10	41	SDAD3/GP23
6	LAD2	18	SMPWR#/ MSBDET/GP33	30	SMD6/SDBCMD/ GP11	42	SDACLK/GP24
7	LAD3	19	SMCD#/MSBIO/ GP34	31	SMD5/SDBLED/ GP12	43	SDALED/GP25
8	LFRAME#	20	SMLVD /GP35/MSBRVD1	32	SMD4/SDBCLK/ GP13	44	SDACMD/GP26
9	SERIRQ	21	SMWE#/ GP36/MSBRVD2	33	SMD3/SDBD3/ GP14	45	SDAPWR#/GP27
10	LDRQ	22	SMRE#/ GP37/MSBRVD3	34	SMD2/SDBD2/ GP15	46	MSAIO/GP50
11	LRESET#	23	SMWP#/PME#/ GP40	35	SMD1/SDBD1/ GP16	47	MSADET/GP51
12	LCLK	24	SMCE#/ SCPSNT#/GP41	36	SMD70/SDBD0/ GP17	48	MSACLK/GP52

5. IT8228E Pin Descriptions

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1	**VCC**	PWR	-	***+3.3V Power Supply.***
13, 37	**GNDD**	GND	-	***Digital Ground.***

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
4 – 7	**LAD[0:3]**	DIO8	VCC	***LPC Address/Data 0 - 3.*** 4-bit LPC address/bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
8	**LFRAME#**	DI	VCC	***LPC Frame #.*** This signal indicates the start of LPC cycle.
9	**SERIRQ**	DIO08	VCC	***Serial IRQ.***
10	**LDRQ#**	DO08	VCC	***LPC DMA Request #.*** An encoded signal for DMA channel select.
11	**LRESET#**	DI	VCC	***LPC RESET #.***
12	**LCLK**	DI	VCC	***LPC Clock.*** ***33 MHz PCI clock input for LPC I/F and SERIRQ.***

Table 5-3.Pin Description of Smart Media Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
15	**SMEJSW#/ MSBLED/ GP30**	DI/ DOD8/ DIOD8	VCC	***Smart Media Eject Input # / MS I/F B LED / General Purpose I/O 30.*** • The first function of this pin is Smart Media Eject Input #. • The second function of this pin is MS I/F B LED. • The third function of this pin is the General Purpose I/O Port 3 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
16	**SMEJCT#/ MSBCLK/ GP31**	DOD24/ DO24/ DIOD24	VCC	***Smart Media Eject Output # / MS I/F B Clock / General Purpose I/O 31.*** • The first function of this pin is Smart Media Eject Output #. • The second function of this pin is MS I/F B Clock. • The third function of this pin is the General Purpose I/O Port 3 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
17	**SMLED#/ SMLOCK#/ MSBBS/ GP32**	DOD24/ DO24/ DIOD24	VCC	***Smart Media LED # / Smart Media Locked # / MS I/F B Bus State / General Purpose I/O 32.*** • The first function of this pin is Smart Media Locked # or Smart Media LED #. • The second function of this pin is MS I/F B Bus State. • The third function of this pin is the General Purpose I/O Port 3 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Smart Media Interface Signals[cont'd]

Pin(s) No.	Symbol	Attribute	Power	Description
18	**SMPWR#/ MSBDET/ GP33**	DOD24/ DI/ DIOD24	VCC	***Smart Media Power On # / MS I/F B Insertion Detect / General Purpose I/O 33.*** • The first function of this pin is Smart Media Power On #. • The second function of this pin is MS I/F B Insertion Detect. • The third function of this pin is the General Purpose I/O Port 3 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
19	**SMCD#/ MSBIO/ GP34**	DI/ DIO08/ DIOD08	VCC	***Smart Media Card Detect # / MS I/F B Data I/O / General Purpose I/O 34.*** • The first function of this pin is Smart Media Card Detect #. • The second function of this pin is MS I/F B Data I/O. • The third function of this pin is the General Purpose I/O Port 3 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.
20	**SMLVD/ GP35/ MSBRVD1**	DI/ DIOD8/ --	VCC	***Smart Media Low Voltage Detect / General Purpose I/O 34 / MS I/F B Reserved 1.*** • The first function of this pin is Smart Media Low Voltage Detect. • The second function of this pin is the General Purpose I/O Port 3 Bit 4. • The third function of this pin is MS I/F B Reserved 1. • The function configuration of this pin is determined by programming the software configuration registers.
21	**SMWE#/ GP36/ MSBRVD2**	DO16/ DIOD16/ --	VCC	***Smart Media Write Enable # / General Purpose I/O 36 / MS I/F B Reserved 2.*** • The first function of this pin is Smart Media Write Enable #. • The second function of this pin is the General Purpose I/O Port 3 Bit 6. • The third function of this pin is MS I/F B Reserved 2. • The function configuration of this pin is determined by programming the software configuration registers.
22	**SMRE#/ GP37/ MSBRVD3**	DO16/ DIOD16/ --	VCC	***Smart Media Read Enable # / General Purpose I/O 37 / MS I/F B Reserved 3.*** • The first function of this pin is Smart Media Read Enable #. • The second function of this pin is the General Purpose I/O Port 3 Bit 7. • The third function of this pin is MS I/F B Reserved 3. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Smart Media Interface Signals [cont'd]

Pin(s) No.	Symbol	Attribute	Power	Description
23	**SMWP#/ PME#/ GP40**	DO16/ DOD16/ DIOD16	VCC	***Smart Media Write Protected # / Power Management Event # / General Purpose I/O 40.*** • The first function of this pin is Smart Media Write Protected #. • The second function of this pin is the power management event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state. • The third function of this pin is the General Purpose I/O Port 4 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
24	**SMCE#/ SCPSNT#/ GP41**	DO16/ DI/ DIOD16	VCC	***Smart Media Card Enable # / Smart Card Present Detect # / General Purpose I/O 41.*** • The first function of this pin is Smart Media Card Enable #. • The second function of this pin is Smart Card Reader Card Present Detect #. • The third function of this pin is the General Purpose I/O Port 4 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
25	**SMCLE/ SCIO/ GP42**	DO16/ DIOD16/ DIOD16	VCC	***Smart Media Command Latch Enable / Smart Card Data I/O / General Purpose I/O 42.*** • The first function of this pin is Smart Media Command Latch Enable. • The second function of this pin is Smart Card Reader Data I/O. • The third function of this pin is the General Purpose I/O Port 4 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
26	**SMALE/ SCRST/ GP43**	DO16/ DOD16/ DIOD16	VCC	***Smart Media Address Latch Enable / Smart Card Reset / General Purpose I/O 43.*** • The first function of this pin is Smart Media Address Latch Enable. • The second function of this pin is Smart Card Reader Reset. • The third function of this pin is the General Purpose I/O Port 4 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
27	**SMBSY#/ SCPWR#/ GP44**	DI/ DOD08/ DIOD08	VCC	***Smart Media Busy # / Smart Card Power FET Control # / General Purpose I/O 44.*** • The first function of this pin is Smart Media Busy #. • The second function of this pin is Smart Card Reader Power FET Control #. • The third function of this pin is the General Purpose I/O Port 4 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Smart Media Interface Signals [cont'd]

Pin(s) No.	Symbol	Attribute	Power	Description
28	**SMWPD#/ SCCLK/ GP45**	DI/ DOD08/ DIOD08	VCC	***Smart Media Write Protect Seal Detect # / Smart Card Clock / General Purpose I/O 45.*** • The first function of this pin is Smart Media Write Protect Seal Detect #. • The second function of this pin is Smart Card Reader Clock. • The third function of this pin is the General Purpose I/O Port 4 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
29	**SMD7/ SDBPWR#/ GP10**	DIO16/ DOD16/ DIOD16	VCC	***Smart Media Data 7 / SD I/F B Power FET Control # / General Purpose I/O 10.*** • The first function of this pin is Smart Media Data 7. • The second function of this pin is SD I/F B Power FET Control #. • The third function of this pin is the General Purpose I/O Port 1 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
30	**SMD6/ SDBCMD/ GP11**	DIO16/ DIO16/ DIOD16	VCC	***Smart Media Data 6 / SD I/F B Command / General Purpose I/O 11.*** • The first function of this pin is Smart Media Data 6. • The second function of this pin is SD I/F B Command. • The third function of this pin is the General Purpose I/O Port 1 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
31	**SMD5/ SDBLED/ GP12**	DIO16/ DO16/ DIOD16	VCC	***Smart Media Data 5 / SD I/F B LED / General Purpose I/O 12.*** • The first function of this pin is Smart Media Data 5. • The second function of this pin is SD I/F B LED. • The third function of this pin is the General Purpose I/O Port 1 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
32	**SMD4/ SDBCLK/ GP13**	DIO16/ DO16/ DIOD16	VCC	***Smart Media Data 4 / SD I/F B Clock / General Purpose I/O 13.*** • The first function of this pin is Smart Media Data 4. • The second function of this pin is SD I/F B Clock. • The third function of this pin is the General Purpose I/O Port 1 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
33	**SMD3/ SDBD3/ GP14**	DIO16/ DIO16/ DIOD16	VCC	***Smart Media Data 3 / SD I/F B Data 3 / General Purpose I/O 14.*** • The first function of this pin is Smart Media Data 3. • The second function of this pin is SD I/F B Data 3. • The third function of this pin is the General Purpose I/O Port 1 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of Smart Media Interface Signals [cont'd]

Pin(s) No.	Symbol	Attribute	Power	Description
34	**SMD2/ SDBD2/ GP15**	DIO16/ DIO16/ DIOD16	VCC	***Smart Media Data 2 / SD I/F B Data 2 / General Purpose I/O 15.*** • The first function of this pin is Smart Media Data 2. • The second function of this pin is SD I/F B Data 2. • The third function of this pin is the General Purpose I/O Port 1 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
35	**SMD1/ SDBD1/ GP16**	DIO16/ DIO16/ DIOD16	VCC	***Smart Media Data 1 / SD I/F B Data 1 / General Purpose I/O 16.*** • The first function of this pin is Smart Media Data 1. • The second function of this pin is SD I/F B Data 1. • The third function of this pin is the General Purpose I/O Port 1 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.
36	**SMD0/ SDBD0/ GP17**	DIO16/ DIO16/ DIOD16	VCC	***Smart Media Data 0 / SD I/F B Data 0 / General Purpose I/O 17.*** • The first function of this pin is Smart Media Data 0. • The second function of this pin is SD I/F B Data 0. • The third function of this pin is the General Purpose I/O Port 1 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-4. Pin Description of Secure Digital Interface A Signals

Pin(s) No.	Symbol	Attribute	Power	Description
38	**SDAD0/ GP20**	DIO08/ DIOD08	VCC	***SD I/F A Data 0 / General Purpose I/O 20.*** • The first function of this pin is SD I/F A Data 0. • The second function of this pin is the General Purpose I/O Port 2 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
39	**SDAD1/ GP21**	DIO08/ DIOD08	VCC	***SD I/F A Data 1 / General Purpose I/O 21.*** • The first function of this pin is SD I/F A Data 1. • The second function of this pin is the General Purpose I/O Port 2 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
40	**SDAD2/ GP22**	DIO08/ DIOD08	VCC	***SD I/F A Data 2 / General Purpose I/O 22.*** • The first function of this pin is SD I/F A Data 2. • The second function of this pin is the General Purpose I/O Port 2 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-4. Pin Description of Secure Digital Interface A Signals[cont'd]

Pin(s) No.	Symbol	Attribute	Power	Description
41	**SDAD3/ GP23**	DIO08/ DIOD08	VCC	***SD I/F A Data 3 / General Purpose I/O 23.*** • The first function of this pin is SD I/F A Data 3. • The second function of this pin is the General Purpose I/O Port 2 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
42	**SDACLK/ GP24**	DO08/ DIOD08	VCC	***SD I/F A Clock / General Purpose I/O 24.*** • The first function of this pin is SD I/F A Clock. • The second function of this pin is the General Purpose I/O Port 2 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.
43	**SDALED/ GP25**	DO08/ DIOD08	VCC	***SD I/F A LED / General Purpose I/O 25.*** • The first function of this pin is SD I/F A LED. • The second function of this pin is the General Purpose I/O Port 2 Bit 5. • The function configuration of this pin is determined by programming the software configuration registers.
44	**SDACMD/ GP26**	DO08/ DIOD08	VCC	***SD I/F A Command / General Purpose I/O 26.*** • The first function of this pin is SD I/F A Command. • The second function of this pin is the General Purpose I/O Port 2 Bit 6. • The function configuration of this pin is determined by programming the software configuration registers.
45	**SDAPWR#/ GP27**	DOD08/ DIOD08	VCC	***SD I/F A Power FET Control # / General Purpose I/O 27.*** • The first function of this pin is SD I/F A Power FET Control #. • The second function of this pin is the General Purpose I/O Port 2 Bit 7. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-5. Pin Description of Memory Stick Interface A Signals

Pin(s) No.	Symbol	Attribute	Power	Description
46	**MSAIO/ GP50**	DO08/ DIOD08	VCC	***MS I/F A Data I/O / General Purpose I/O 50.*** • The first function of this pin is MS I/F A Data I/O. • The second function of this pin is the General Purpose I/O Port 5 Bit 0. • The function configuration of this pin is determined by programming the software configuration registers.
47	**MSADET/ GP51**	DI/ DIOD08	VCC	***MS I/F A Insertion Detect / General Purpose I/O 51.*** • The first function of this pin is MS I/F A Insertion Detect. • The second function of this pin is the General Purpose I/O Port 5 Bit 1. • The function configuration of this pin is determined by programming the software configuration registers.
48	**MSACLK/ GP52**	DO08/ DIOD08	VCC	***MS I/F A Clock / General Purpose I/O 52.*** • The first function of this pin is MS I/F A Clock. • The second function of this pin is the General Purpose I/O Port 5 Bit 2. • The function configuration of this pin is determined by programming the software configuration registers.
2	**MSABS/ GP53**	DO08/ DIOD08	VCC	***MS I/F A Bus State / General Purpose I/O 53.*** • The first function of this pin is MS I/F A Bus State. • The second function of this pin is the General Purpose I/O Port 5 Bit 3. • The function configuration of this pin is determined by programming the software configuration registers.
3	**MSALED/ GP54**	DOD08/ DIOD08	VCC	***MS I/F A LED / General Purpose I/O 54.*** • The first function of this pin is MS I/F A LED. • The second function of this pin is the General Purpose I/O Port 5 Bit 4. • The function configuration of this pin is determined by programming the software configuration registers.

Table 5-6. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
14	**CLKIN**	DI	VCC	***24 or 48 MHz Clock Input.***

IO Cell:
DO8: 8mA Digital Output buffer
DOD8: 8mA Digital Open-Drain Output buffer
DO16: 16mA Digital Output buffer
DOD16: 16mA Digital Open-Drain Output buffer
DO24: 24mA shink/12mA Drive Digital Output buffer
DOD24: 24mA Digital Open-Drain Output buffer

DIO8: 8mA Digital Input/Output buffer
DIOD8: 8mA Digital Open-Drain Input/Output buffer
DIO16: 16mA Digital Input/Output buffer
DIOD16: 16mA Digital Open-Drain Input/Output buffer
DIOD24: 24mA Digital Open-Drain Input/Output buffer

DI: Digital Input

6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1 (Set 1)

Pin(s) No.	Symbol	Attribute	Description
29	SMD7/ SDBPWR#/ GP10	DIO16/ DOD16/ DIOD16	*Smart Media Data 7 / SD I/F B Power FET Control # / General Purpose I/O 10.*
30	SMD6/ SDBCMD/ GP11	DIO16/ DIOD16/ DIOD16	*Smart Media Data 6 / SD I/F B Command / General Purpose I/O 11.*
31	SMD5/ SDBLED/ GP12	DIO16/ DOD16/ DIOD16	*Smart Media Data 5 / SD I/F B LED / General Purpose I/O 12.*
32	SMD4/ SDBCLK/ GP13	DIO16/ DO16/ DIOD16	*Smart Media Data 4 / SD I/F B Clock / General Purpose I/O 13.*
33	SMD3/ SDBD3/ GP14	DIO16/ DIO16/ DIOD16	*Smart Media Data 3 / SD I/F B Data 3 / General Purpose I/O 14.*
34	SMD2/ SDBD2/ GP15	DIO16/ DIO16/ DIOD16	*Smart Media Data 2 / SD I/F B Data 2 / General Purpose I/O 15.*
35	SMD1/ SDBD1/ GP16	DIO16/ DIO16/ DIOD16	*Smart Media Data 1 / SD I/F B Data 1 / General Purpose I/O 16.*
36	SMD0/ SDBD0/ GP17	DIO16/ DIO16/ DIOD16	*Smart Media Data 0 / SD I/F B Data 0 / General Purpose I/O 17.*

Table 6-2. General Purpose I/O Group 2 (Set 2)

Pin(s) No.	Symbol	Attribute	Description
38	SDAD0/GP20	DIO16/ DIOD16	*SD I/F A Data 0 / General Purpose I/O 20.*
39	SDAD1/GP21	DIO16/ DIOD16	*SD I/F A Data 1 / General Purpose I/O 21.*
40	SDAD2/GP22	DIO16/ DIOD16	*SD I/F A Data 2 / General Purpose I/O 22.*
41	SDAD3/GP23	DIO16/ DIOD16	*SD I/F A Data 3 / General Purpose I/O 23.*
42	SDACLK/GP24	DO16/ DIOD16	*SD I/F A Clock / General Purpose I/O 24.*
43	SDALED/GP25	DOD16/ DIOD16	*SD I/F A LED / General Purpose I/O 25.*
44	SDACMD/ GP26	DIO16/ DIOD16	*SD I/F A Command / General Purpose I/O 26.*
45	SDAPWR#/ GP27	DOD16/ DIOD16	*SD I/F A Power FET Control # / General Purpose I/O 27.*

Table 6-3. General Purpose I/O Group 3 (Set 3)

Pin(s) No.	Symbol	Attribute	Description
15	**SMEJSW#/ MSBLED/ GP30**	DI/DOD8/ DIOD8	***Smart Media Eject Input # / MS I/F B LED / General Purpose I/O 30.***
16	**SMEJCT#/ MSBCLK/GP31**	DOD24/ DO24/ DIOD24	***Smart Media Eject Output # / MS I/F B Clock / General Purpose I/O 31.***
17	**SMLED#/ SMLOCK#/ MSBBS/GP32**	DOD24/ DO24/ DIOD24	***Smart Media LED # / Smart Media Locked # / MS I/F B Bus State / General Purpose I/O 32.***
18	**SMPWR#/ MSBDET/GP33**	DOD24/DI/ DIOD24	***Smart Media Power On # / MS I/F B Insertion Detect / General Purpose I/O 33.***
19	**SMCD#/ MSBIO/GP34**	DI/DIO16/ DIOD16	***Smart Media Card Detect # / MS I/F B Data I/O / General Purpose I/O 34.***
20	**SMLVD/GP35 / MSBRVD1**	DI/DIOD8/ --	***Smart Media Low Voltage Detect / General Purpose I/O 35 / MS I/F B Reserved 1.***
21	**SMWE#/GP36 / MSBRVD2**	DO16/ DIOD16/--	***Smart Media Write Enable # / General Purpose I/O 36 / MS I/F B Reserved 2.***
22	**SMRE#/GP37/ MSBRVD3**	DO16/ DIOD16/--	***Smart Media Read Enable # / General Purpose I/O 37 / MS I/F B Reserved 3.***

Table 6-4. General Purpose I/O Group 4 (Set 4)

Pin(s) No.	Symbol	Attribute	Description
23	**SMWP#/PME #/ GP40**	DO16/ DOD16/ DIOD16	***Smart Media Write Protected # / Power Management Event # / General Purpose I/O 40.***
24	**SMCE#/ SCPSNT#/ GP41**	DO16/ DI/DIOD16	***Smart Media Card Enable # / Smart Card Present Detect # / General Purpose I/O 41.***
25	**SMCLE/ SCIO/GP42**	DO16/ DIOD16/DIOD16	***Smart Media Command Latch Enable / Smart Card Data I/O / General Purpose I/O 42.***
26	**SMALE/ SCRST/ GP43**	DO16/ DOD16/ DIOD16	***Smart Media Address Latch Enable / Smart Card Reset / General Purpose I/O 43.***
27	**SMBSY#/ SCPWR#/GP44**	DI/DOD16/ DIOD16	***Smart Media Busy # / Smart Card Power FET Control # / General Purpose I/O 44.***
28	**SMWPD#/ SCCLK/GP45**	DI/DOD16/ DIOD16	***Smart Media Write Protect Seal Detect # / Smart Card Clock / General Purpose I/O 45.***

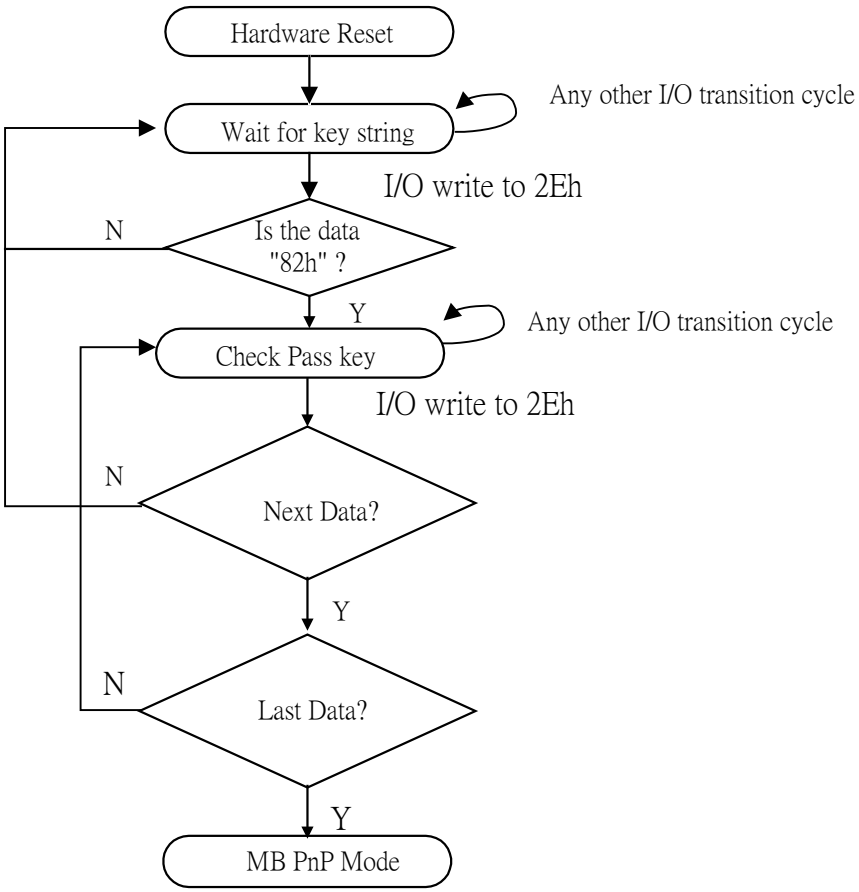
Table 6-5. General Purpose I/O Group 5 (Set 5)

Pin(s) No.	Symbol	Attribute	Description
46	**MSAIO/GP50**	DIO16/ DIOD16	***MS I/F A Data I/O / General Purpose I/O 50.***
47	**MSADET/GP51**	DI/DIOD16	***MS I/F A Insertion Detect / General Purpose I/O 51.***
48	**MSACLK/GP52**	DO16/ DIOD16	***MS I/F A Clock / General Purpose I/O 52.***
2	**MSABS/GP53**	DO16/ DIOD16	***MS I/F A Bus State / General Purpose I/O 53.***
3	**MSALED/GP54**	DOD16/ DIOD16	***MS I/F A LED / General Purpose I/O 54.***

7. Configuration

7.1 Configuring Sequence Description

After the hardware or power-on reset, the IT8228E enters the normal mode with all logical devices disabled.



There are three steps to completing the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are to be performed during the Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) of the next step.

		Address port	Data port
	82h, 28h, 55h, 55h;	2Eh	2Fh
or	82h, 28h, 55h, AAh;	4Eh	4Fh

(2) Modify the Data of the Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to "1" to exit the MB PnP Mode.

7.2 Description of the Configuration Registers

Table 7-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	**Configure Control**
All	07h	R/W	NA	**Logical Device Number (LDN)**
All	20h	R	82h	**Chip ID Byte 1**
All	21h	R	28h	**Chip ID Byte 2**
All	22h	R	00h	**Chip Version**
All	23h	R/W	00h	**Clock and GPIO Selection Register**
F4h	2Eh	R/W	00h	**Test 1 Register**
F4h	2Fh	R/W	00h	**Test 2 Register**

Table 7-2. Secure Digital Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
00h	30h	R/W	00h	**Secure Digital Controller Activate**
00h	60h	R/W	02h	**Secure Digital Controller Base Address MSB Register**
00h	61h	R/W	30h	**Secure Digital Controller Base Address LSB Register**
00h	70h	R/W	09h	**Secure Digital Controller Interrupt Level Select**
00h	74h	R/W	06h	**Secure Digital Controller DMA Channel Select**
00h	F0h	R/W	00h	**Secure Digital Controller Special Configuration Register**

Table 7-3. Smart Media Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	**Smart Media Controller Activate**
01h	60h	R/W	02h	**Smart Media Controller Base Address MSB Register**
01h	61h	R/W	60h	**Smart Media Controller Base Address LSB Register**
01h	70h	R/W	0Bh	**Smart Media Controller Interrupt Level Select**
01h	F0h	R/W	00h	**Smart Media Controller Special Configuration Register**

Table 7-4. Memory Stick Controller A Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
02h	30h	R/W	00h	**Memory Stick Controller A Activate**
02h	60h	R/W	02h	**Memory Stick Controller A Base Address MSB Register**
02h	61h	R/W	20h	**Memory Stick Controller A Base Address LSB Register**
02h	70h	R/W	05h	**Memory Stick Controller A Interrupt Level Select**
02h	74h	R/W	05h	**Memory Stick Controller A DMA Channel Select**
02h	F0h	R/W	02h	**Memory Stick Controller A Special Configuration Register**

Table 7-5. Memory Stick Controller B Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
03h	30h	R/W	00h	**Memory Stick Controller B Activate**
03h	60h	R/W	02h	**Memory Stick Controller B Base Address MSB Register**
03h	61h	R/W	28h	**Memory Stick Controller B Base Address LSB Register**
03h	70h	R/W	05h	**Memory Stick Controller B Interrupt Level Select**
03h	74h	R/W	07h	**Memory Stick Controller B DMA Channel Select**
03h	F0h	R/W	02h	**Memory Stick Controller B Special Configuration Register**

Table 7-6. Smart Card Reader Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	**Smart Card Reader Activate**
04h	60h	R/W	03h	**Smart Card Reader Base Address MSB Register**
04h	61h	R/W	38h	**Smart Card Reader Base Address LSB Register**
04h	70h	R/W	09h	**Smart Card Reader Interrupt Level Select**
04h	F0h	R/W	02h	**Smart Card Reader Special Configuration Register 1**
04h	F1h	R/W	7Fh	**Smart Card Reader Special Configuration Register 2**

Table 7-7. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
05h	60h	R/W	00h	**Interrupt Status Access Base Address MSB Register**
05h	61h	R/W	00h	**Interrupt Status Access Base Address LSB Register**
05h	B0h	R/W	00h	**GPIO Set 1 Pin Polarity Register**
05h	B1h	R/W	00h	**GPIO Set 2 Pin Polarity Register**
05h	B2h	R/W	00h	**GPIO Set 3 Pin Polarity Register**
05h	B3h	R/W	00h	**GPIO Set 4 Pin Polarity Register**
05h	B4h	R/W	00h	**GPIO Set 5 Pin Polarity Register**
05h	B8h	R/W	00h	**GPIO Set 1 Pin Internal Pull-up Enable Register**
05h	B9h	R/W	00h	**GPIO Set 2 Pin Internal Pull-up Enable Register**
05h	BAh	R/W	00h	**GPIO Set 3 Pin Internal Pull-up Enable Register**
05h	BBh	R/W	00h	**GPIO Set 4 Pin Internal Pull-up Enable Register**
05h	BCh	R/W	00h	**GPIO Set 5 Pin Internal Pull-up Enable Register**
05h	C8h	R/W	00h	**Simple I/O Set 1 Output Enable Register**

Table 7-8. GPIO Configuration Registers[cont'd]

LDN	Index	R/W	Reset	Configuration Register or Action
05h	C9h	R/W	00h	**Simple I/O Set 2 Output Enable Register**
05h	CAh	R/W	00h	**Simple I/O Set 3 Output Enable Register**
05h	CBh	R/W	00h	**Simple I/O Set 4 Output Enable Register**
05h	CCh	R/W	00h	**Simple I/O Set 5 Output Enable Register**
05h	F0h	R/W	00h	**Simple I/O Set 1 Data Register**
05h	F1h	R/W	00h	**Simple I/O Set 2 Data Register**
05h	F2h	R/W	00h	**Simple I/O Set 3 Data Register**
05h	F3h	R/W	00h	**Simple I/O Set 4 Data Register**
05h	F4h	R/W	00h	**Simple I/O Set 5 Data Register**
05h	F5h	R/W	00h	**SWC Status Register**
05h	F6h	R/W	00h	**SWC_STS to PME Enable Register**
05h	F7h	R/W	00h	**SWC_STS to SMI Enable Register**

7.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 7-9. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0	Base + (0 – 1)	SDC
LDN=1	Base + (0 – 7)	SMC
LDN=2	Base + (0 - 7)	MSCA
LDN=3	Base + (0 - 7)	MSCB
LDN=4	Base + (0 - 7)	SCR
LDN=5	Base + (0 - 1)	GPIO

7.3 Global Configuration Registers (LDN: All)

7.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	**Reserved**
1	**Returns to the "Wait for Key" state.** This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

7.3.2 Logical Device Number (LDN, Index=07h)

This register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices. This register is **read/write**.

7.3.3 Chip ID Byte 1 (Index=20h, Default=82h)

This register is the Chip ID Byte 1 and is **read only**. Bits [7:0]=82h when read.

7.3.4 Chip ID Byte 2 (Index=21h, Default=28h)

This register is the Chip ID Byte 2 and is **read only**. Bits [7:0]=28h when read.

7.3.5 Chip Version (Index=22h, Default=00h)

This register is the Chip Version and is **read only**.

7.3.6 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**PME_EN (Power Management Event output enable)** This bit enables PME# (pin 23) function when SMC is disabled. 0: disabled (default). 1: enabled.
3	**Reserved**
2	**PIN20_22_SEL (Pin 20, 21, and 22 Multi-function Selection)** This bit selects the priority of pin 20, 21 and 22. 0: the priority are Pin 20: SMLVD, GP35, and MSBRVD1 Pin 21: SMWE#, GP36, and MSBRVD2 Pin 22: SMRE#, GP37, and MSBRVD3 (default). 1: the priority are Pin 20: SMLVD, GP35, and MSBRVD1 Pin 21: SMWE#, MSBRVD2, and GP36 Pin 22: SMRE#, MSBRVD3, and GP37.
1	**SD_CLK_SEL (SD block Clock source Select)** This bit selects the clock frequency for the SD controller block. 0: 48Mhz (default). 1: 33Mhz (LCLK).
0	**CLKIN_FREQ (CLKIN Frequency)** This bit determines the frequency of CLKIN pin. 0: 48 MHz (default). 1: 24 MHz.

7.3.7 Test 1 Register (Index=2Eh, Default=00h)

This register is the Test 1 Register and is reserved for ITE. It should not be set.

7.3.8 Test 2 Register (Index=2Fh, Default=00h)

This register is the Test 2 Register and is reserved for ITE. It should not be set.

7.4 Secure Digital Controller Configuration Registers (LDN=00h)

7.4.1 Secure Digital Controller Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**SDC_EN (Secure Digital Controller Activation)** 0: Disabled (default). 1: Secure Digital Controller enabled.

7.4.2 Secure Digital Controller Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only**, with "0h" for Base Addresses [15:12].
3-0	Mapped as Base Addresses [11:8].

7.4.3 Secure Digital Controller Base Address LSB Register (Index=61h, Default=30h)

Bit	Description
7-1	**Read/write** mapped as Base Addresses [7:1].
0	**Read only** as "0b."

7.4.4 Secure Digital Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for SDC.

7.4.5 Secure Digital Controller DMA Channel Select (Index=74h, Default=06h)

Bit	Description
7-3	Reserved with default "00h."
2-0	Select the DMA channel [Note2] for SDC.

7.4.6 Secure Digital Controller Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-3	Reserved with default "00h".
2	**Port_1_Enable.** Enable SD Port 1 (pin port group B). 1: Enable. 0: Disable.
1	**Port_0_Enable.** Enable SD Port 0 (pin port group A). 1: Enable. 0: Disable.
0	**SDC_IRQ_SHR (SDC Interrupt Request Sharing).** 0: Normal (default). 1: Enable SDC IRQ sharing.

7.5 Smart Media Controller Configuration Registers (LDN=01h)

7.5.1 Smart Media Controller Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**SMC_EN (Smart Media Activation)** 0: Disabled (default). 1: Smart Media Controller enabled.

7.5.2 Smart Media Controller Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only**, with "0h" for Base Addresses [15:12].
3-0	Mapped as Base Addresses [11:8].

7.5.3 Smart Media Controller Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-3	**Read/write** mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

7.5.4 Smart Media Controller Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for SMC.

7.5.5 Smart Media Controller Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-2	Reserved with default "00h".
1	**SMLOCK_SMLED.** Smart Media I/F function selection of Pin 17. 1: SMLED. 0: SMLOCK#.
0	**SMC_IRQ_SHR (SMC Interrupt Request Sharing).** 0: Normal (default). 1: Enable SMC IRQ sharing.

7.6 Memory Stick Controller A Configuration Registers (LDN=02h)

7.6.1 Memory Stick Controller A Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**MSCA_EN (Memory Stick Controller A Activation)** 0: Disabled (default). 1: Memory Stick Controller A enabled.

7.6.2 Memory Stick Controller A Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only**, with "0h" for Base Addresses [15:12].
3-0	Mapped as Base Addresses [11:8].

7.6.3 Memory Stick Controller A Base Address LSB Register (Index=61h, Default=20h)

Bit	Description
7-3	**Read/write** mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

7.6.4 Memory Stick Controller A Interrupt Level Select (Index=70h, Default=05h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for MSCA.

7.6.5 Memory Stick Controller A DMA Channel Select (Index=74h, Default=05h)

Bit	Description
7-3	Reserved with default "00h."
2-0	Select the DMA channel [Note2] for MSCA.

7.6.6 Memory Stick Controller A Special Configuration Register 1 (Index=F0h, Default=02h)

Bit	Description
7-1	Reserved with default "00h".
0	**MSCA_IRQ_SHR (MSCA Interrupt Request Sharing).** 0: Normal (default). 1: Enable MSCA IRQ sharing.

7.7 Memory Stick Controller B Configuration Registers (LDN=03h)

7.7.1 Memory Stick Controller B Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**MSCB_EN (Memory Stick Controller B Activation)** 0: Disabled (default). 1: Memory Stick Controller B enabled.

7.7.2 Memory Stick Controller B Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only**, with "0h" for Base Addresses [15:12].
3-0	Mapped as Base Addresses [11:8].

7.7.3 Memory Stick Controller B Base Address LSB Register (Index=61h, Default=28h)

Bit	Description
7-3	**Read/write** mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

7.7.4 Memory Stick Controller B Interrupt Level Select (Index=70h, Default=05h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for MSCB.

7.7.5 Memory Stick Controller B DMA Channel Select (Index=74h, Default=07h)

Bit	Description
7-3	Reserved with default "00h."
2-0	Select the DMA channel [Note2] for MSCB.

7.7.6 Memory Stick Controller B Special Configuration Register 1 (Index=F0h, Default=02h)

Bit	Description
7-1	Reserved with default "00h".
0	**MSCB_IRQ_SHR (MSCB Interrupt Request Sharing).** 0: Normal (default). 1: Enable MSCB IRQ sharing.

7.8 Smart Card Reader Configuration Registers (LDN=04h)

7.8.1 Smart Card Reader Activate (Index=30h, Default=00h)

Bit	Description
7-1	**Reserved**
0	**SCR_EN (Smart Card Reader Activation)** 0: Disabled (default). 1: Smart Card Reader enabled.

7.8.2 Smart Card Reader Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only**, with "0h" for Base Addresses [15:12].
3-0	Mapped as Base Addresses [11:8].

7.8.3 Smart Card Reader Base Address LSB Register (Index=61h, Default=38h)

Bit	Description
7-3	**Read/write** mapped as Base Addresses [7:3].
2-0	**Read only** as "000b."

7.8.4 Smart Card Reader Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [Note1] for SCR.

7.8.5 Smart Card Reader Special Configuration Register 1 (Index=F0h, Default=02h)

Bit	Description
7	**COM_PNP_EN** 0: Disable COM Port device Plug-and-Play operation (default). 1: Enable COM Port device Plug-and-Play operation.
6-5	**Reserved**
4	**PNP_ID** This bit is only available when bit 7=1 0: PNP_ID Access mode (default). 1: Normal Plug-and-Play operation mode.
3	**SCR_IRQ_SHR (SCR Interrupt Request Sharing).** 0: Normal (default). 1: Enable SCR IRQ sharing.
2	**SCPWR_POR (SCPWR Polarity)** 0: Active low (default). 1: Active high.
1-0	**SCCLK_SEL1-0 (SCCLK Frequency Selection)** 00: Stop (default) 01: 3.5 MHz 10: 7.1 MHz 11: Special Frequency (96 MHz/SCDIV)

7.8.6 Smart Card Reader Special Configuration Register 2 (Index=F1h, Default=7Fh)

Bit	Description
7	**SCPRES_POR (SCPRES# Polarity)** 0: Active low (default). 1: Active high.
6-0	**SCDIV6-0 (SCCLK Special Divisor).**

7.9 GPIO Configuration Registers (LDN=05h)

7.9.1 Interrupt Status Access Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**Read/write** mapped as Base Address [11:8].

7.9.2 Interrupt Status Access Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-0	**Read/write** mapped as Base Address [7:0].

7.9.3 GPIO Pin Set 1, 2, 3, 4 and 5 Polarity Registers (Index=B0h, B1h, B2h, B3h and B4h, Default=00h)

Bit	Description
7-0	**PIN_POR7-0 (Pin Polarity)** These bits program the GPIO pins' polarity. 0: Non-inverting (default). 1: Inverting.

7.9.4 GPIO Pin Set 1, 2, 3, 4 and 5 Pin Internal Pull-up Enable Registers (Index=B8h, B9h, BAh, BBh and BCh, Default=00h)

Bit	Description
7-0	**PIN_PU7-0 (Pin Pull-up)** These bits are used to enable the GPIO pin internal pull-up. 0: No Pull-up (default). 1: With pull-up resistor.

7.9.5 Simple I/O Set 1, 2, 3, 4 and 5 Output Enable Registers (Index=C8h, C9h, CAh, CBh and CCh, Default=00h)

Bit	Description
7-0	**SMIO_DIR7-0 (Simple I/O Direction Select)** These bits determine the directions of the Simple I/O pins. 0: Input (default). 1: Output.

7.9.6 Simple I/O Set 1, 2, 3, 4, 5, and 6 Data Registers (Index=F0h, F1h, F2h, F3h, and F4h, Default=00h)

Bit	Description
7-0	**SMIO_D7-0 (Simple I/O Data)** These are the data registers of the GPIO pins. When the GPIO pin is set as input mode, the register is read-only and reflects the state of the pin. When the GPIO pin is set as output mode, the register can be read/written and controls the state of the GPIO pin.

7.9.7 SWC Status Register (SWC_STS) (Index=F5h, Default =--)

Bit	Description
7-5	**Reserved**
4	**SCR_IRQ_STS (Smart Card Reader IRQ Event Status)** This bit indicates that an IRQ was generated by the Smart Card Reader module. This bit is set only if the Smart Card Reader module is active. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive since last cleared (default). 1: An enabled IRQ, from the Smart Card Reader module.
3	**MSCB_IRQ_STS (Memory Stick Controller B IRQ Event Status)** This bit indicates that an IRQ was generated by the Memory Stick Controller B module. This bit is set only if the Memory Stick Controller B module is active. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive since last cleared (default). 1: An enabled IRQ, from the Memory Stick Controller B module.
2	**MSCA_IRQ_STS (Memory Stick Controller A IRQ Event Status)** This bit indicates that an IRQ was generated by the Memory Stick Controller A module. This bit is set only if the Memory Stick Controller A module is active. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive since last cleared (default). 1: An enabled IRQ, from the Memory Stick Controller A module.
1	**SMC_IRQ_STS (Smart Media Controller IRQ Event Status)** This bit indicates that an IRQ was generated by the Smart Media Controller module. This bit is set only if the Smart Media Controller module is active. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive since last cleared (default). 1: An enabled IRQ, from the Smart Media Controller module.
0	**SDC_IRQ_STS (SDC IRQ Event Status)** This bit indicates that an IRQ was generated by the Secure Digital Controller module. This bit is set only if the SDC module is active. Writing “1” will clear this bit; writing “0” will be ignored. 0: Inactive since last cleared (default). 1: An enabled IRQ, from the SDC module.

7.9.8 SWC_STS to PME Enable Register (Index=F6h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**SWC_STS4_2PME** Enable the activation of the PME by an active event of SCR_IRQ_STS. 0: Disabled (default). 1: Enabled.
3	**SWC_STS3_2PME** Enable the activation of the PME by an active event of MSCB_IRQ_STS. 0: Disabled (default). 1: Enabled.
2	**SWC_STS2_2PME** Enable the activation of the PME by an active event of MSCA_IRQ_STS. 0: Disabled (default). 1: Enabled.
1	**SWC_STS1_2PME** Enable the activation of the PME by an active event of SMC_IRQ_STS. 0: Disabled (default). 1: Enabled.
0	**SWC_STS0_2PME** Enable the activation of the PME by an active event of SDC_IRQ_STS. 0: Disabled (default). 1: Enabled.

7.9.9 SWC_STS to SMI Enable Register (Index=F7h, Default=00h)

Bit	Description
7-5	**Reserved**
4	**SWC_STS4_2SMI** Enable the activation of the SMI by an active event of SCR_IRQ_STS. 0: Disabled (default). 1: Enabled.
3	**SWC_STS3_2SMI** Enable the activation of the SMI by an active event of MSCB_IRQ_STS. 0: Disabled (default). 1: Enabled.
2	**SWC_STS2_2SMI** Enable the activation of the SMI by an active event of MSCA_IRQ_STS. 0: Disabled (default). 1: Enabled.
1	**SWC_STS1_2SMI** Enable the activation of the SMI by an active event of SMC_IRQ_STS. 0: Disabled (default). 1: Enabled.
0	**SWC_STS0_2SMI** Enable the activation of the SMI by an active event of SDC_IRQ_STS. 0: Disabled (default). 1: Enabled.

Note 1: Interrupt level mapping

Fh-Dh: not valid
Ch: IRQ12
.
.
3h: IRQ3
2h: not valid
1h: IRQ1
0h: no interrupt selected

Note 2: DMA channel mapping

7h: DMA7
6h: DMA6
5h: DMA5
4h: no DMA channel selected
3h: DMA3
2h: DMA2
1h: DMA1
0h: DMA0

8. Functional Description

8.1 LPC Interface

The IT8228E supports the peripheral site of the LPC I/F as described in the LPC Interface Specification Rev.1.0 (Sept. 29, 1997). In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK, which is the same as PCICLK.), the IT8228E also supports LDRQ#, SERIRQ and PME#.

8.1.1 LPC Transactions

The IT8228E supports some parts of the cycle types described in the LPC I/F specification. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Media Interface module processes a positive decoding and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will make reactions according to the DMA requests from the DMA devices in the Media Interface modules and decide whether to ignore the current transaction or not.

8.1.2 LDRQ# Encoding

The Media Interface module provides two DMA devices: the MS and the SD. The LPC Interface provides LDRQ# encoding to reflect the DREQ [3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to trace DMA requests quickly. But, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there is at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and send those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

8.2 Serialized IRQ

The IT8228E follows the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature and is able to interface most PC chipsets. The IT8228E encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

8.2.1 Continuous Mode

When in the continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the Turn-around State of current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events although no IRQn status is changed. The SERIRQ enter the continuous mode following a system reset.

8.2.2 Quiet Mode

In the Quiet mode, when one SIRQ Slave detects that its input IRQn/events have been changed, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence. In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity = low mode power consumption.

8.2.3 Waveform Samples of SERIRQ Sequence

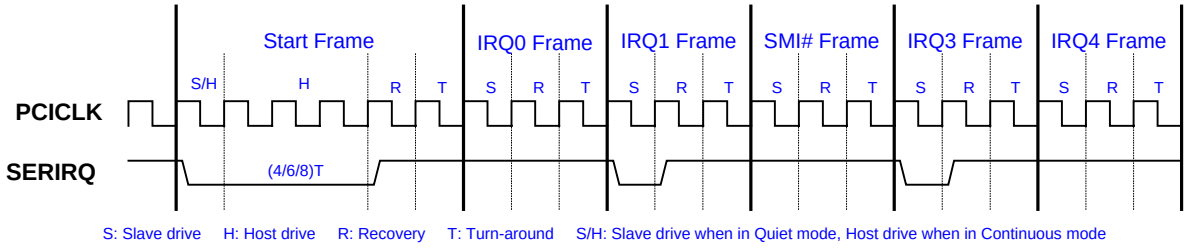


Figure 8-1. Start Frame Timing

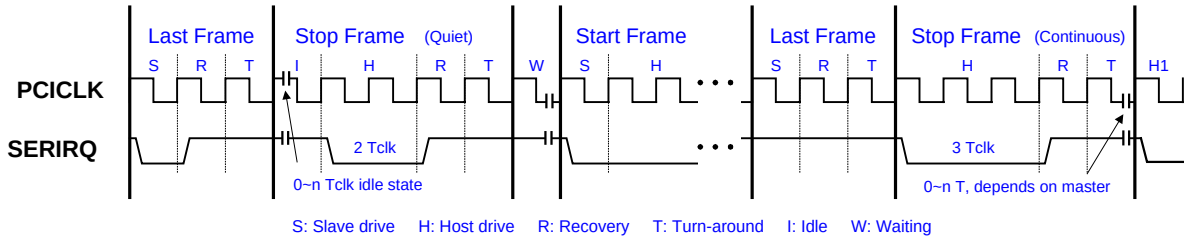


Figure 8-2. Stop Frame Timing

8.2.4 SERIRQ Sampling Slot

Slot Number	IRQn / Events	# of Clocks Past Start	IT8228E
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95 / 65	-

8.3 General Purpose I/O

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into five registers. The accessed I/O registers are the Simple I/O Data Registers (LDN=05h, Index=F0h, F1h, F2h, F3h and F4h).

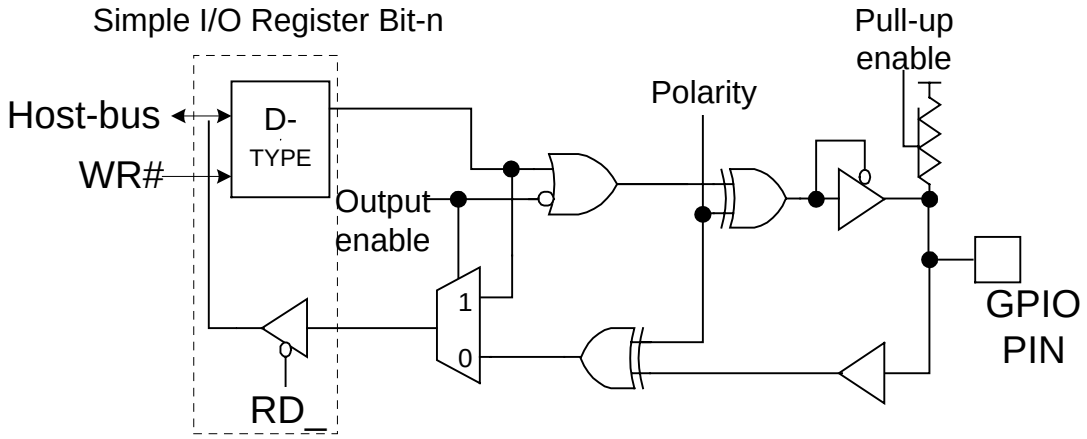


Figure 8-3. General Logic of GPIO Function

8.4 Power Management Event (PME#)

IT8228E implements a PME# used for transparent power management. The output consists of the enabled interrupts from each of the functional blocks in the chip. The interrupts are enabled onto the PME# output via the SWC_STS to PME Enable Register.

8.5 SD Host Controller (SDC)

8.5.1 Overview

The SD (Secure Digital) Host Controller provides the interface between a host processor (LPC interface) and SD I/F. On SD I/F side, it offers four serial data lines, a serial command line and synchronous clock. Both SD memory card and I/O card Interfaces are supported.

8.5.2 Features

- Built-in CRC circuit: CRC7 for commands and CRC16 for Data
- SD Memory/IO Card/MMC Interface supported: COMMAND (1line) and Data/INT/Card Detect (4 lines)
- 512-byte FIFO buffers
- DMA supported
- Interrupt polling transmission supported
- The transfer data length can be set up to either 2^9 bytes or 1 byte.
- Sector counter for multiple Read/Write operation

8.5.3 Register Descriptions

Table 8-1. SD Host Controller Access Port

Address	R/W	Default	Name
Base + 0h	R/W	00h	SD Host Controller Access Index Port
Base + 1h	R/W	--	SD Host Controller Access Data Port

Table 8-2. SD Host Controller Register

Index	R/W	Default	Name
00h	R/W	00h	SD_CMD
01h	R/W	00h	SD_CMD_MD
02h	R/W	00h	SD_PORTSEL
04h	R/W	00h	SD_ARG1
05h	R/W	00h	SD_ARG2
06h	R/W	00h	SD_ARG3
07h	R/W	00h	SD_ARG4
08h	R/W	00h	SD STOP
09h	R/W	00h	SD_SEC_EN
0Ah	R/W	00h	SD_SECCNTL
0Bh	R/W	00h	SD_SECCNTH

Table 8-2. SD Host Controller Register[cont'd]

Index	R/W	Default	Name
0Ch	R	--	SD_RSP0
0Dh	R	--	SD_RSP1
0Eh	R	--	SD_RSP2
0Fh	R	--	SD_RSP3
10h	R	--	SD_RSP4
11h	R	--	SD_RSP5
12h	R	--	SD_RSP6
13h	R	--	SD_RSP7
14h	R	--	SD_RSP8
15h	R	--	SD_RSP9
16h	R	--	SD_RSP10
17h	R	--	SD_RSP11
18h	R	--	SD_RSP12
19h	R	--	SD_RSP13
1Ah	R	--	SD_RSP14
1Bh	R	--	SD_RSP15
1Ch	R/W-R	00h	SD_INFOL
1Dh	R/W-R	00h	SD_INFOH
1Eh	R/W-R	00h	SD_BUFSTS
1Fh	R/W-R	00h	SD_ERR
20h	R/W	1Dh	SD_INFOL_MASK
21h	R/W	03h	SD_INFOH_MASK
22h	R/W	7Fh	SD_BUFSTS _MASK
23h	R/W	83h	SD_ERR _MASK
24h	R/W	20h	SD_CLK_CTRLL
25h	R/W	00h	SD_CLK_CTRLH
26h	R/W	00h	SD_SIZEL
27h	R/W	02h	SD_SIZEH
28h	R/W	EEh	SD_OPTION1
29h	R/W	00h	SD_OPTION2
2Ch	R/W	00h	SD_CMD_END_ERR_STS
2Dh	R/W	20h	SD_CRC_ERR_STS
2Eh	R/W	00h	SD_TIMEOUT_ERR_STS
30h	R/W	00h	SD_BUFL
31h	R/W	00h	SD_BUFH
34h	R/W	00h	SDIO_MODE

SD Host Controller Register[cont'd]

Index	R/W	Default	Name
36h	R/W	00h	SDIO_INFOL
37h	R/W	00h	SDIO_INFOH
38h	R/W	01h	SDIO_INFOL_MASK
39h	R/W	00h	SDIO_INFOH_MASK
6Ch	R/W	00h	DMA_EN
E0h	R/W	00h	SOFT_RST
E2h	R/W	04h	VERSION
F2h	R/W	00h	Power Control
F4h	R/W	00h	EXT_SDIO
F5h	R/W	07h	EXT_SDIO_MASK
F6h	R	--	EXT_WP
FAh	R/W-R	--	EXT_CD_DAT3
FEh	R/W	FFh	EXT_CD_DAT3_MASK

8.5.3.1 SD Command Register (SD_CMD)

The SD Command, an 8-bit **read/write** register, is the data size [7:0] for Command parameter.
For example:

CMD6 is corresponding to 8'b00_000110.
CMD18 is corresponding to 8'b00_010010.
ACMD13 is corresponding to 8'b01_001101.

Index: 00h

Bit	R/W	Default	Description
7 – 6	R/W	00b	**Command Type (CT[1:0])** 00b: CMD of SD Memory Card/MultiMediaCard 01b: ACMD followed by CMD55 of SD Memory Card 10b: Command for Mutual Authentication 11b: Reserved
5 – 0	R/W	00h	**Command Format (CF[45:40])** Correspond to bit position of Command Format [45:40] (command index).

8.5.3.2 SD Command Mode Register (SD_CMD_MD)

The SD Command Mode, an 8-bit **read/write** register, is the data size [7:0] for Command Mode selection.

Index: 01h

Bit	R/W	Default	Description
7 – 6	R/W	00b	**Command mode** 00b: Normal command (CMD12 is auto transfer) 01b: SDIO command (Host < - > Card) (CMD12 not auto transfer) 10b: Reserved 11b: Reserved SDIO command is only used by extended commands. CMD12 auto transfer means that it will stop transmission by sector count.
5	R/W	0b	**Multiple block transfer eanble** This bit is used to select single/Multiple block transfer (effective only in case of with data). 0: Single Block Transfer. 1: Multiple Block Transfer.
4	R/W	0b	**Write/Read mdoe** This bit is used to select Write/Read transfer (effective only in case of with data). 0: Write (Host → SD Card). 1: Read (Host ← SD Card).
3	R/W	1b	**Data mode enable** 0: Without Data. 1: With Data.
2 – 0	R/W	0b	**Extend command mode and Response type select** **Code Command mode Response** 000b: Normal mode Decoded command 001b: Extended command Reserved 010b: Extended command Reserved 011b: Extended command No response 100b: Extended command R1, R6, R5 101b: Extended command R1b 110b: Extended command R2 111b: Extended command R3, R4 A controller will not reflect bits 7-3 value on mode (000b). If software selected normal mode (000b), the controller automatically decides response type and transfer mode (data mode, write/read mode and single/multiple block) for command index. If software selected extended mode (011b to 111b), software must set an appropriate value in bits 7-3 for command index. Controller decides CMD7 and CMD12 with R1b response in normal mode (000b). If you don't want to use any response for CMD7 or CMD12, you need to set extended command.

8.5.3.3 SD Port Selection Register (SD_PORTSEL)

The SD Port Selection, an 8-bit **read/write** register, selects one of the appropriate SD Memory Cards.

Index: 02h

Bit	R/W	Default	Description
7 – 2	-	-	**Reserved for ITE use.**
1 – 0	R/W	00b	**Port Select** 00: Select Port 0 01: Select Port 1 10: Reserved 11: Reserved

8.5.3.4 SD Command Argument Register (SD_ARG4, SD_ARG3, SD_ARG2, and SD_ARG1)

The SD Command Argument, four **read/write** registers, are corresponded to bit position of Command Format [39:8] (argument).

Index: 04h (SD_ARG1)

Bit	R/W	Default	Description
7 – 0	R/W	00b	**Command Format [15:8] (CF[15:8])**

Index: 05h (SD_ARG2)

Bit	R/W	Default	Description
7 – 0	R/W	00b	**Command Format [23:16] (CF[23:16])**

Index: 06h (SD_AR3)

Bit	R/W	Default	Description
7 – 0	R/W	00b	**Command Format [31:24] (CF[31:24])**

Index: 07h (SD_ARG4)

Bit	R/W	Default	Description
7 – 0	R/W	00b	**Command Format [39:32] (CF[39:32])**

8.5.3.5 Data Stop Register (SD_STOP)

The Data Stop, an 8-bit read/write register, is used to stop the transfer.

Index: 08h

Bit	R/W	Default	Description
7 – 1	R/W	00h	**Reserved for ITE use.**
0	R/W	0h	**STOP** Set 1 to this bit to transfer CMD12 and the transmission state of the controller will be aborted. Set 0 to this bit just before CMD17, CMD18, CMD24, CMD25, CMD27, CMD30, CMD42, CMD56, ACMD43-48, ACMD18, or ACMD25 are set.

8.5.3.6 Transfer Sector Counter Enable Register (SD_SEC_EN)

The Transfer Sector Counter Enable, an 8-bit **read/write** register, is used to enable Transfer Sector Counter.

Index: 09h

Bit	R/W	Default	Description
7 – 1	R/W	00h	**Reserved for ITE use.**
0	R/W	0h	**SECEN** Set 1 to this bit to Transfer Sector Counter. Set 0 to this bit to disable. It is recommended to use the sector counter function in CMD18 and CMD25. This function will transmit CMD12 automatically.

8.5.3.7 Transfer Sector Count Register (SD_SECCNTL and SD_SECCNTH)

The Transfer Sector Count, a 16-bit **read/write** register (two bytes), is used to determine transfer sector count. This register is enabled when SECEN of SD_SEC_EN register is set to "1". The size of transfer unit has to be 512 bytes (one sector). If set 0001h to CNT [15:0], the transfer sector count is 1. If set FFFFh to CNT [15:0], the transfer sector count is 65535. If set 0000h to CNT [15:0] to CNT [15:0], the transfer sector count is 65536. Hardware performs decrement of this counter internally for transfer multiple sector data. Finally, when all data are sent out or received, hardware will send STOP_TRANSMISSION to SD Memory Card automatically.

Index: 0Ah (SD_SECCNTL)

Bit	R/W	Default	Description
7 – 0	R/W	00b	**Count [7:0] (CNT[7:0])**

Index: 0Bh (SD_SECCNTH)

Bit	R/W	Default	Description
7 – 0	R/W	00b	**Count [15:8] (CNT[15:8])**

8.5.3.8 SD Memory Card Response Register (SD_RSP0 – SD_RSP14)

The SD Memory Card Response, 15 **read only** registers, indicate SD Memory Card response value. R2 only indicates bit position 127:8 because CRC is calculated by hardware.
Response meaning and registers:

Response type	Meaning of Response	Registers
R1, R1b (normal response)	Card Status	RSP [39:8]
R2 (CID, CSD registers)	CID or CSD registers	RSP [127:8]
R3 (OCR register)	OCR register	RSP [39:8]
[R4 (Fast I/O)	RCA, reg addr, read reg content	RSP [39:8]]
[R5 (Interrupt)	RCA [31:16], [15:0] are not defined	RSP [39:8]]
R6 (Published RCA response)	New published RCA [31:16] etc.	RSP [39:8]

Index: 0Ch (SD_RSP0)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [15:8] (RSP[15:8])**

Index: 0Dh (SD_ RSP1)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [23:16] (RSP[23:16])**

Index: 0Eh (SD_RSP2)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [31:24] (RSP[31:24])**

Index: 0Fh (SD_ RSP3)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [39:32] (RSP[39:32])**

Index: 10h (SD_RSP4)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [47:40] (RSP[47:40])**

Index: 11h (SD_ RSP5)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [55:48] (RSP[55:48])**

Index: 12h (SD_RSP6)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [63:56] (RSP[63:56])**

Index: 13h (SD_ RSP7)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [71:64] (RSP[71:64])**

Index: 14h (SD_RSP8)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [79:72] (RSP[79:72])**

Index: 15h (SD_ RSP9)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [87:80] (RSP[87:80])**

Index: 16h (SD_RSP10)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [95:88] (RSP[95:88])**

Index: 17h (SD_ RSP11)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [103:96] (RSP[103:96])**

Index: 18h (SD_RSP12)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [111:104] (RSP[111:104])**

Index: 19h (SD_ RSP13)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [119:112] (RSP[119:112])**

Index: 1Ah (SD_RSP14)

Bit	R/W	Default	Description
7 – 0	R	--	**Response [127:110] (RSP[127:110])**

8.5.3.9 SD Memory Card Information Register (SD_INFOL and SD_INFOH)

The SD Memory Card Information, a 16-bit **read/write or read only** register, responds some cards' status of the PORT0.

Index: 1Ch (SD_INFOL)

Bit	R/W	Default	Description
7	R	--	**Write Protect** 0: Normal. 1: Write Protect for Port 0.
6 – 3	--	--	**Reserved for ITE use.**
2	R/W	0b	**Write/Read Access all End** Writing "0" to this bit will clear it. 0: No data response end occurs from the last clear. 1: Data response ~~is~~ ends.
1	--	--	**Reserved for ITE use.**
0	R/W	0b	**Response End** Writing "0" to this bit will clear it. 0: No command response end occurs from the last clear. 1: Command response ~~is~~ ends.

Index: 1Dh (SD_INFOH)

Bit	R/W	Default	Description
7 – 3	--	--	**Reserved for ITE use.**
2	R	--	**SDA_D3 Card Detect** When there is no data transfer, SDA_D3 is used as card detection. 0: SDA_D3 is low. 1: SDA_D3 is high.
1	R/W	0b	**SDA_D3 Card Inserted** Writing "0" to this bit will clear it. During four-bit data transfer, this status should be ignored. 0: No Card insertion detected from the last clear. 1: Card insertion detected.
0	R/W	0b	**SDA_D3 Card Removed** Writing "0" to this bit will clear it. During four-bit data transfer, this status should be ignored. 0: No Card removal detected from the last clear. 1: Card Writing detected.

8.5.3.10 SD Memory Card Buffer Status Register (SD_BUFSTS)

The SD Memory Card Buffer Status, an 8-bit **read/write or read only** register, responds command status.
Index: 1Eh

Bit	R/W	Default	Description
7	R/W	0b	**Illegal Access Error (ILA)** Writing "0" to this bit will clear it. 0: Normal from last clear. 1: Illegal accessing error. There are 3 cases: Case 1:Even if transaction is active, host writes SD_CMD register. Case 2:Software sets SD_CMD_MD[2:0]=3'b011 (no response) and SD_CMD_MD[3]=1'b1 (with data). Case 3:Software sets SD_CMD_MD[3]=1'b1 (with data) when SD_CMD=8'b00001100 (CMD12) is set.
6	R	0b	**Command Busy (CBSY)** 0: Command transaction finished. 1: During command transaction.
5 – 2	--	0h	**Reserved for ITE use.**
1	R/W	0b	**Write Enable (BWE)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: Write buffer to SD Memory Card is empty. (The size is specified by SD_SIZE)
0	R/W	0b	**Read Enable (BRE)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: Write buffer to SD Memory Card is empty. (The size is specified by SD_SIZE)

8.5.3.11 SD Memory Card Error Register (SD_ERR)

The SD Memory Card Error, an 8-bit **read/write or read only** register, responds error messages. About Erase command, if Timeout error (ERR3) occurs but no Response timeout error (ERR6), Software can know the end of Erase Command by polling the DAT0 (SDA_D0 or SDB_D0) as high.
Index: 1Fh

Bit	R/W	Default	Description
7	R	--	**DAT0 (SDA_D0 or SDB_D0) of the selected port** This bit responses DAT0 of the selected port (by SD_PORTSEL). 0: DAT0 of the selected port is "0". 1: DAT0 of the selected port is "1".
6	R/W	0b	**Response Timeout (ERR6)** Writing "0" to this bit will clear it. 0: Normal from last clear. 1: Response timeout occurs. There are two cases: Case 1: No command responds more than 640 SDCLK cycles. Case 2: No SD_STOP responds more than 640 SDCLK cycles.
5	R/W	0b	**Illegal Read Access (ERR5)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: Even if buffer is empty, the host still reads from it.

[cont'd]

Bit	R/W	Default	Description
4	R/W	0b	**Illegal Write Access (ERR4)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: If data read/write command state is not asserted, the host still writes to buffer.
3	R/W	0b	**Timeout (except response time out) (ERR3)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: Timeout occurs (except response timeout). There are five cases: Case 1: Keep busy (DAT0=0) more than N cycles after R1b response. Case 2: Keep busy (DAT0=0) more than N cycles after Write CRC Status. Case 3: No writes CRC Status more than N cycles after Write cycle. Case 4: No Read Data more than N cycles after Read Command. Case 5: Keep busy more than N cycles after SD_STOP. N is determined by SD_OPTION register bits 7-4.
2	R/W	0b	**End Error (ERR2)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: End error occurs. There are four cases: Case 1: END bit error in Command response (Illegal response length). Case 2: END bit error in Read Data (Illegal data length). Case 3: END bit error in Write CRC Status (Illegal CRC status length). Case 4: END bit error in SD_STOP response.
1	R/W	0b	**CRC Error (ERR1)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: CRC error occurs. There are four cases: Case 1: Error in Write CRC Status. Case 2: CRC error in Read Data. Case 3: CRC error in SD_STOP response. Case 4: CRC error in Command response.
0	R/W	0b	**Command Error (ERR0)** Writing "0" to this bit will clear it. 0: Normal from the last clear. 1: Command error occurs. There are two cases: Case 1: Command index error in Command response. Case 2: Command index error in SD_STOP response.

8.5.3.12 SD Memory Card Information Mask Register (SD_INFOL_MASK and SD_INFOH_MASK)

The SD Memory Card Information Mask, a 16-bit **read/write** register, enables SD_INFOL and SD_INFOH to generate interrupt with writing "0" to each bit.

Index: 20h (SD_INFOL_MASK)

Bit	R/W	Default	Description
7 – 3	--	--	**Reserved for ITE use.**
2	R/W	1b	**Write/Read Access all End Mask** 0: Enables SD_INFOL2 (Write/Read Access all End) to generate interrupt. 1: Masks SD_INFOL2 (Write/Read Access all End) to generate interrupt.
1	--	--	**Reserved for ITE use.**
0	R/W	1b	**Response End Mask** 0: Enables SD_INFOL0 (Response End) to generate interrupt. 1: Masks SD_INFOL0 (Response End) to generate interrupt.

Index: 21h (SD_INFOH_MASK)

Bit	R/W	Default	Description
7 – 2	--	--	**Reserved for ITE use.**
1	R/W	1b	**SDA_D3 Card Inserted Mask** 0: Enables SD_INFOH1 (SDA_D3 Card Inserted) to generate interrupt. 1: Masks SD_INFOH1 (SDA_D3 Card Inserted) to generate interrupt.
0	R/W	1b	**SDA_D3 Card Removed Mask** 0: Enables SD_INFOH0 (SDA_D3 Card Removed) to generate interrupt. 1: Masks SD_INFOH0 (SDA_D3 Card Removed) to generate interrupt.

8.5.3.13 SD Memory Card Buffer Status Mask Register (SD_BUFSTS_MASK)

The SD Memory Card Buffer Status Mask, an 8-bit **read/write or read only** register, enables SD_BUFSTS to generate interrupt with writing "0" to each bit.

Index: 22h

Bit	R/W	Default	Description
7	R/W	1b	**Illegal Access Error Mask (IMASK)** 0: Enables SD_BUFSTS7 (Illegal Access Error) to generate interrupt. 1: Masks SD_BUFSTS7 (Illegal Access Error) to generate interrupt.
6 – 2	--	00h	**Reserved for ITE use.**
1	R/W	1b	**Write Enable Mask (BMSK1)** 0: Enables SD_BUFSTS1 (Write Enable) to generate interrupt. 1: Masks SD_BUFSTS1 (Write Enable) to generate interrupt.
0	R/W	1b	**Read Enable Mask (BMSK0)** 0: Enables SD_BUFSTS0 (Read Enable) to generate interrupt. 1: Masks SD_BUFSTS0 (Read Enable) to generate interrupt.

8.5.3.14 SD Memory Card Error Mask Register (SD_ERR_MASK)

The SD Memory Card Error Mask, an 8-bit **read/write or read only** register, enables SD_ERR to generate interrupt with writing "0" to each bit.

Index: 23h

Bit	R/W	Default	Description
7	--	0b	**Reserved for ITE use.**
6	R/W	1b	**Response Timeout Mask (EMASK6)** 0: Enables ERR6 (Response Timeout) to generate interrupt. 1: Masks ERR6 (Response Timeout) to generate interrupt.
5	R/W	1b	**Illegal Read Access Mask (EMASK5)** 0: Enables ERR5 (Illegal Read Access) to generate interrupt. 1: Masks ERR5 (Illegal Read Access) to generate interrupt.
4	R/W	1b	**Illegal Write Access Mask (EMASK4)** 0: Enables ERR4 (Illegal Write Access) to generate interrupt. 1: Masks ERR4 (Illegal Write Access) to generate interrupt.
3	R/W	1b	**Timeout Mask (EMASK3)** 0: Enables ERR3 (Timeout) to generate interrupt. 1: Masks ERR3 (Timeout) to generate interrupt.
2	R/W	1b	**End Error Mask (EMASK2)** 0: Enables ERR2 (End Error) to generate interrupt. 1: Masks ERR2 (End Error) to generate interrupt.
1	R/W	1b	**CRC Error Mask (EMASK1)** 0: Enables ERR1 (CRC Error) to generate interrupt. 1: Masks ERR1 (CRC Error) to generate interrupt.
0	R/W	1b	**Command Error Mask (EMASK0)** 0: Enables ERR0 (Command Error) to generate interrupt. 1: Masks ERR0 (Command Error) to generate interrupt.

8.5.3.15 SD Clock Enable Register (SD_CLKEN)

The SD Clock Enable, a **read/write** register, enables the SDCLK divisor.

Index: 24h

Bit	R/W	Default	Description
7 – 1	--	00h	**Reserved for ITE use.**
0	R/W	0b	**SD Clock Enable (SDCLK_EN)** Software has to wait at least 250ms (SD Memory power up time) after card is inserted. 0: Disable. 1: Enable.

8.5.3.16 SD Clock Devisor Register (SD_CLK_DIV)

The SD Clock Enable, a **read/write** register, enables the SDCLK divisor.

Index: 25h

Bit	R/W	Default	Description
7 – 0	R/W	20h	**SD Clock Divisor Select (SD_CLK_DIV)** Frequency of SDCLK is the frequency of the clock source of SD I/F Controller (48MHz or 33MHz, selected by bit 1 of Clock Selection register. Please refer to 8.3.6) divided by Divisor. 00h: Divisor = 2 01h: Divisor = 4 02h: Divisor = 8 04h: Divisor = 16 08h: Divisor = 32 10h: Divisor = 64 20h: Divisor = 128 40h: Divisor = 256 80h: Divisor = 512 Else: Reserved

8.5.3.17 SD Transfer Data Length Register (SD_SIZEL and SD_SIZEH)

The SD Transfer Data Length, a 10-bit **read/write** register, determines the transfer data length. For SD memory multiple Read, software can only set 512 Bytes. If an undefined code is selected, the transfer data length will be 512 Bytes.

Index: 26h (SD_SIZEL)

Bit	R/W	Default	Description
7 – 3	R/W	00h	**Transfer Data Length [7:0] (LEN [7:0])**

Index: 27h (SD_SIZEH)

Bit	R/W	Default	Description
7 – 2	--	--	**Reserved for ITE use.**
1 – 0	R/W	2h	**Transfer Data Length [9:8] (LEN [9:8])**

Table 8-3. SD Data Transfer Data Length

LEN [9:0]	Transfer Data Length	Explanation
10'b10_0000_0000	512 Bytes (Default)	Data
10'b01_1111_1111 ~ 10'b01_0000_0001	511 Bytes ~ 257 Bytes	Only use data area access
10'b01_0000_0000	256 Bytes	
10'b00_1111_1111 ~ 10'b00_1000_0001	255 Bytes ~ 129 Bytes	Only use data area access
10'b00_1000_0000	128 Bytes	
10'b00_0111_1111 ~ 10'b00_0100_0001	127 Bytes ~ 65 Bytes	Only use data area access
10'b00_0100_0000	64 Bytes	
10'b00_0011_1111 ~ 10'b00_0010_0001	63 Bytes ~ 33 Bytes	Only use data area access
10'b00_0010_0000	32 Bytes	
10'b00_0001_1111 ~ 10'b00_0001_0001	31 Bytes ~ 17 Bytes	Only use data area access
10'b00_0001_0000	16 Bytes	
10'b00_0000_1111 ~ 10'b00_0000_1001	15 Bytes ~ 9 Bytes	Only use data area access
10'b00_0000_1000	8 Bytes	Random number etc.
10'b00_0000_0111 ~ 10'b00_0000_0101	7 Bytes ~ 5 Bytes	Only use data area access
10'b00_0000_0100	4 Bytes	
10'b00_0000_0011	3 Bytes	Only use data area access
10'b00_0000_0010	2 Bytes	
10'b00_0000_0001	1 Byte	For Lock/Unlock
10'b00_0000_0000	Not defined	

8.5.3.18 SD Access Control Option Register (SD_OPTION)

The SD Access Control Option, an 8-bit **read/write** register, controls some time counters.

Index: 28h

Bit	R/W	Default	Description
7 – 4	R/W	Eh	**SD Response Timeout Counter** 1111b: Timeout Test mode 1110b: SDCLK * 2^{27} (Default) 1101b: SDCLK * 2^{26} **:** **:** 0001b: SDCLK * 2^{14} 0000b: SDCLK * 2^{13}
3 – 0	R/W	Eh	**SD Card Detect Stability Time Counter** 1111b: Timeout Test mode 1110b: SD I/F Controller Clock * 2^{24} (Default) 1101b: SD I/F Controller Clock * 2^{23} **:** **:** 0001b: SD I/F Controller Clock * 2^{11} 0000b: SD I/F Controller Clock * 2^{10}

8.5.3.19 SD Data Width Register (SD_DATA_SEL)

The SD Data Width, a **read/write** register, selects the transfer data width.

Index: 29h

Bit	R/W	Default	Description
7 – 1	--	00h	**Reserved for ITE use.**
0	R/W	0b	**SD Data Width** 0: 4 bits width. 1: 1 bit width.

8.5.3.20 SD CMD and END Error Status Register (SD_CMD_END_ERR_STS)

The SD CMD and END Error Status, an 8-bit **read only** register, responds Command and End error messages.

Index: 2Ch

Bit	R/W	Default	Description
7 – 6	--	00b	**Reserved for ITE use.**
5	R	0b	**END Error in Write CRC Status** 0: Normal. 1: END bit error in Write CRC Status.
4	R	0b	**END Error in Read Data Status** 0: Normal. 1: END bit error in Read Data.
3	R	0b	**END Error in SD_STOP Response** 0: Normal. 1: END bit error in SD_STOP response.
2	R	0b	**END Error in Command Response** 0: Normal. 1: END bit error in Command response.
1	R	0b	**Command Index Error in SD_STOP Response** 0: Normal. 1: Command index error in SD_STOP response.
0	R	0b	**Command Index Error in Command Response** 0: Normal. 1: Command index error in command response.

8.5.3.21 SD CRC Error Status Register (SD_CRC_ERR_STS)

The SD CRC Error Status, an 8-bit **read only** register, responds CRC error messages.

Index: 2Dh

Bit	R/W	Default	Description
7	--	0b	**Reserved for ITE use.**
6 – 4	R	010b	**Write CRC Status**
3	R	0b	**Error in Write CRC Status** 0: Normal. 1: Error in writes CRC status.
2	R	0b	**CRC Error in Read Data** 0: Normal. 1: CRC Error in Read Data.
1	R	0b	**CRC Error in SD_STOP Response** 0: Normal. 1: CRC Error in SD_STOP response.
0	R	0b	**CRC Error in Command Response** 0: Normal. 1: CRC Error in command response.

8.5.3.22 SD Timeout Error Status Register (SD_TIMEOUT_ERR_STS)

The SD Timeout Error Status, an 8-bit **read only** register, responds Timeout error messages.

Index: 2Eh

Bit	R/W	Default	Description
7	--	0b	**Reserved for ITE use.**
6	R	0b	**More BUSY after Write CRC Status** 0: Normal. 1: Keep busy more than N cycles after Write CRC Status.
5	R	0b	**No Write CRC Status** 0: Normal. 1: No Write CRC Status more than N cycles after Write cycle.
4	R	0b	**No Read Data in Read Command** 0: Normal. 1: No Read Data more than N cycles after Read Command.
3	R	0b	**More Busy after SD_STOP** 0: Normal. 1: Keep busy more than N cycles after SD_STOP.
2	R	0b	**More Busy after R1b Response** 0: Normal. 1: Keep busy more than N cycles after R1b response.
1	R	0b	**No SD_STOP Response** 0: Normal. 1: No SD_STOP response more than 640 SDCLK.
0	R	0b	**No Command Response** 0: Normal. 1: No Command response more than 640 SDCLK.

8.5.3.23 SD Buffer Read/Write Port Register (SD_BUFL and SD_BUFH)

This register receives/transmits data from/to SD Card. This register connects to internal 512-byte buffer RAM.

Index: 30h (SD_BUFL)

Bit	R/W	Default	Description
7 – 0	R/W	00h	**Buffer [7:0] (BUF [7:0])**

Index: 31h (SD_BUFH)

Bit	R/W	Default	Description
7 – 0	R/W	00h	**Buffer [15:8] (BUF [15:8])**

8.5.3.24 SDIO Mode Control Register (SD_MODE1 and SD_MODE2)

The SDIO Mode Control registers select SDIO mode.

Index: 34h (SDIO_MODE1)

Bit	R/W	Default	Description
7 – 3	--	00h	**Reserved for ITE use.**
2	R/W	0b	**Read Wait Request (RWREQ)** This command is related when it is used on multiple read/write (CMD18, CMD25, CMD53 etc). RWREQ is not available in the conditions during Last sector transfer, CMD12 and IO abort no transaction. In the conditions, it will be automatically disabled. When RWREQ is set in the condition, it asserted EXWT. (Not pull down DAT2) It recommends setting C52PUB and RWREQ at the same time on read transfer. 0: Not reflect. When SDIO direct RW commands complete on read wait function, software should clear RWREQ. 1: Read Wait mode enables. This bit is only reflected in multiple read transfer operation. Case 1:When Read transfer with IOABT set, Read-wait (DAT2=”0”) is automatically released (DAT=”1”) after CMD52. Case 2:When Read transfer with C52PUB set, Read-wait (DAT2=”0”) is not automatically released (DAT2=”1”) after CMD52. Case 3:When no transaction; (It should not be used) When RWREQ is set, Read-wait (DAT2=”0”) is not asserted. RWREQ will not be automatically cleared.
1	--	0b	**Reserved.**
0	R/W	0b	**SD IO mode (IOMOD)** 0: Disable SD Host controller to receive IRQ from SDIO card on Port 0. 1: Enable SD Host controller to receive IRQ from SDIO card on Port 0.

Index: 35h (SDIO_MODE2)

Bit	R/W	Default	Description
7 – 2	--	00h	**Reserved for ITE use.**
1	R/W	0b	**SDIO Abort Data During the reception Not Cancelled (C52PUB)** This command is related when it is used on multiple read/write (CMD18, CMD25, CMD53 etc). C52PUB is not available in the conditions during Last sector transfer, CMD12 and IO abort no transaction. In the conditions, it will be automatically disabled. When C52PUB is set in the condition, it asserted EXPUB52. (Not transfer CMD52) It recommends setting C52PUB and RWREQ at the same time on read transfer. The value in SD_ARG, set before this register is set, will be the argument of CMD52. 0: Clear. 1: CMD52 (none abort) is automatically transmitted when this bit is set. In addition, SD Controller transmission state can be waited. The argument of CMD52 will be the value in SD Command Argument register. C52PUB is automatically clear after CMD52 response. Case 1:When Read transfer with RWREQ set; (none abort) CMD52 is automatically transmitted after C52PUB (with RWREQ set) was set and it receives proper sector data and SD controller transmission wait state. Read-wait (DAT2=”0”) is not automatically released (DAT2=”1”) after CMD52. Software should clear RWREQ after response of CMD52 is finished. Case 2:When Write transfer; CMD52 is automatically transmitted after C52PUB is set and it transfers proper sector data and SD Controller transmission wait state. Case 3:When no transaction; (It should not be used.) When C52PUB is set, CMD52 will not be transferred. C52PUB is not auto-cleared.
0	R/W	0b	**SDIO Abort Data During the reception Cancelled (IOABT)** IOABT bit should only be used in IO multiple transaction. This command is related when it is used on multiple read/write (CMD53). 0: Cleared. 1: CMD52 (abort) is automatically transmitted when this bit is set and SD controller transmission state can be aborted. The value in SD_ARG, set before this register is set, will be the argument of CMD52. IOABT will not be auto-cleared. Software needs to clear this bit after command response. Case 1:When Read transfer with RWREQ set; When IOABT is set, CMD52 is transferred soon. In addition, Read-wait (DAT2=”0”) is automatically released (DAT2=”1”) after CMD52 (abort). Case 2:When Read transfer without RWREQ set; When IOABT is set, CMD52 is transferred soon. Case 3:When Write transfer; When IOABT is set and block data transferred completely, CMD52 is transferred. Case 4:When no transaction; (It should not be used.) When IOABT is set, CMD52 will not be transferred.

8.5.3.25 SD IO Card Information Register (SDIO_INFOL and SDIO_INFOH)

The SD IO Card Information, a 16-bit **read/write or read only** register, responds some IO cards' status. If one bit of this register is set to "1" and the relative bit in SDIO_INFO_MASK is enabled (not masked), an interrupt will be asserted to the host.

Index: 36h (SDIO_INFOL)

Bit	R/W	Default	Description
7 – 3	--	00h	**Reserved for ITE use.**
2	R/W	0b	**Read Wait Ready (RWRDY)** Writing "0" to this bit will clear it. 0: Normal. 1: SD controller is ready to read wait mode. DAT2 is pulled down 2 clocks after the end of data block.
1	R/W	0b	**SD IO Abort Ready (C52RDY)** Writing "0" to this bit will clear it. 0: Normal. 1: SD controller is ready to issue CMD52. (Data during the reception are not cancelled but CMD52 is issued automatically.)
0	R/W	0b	**SDIO Interrupt (IOIRQ)** Writing "0" to this bit will clear it. SD controller can recognize SDIO card interrupt as follows (interrupt period); Case 1: Asynchronous interrupt; SD controller can recognize asynchronous interrupt when there is no data transfer state. SDIO IRQ trigger is DAT1 pulled down in SDIO asynchronous interrupt period. Case 2: 4bit mode and with data command; SD controller can recognize synchronous interrupt in the data transfer state. SDIO IRQ trigger is DAT1 pulled down in SDIO synchronous interrupt period. (Between data blocks) 0: No interrupt. 1: An interrupt occurs from SDIO card on port 0.

Index: 37h (SDIO_INFOH)

Bit	R/W	Default	Description
7	R/W	0b	**Exclude Read Wait Area (EXWT)** Writing "0" to this bit will clear it. 0: Normal. 1: When not read operation, software sets RWREQ. SD controller fails in read wait mode. RWREQ is still asserted at the end of any transaction. When RWREQ is set during Last section transfer, CMD12 and IO abort, EXWT will be set.
6	R/W	0b	**Exclude PUB52 Area (EXPUB52)** Writing "0" to this bit will clear it. 0: Normal. 1: When not read/write operation, software sets C52PUB. SD controller fails to issue CMD52. C52PUB is still asserted at the end of any transaction. When C52PUB is set during Last section transfer, CMD12 and IO abort, EXPUB52 will be set.
5 – 0	--	00h	**Reserved for ITE use.**

8.5.3.26 SDIO Card Information Mask Register (SDIO_INFOL_MASK and SDIO_INFOH_MASK)

The SDIO Card Information Mask, a 16-bit **read/write** register, enables SDIO_INFOL and SDIO_INFOH to generate interrupt with writing "0" to each bit.

Index: 38h (SDIO_INFOL_MASK)

Bit	R/W	Default	Description
7 – 3	--	--	**Reserved for ITE use.**
2	R/W	0b	**RWRDY Mask (MEXWT)** 0: Enables RWRDY of SDIO_INFOL to generate interrupt. 1: Masks RWRDY of SDIO_INFOL to generate interrupt.
1	R/W	0b	**C52RDY Mask (MEXWT)** 0: Enables C52RDY of SDIO_INFOL to generate interrupt. 1: Masks C52RDY of SDIO_INFOL to generate interrupt.
0	R/W	1b	**IOIRQ Mask (IOMSK)** 0: Enables IOIRQ of SDIO_INFOL to generate interrupt. 1: Masks IOIRQ of SDIO_INFOL to generate interrupt.

Index: 39h (SDIO_INFOH_MASK)

Bit	R/W	Default	Description
7	R/W	0b	**EXWT Mask (MEXWT)** 0: Enables EXWT of SDIO_INFOH to generate interrupt. 1: Masks EXWT of SDIO_INFOH to generate interrupt.
6	R/W	0b	**EXPUB52 Mask (MEXPUB52)** 0: Enables EXPUB52 of SDIO_INFOH to generate interrupt. 1: Masks EXPUB52 of SDIO_INFOH to generate interrupt.
5 – 0	--	00h	**Reserved for ITE use.**

8.5.3.27 DMA Enable Register (DMA_EN)

The DMA Enable, a **read/write** register, enables the DMA data transfer between the host and the SD controller.

Index: 6Ch

Bit	R/W	Default	Description
7 – 2	--	00h	**Reserved for ITE use.**
1	R/W	0b	**DMA Enable (DMAEN)** 0: Disable. 1: Enable DMA mode for Data buffer read and write.
0	--	0b	**Reserved for ITE use.**

8.5.3.28 Software Reset Register (SOFT_RST)

The Software Reset, a **read/write** register, resets SD Memory Card interface module.

Index: E0h

Bit	R/W	Default	Description
7 – 1	--	00h	**Reserved for ITE use.**
0	R/W	0b	**Software Reset (SDRST)** 0: Reset SD Memory Card interface. 1: Release reset.

8.5.3.29 Controller Version Register (VERSION)

The Controller Version, a **read only** register, responds the controller development version.

Index: E2h

Bit	R/W	Default	Description
7 – 0	R	04h	**Controller Version (VERSION)**

8.5.3.30 SD Card I/F Power Register (Power Control)

SDAPWR# and SDBPWR# cannot be active simultaneously.

Index: F2h

Bit	R/W	Default	Description
7 – 2	--	00h	**Reserved for ITE use.**
1	R/W	0b	**Power Control 1 (SDPWR1)** 0: Power off (SDBPWR = Hi-Z). 1: Power ON (SDBPWR = LOW).
0	R/W	0b	**Power Control 0 (SDPWR0)** 0: Power off (SDAPWR = Hi-Z). 1: Power ON (SDAPWR = LOW).

8.5.3.31 SD IO Card Information for Port 1 Register (EXT_SDIO)

The SD IO Card Information for Port 1, an 8-bit **read/write or read only** register, includes IOIRQ1 and IOMOD1 for Port 1.

Index: F4h (EXT_SDIO)

Bit	R/W	Default	Description
7 – 5	--	0h	**Reserved for ITE use.**
4	R/W	0b	**SD IO Mode for Port 1 (IOMOD1)** 0: Disable SD Host controller to receive IRQ from SDIO card on Port 1. 1: Enable SD Host controller to receive IRQ from SDIO card on Port 1.
3 – 1	--	0h	**Reserved for ITE use.**
0	R/W	0b	**SDIO Interrupt for Port 1(IOIRQ1)** Writing "0" to this bit will clear it. SD controller can recognize SDIO card interrupt as follows (interrupt period); Case 1: Asynchronous interrupt; SD controller can recognize asynchronous interrupt when there is no data transfer state. SDIO IRQ trigger is DAT1 pulled down in SDIO asynchronous interrupt period. Case 2: 4bit mode and with data command; SD controller can recognize synchronous interrupt in data transfer state. SDIO IRQ trigger is DAT1 pulled down in SDIO synchronous interrupt period. (Between data blocks) 0: No interrupt. 1: An interrupt occurs from the SDIO card on port 1.

8.5.3.32 SDIO Card Information Mask for Port 1 Register (EXT_SDIO MASK)

The SDIO Card Information Mask for Port 1, an 8-bit **read/write** register, enables IOIRQ1 to generate interrupt with writing "0" to it.

Index: F5h (EXT_SDIO MASK)

Bit	R/W	Default	Description
7 – 1	--	03h	**Reserved for ITE use.**
0	R/W	1b	**IOIRQ1 Mask (IOMSK1)** 0: Enables IOIRQ1 of EXT_SDIO to generate interrupt. 1: Masks IOIRQ1 of EXT_SDIO to generate interrupt.

8.5.3.33 Write Protect for Port 1 Register (EXT_WP)

Index: F6h (EXT_WP)

Bit	R/W	Default	Description
7 – 1	--	--	**Reserved for ITE use.**
0	R	--	**Write Protect for Port 1** 0: Normal. 1: Write Protect for Port 1.

8.5.3.34 Card Detect with SDB_DAT3 Register (EXT_CD_DAT3)

Index: 1Dh (EXT_CD_DAT3)

Bit	R/W	Default	Description
7 – 3	--	--	**Reserved for ITE use.**
2	R	--	**SDB_D3 Card Detect** When there is no data transfer, SDB_D3 is used as card detection. 0: SDB_D3 is low. 1: SDB_D3 is high.
1	R/W	0b	**SDB_D3 Card Inserted** Writing "0" to this bit will clear it. During four-bit data transfer, this status should be ignored. 0: No Card insertion detected from the last clear. 1: Card insertion detected.
0	R/W	0b	**SDB_D3 Card Removed** Writing "0" to this bit will clear it. During four-bit data transfer, this status should be ignored. 0: No Card removal detected from the last clear. 1: Card removal detected.

8.5.3.35 Card Detect with SDB_DAT3 Mask Register (EXT_CD_DAT3_MASK)

Index: FEh (EXT_CD_DAT3_MASK)

Bit	R/W	Default	Description
7 – 2	--	--	**Reserved for ITE use.**
1	R/W	1b	**SDB_D3 Card Inserted Mask** 0: Enables bit 1 of EXT_CD_DAT3 (SDB_D3 Card Inserted) to generate interrupt. 1: Masks bit 1 of EXT_CD_DAT3 (SDB_D3 Card Inserted) to generate interrupts.
0	R/W	1b	**SDB_D3 Card Removed Mask** 0: Enables bit 0 of EXT_CD_DAT3 (SDB_D3 Card Removed) to generate interrupt. 1: Masks bit 0 of EXT_CD_DAT3 (SDB_D3 Card Removed) to generate interrupts.

8.6 Smart Media Host Controller

8.6.1 Overview

The Smart Media Host Controller provides the interface between a host processor and Smart Media I/F. The hardware is implemented from the reference circuit of *SmartMedia™ Interface Library (SMIL)*.

8.6.2 Features

- Flash Memory Control Interface
- Eject On/Off
- Lock/Unlock Function
- ECC Calculation circuit

8.6.3 Register Descriptions

Table 8-4. Memory Stick Register List

Address	R/W	Default	Name
Base + 0h	R/W	0--	Data Register (DATAR)
Base + 0h	R	--	Controller Identify Register (CIDR, total 12 bytes)
Base + 0h	R	--	ECC Register (ECCR, total 6 bytes)
Base + 2h	W	00h	Mode Register (MODER)
Base + 2h	R	00h	Status Register (STSR)
Base + 4h	R	00h	Interrupt Status Register (INTSTSR)
Base + 6h	R	00h	Interrupt Mask Register (INTMSKR)

8.6.3.1 Data Register (DATAR)

Address: Base address + 0h

Bit	R/W	Default	Description
7 – 0	R/W	01h	**Data Register (DATA[7:0])** This is the register to execute data transfer between SmartMedia™ and host system. By writing this register, the SmartMedia Card will be programmed. By reading this register, the SmartMedia Card, ECC data and controller ID will be read

8.6.3.2 Mode Register (MODER)

Address: Base address + 2h

Bit	R/W	Default	Description
7 – 0	R/W	01h	**Mode Register (MODE [7:0])** This register will set the data transfer mode of the Data Register. It is prohibited to use other commands not specified in the table below.

Table 8-5. Mode register setting command

Command	Code	Function
Read Data	0001 0100(14h)	SmartMedia Data Read Mode
Write command	0001 0101(15h)	SmartMediaTM Command Write Mode (SmartMedia Data Read)
Write Address	0001 0110(16h)	SmartMedia Address Write Mode (SmartMedia Data Read)
Write Data	1001 0100(94h)	SmartMedia Data Write Mode
Write command	1001 0101(95h)	SmartMedia Command Write Mode (SmartMedia Data Write/Erase)
Write Address	1001 0110(96h)	SmartMedia Address Write Mode (SmartMedia Data Write/Erase)
Standby	0000 0000(00h)	SmartMedia Standby Mode
Vcc Power Off	0000 1000(08h)	Vcc Power Off for SmartMedia
Vcc Power On	0000 1100(0Ch)	Vcc Power On for SmartMedia
LED Off	xxxx x0xx(00h)	LED turn Off
LED On	xxxx x1xx(04h)	LED turn On
SmartMediaTM Eject On	0110 1000(68h)	SmartMedia Eject On
SmartMediaTM Eject Off	0000 1000(08h)	SmartMedia Eject Off
SmartMedia Lock	0110 1100(6Ch)	SmartMedia Locked
SmartMedia UnLock	0000 1100(0Ch)	SmartMedia UnLocked
Reset ECC Logic	X11X XXXX(-)	SmartMedia ECC Data Reset
R/W with ECC	X011 XXXX(-)	SmartMedia Data Read with ECC data count up
Read ECC Data	X101 XXXX(-)	SmartMedia ECC Data Read
Read Controller ID	X100 XXXX(40h)	Controller Identify Data Read

8.6.3.3 Status Register (STSR)

Address: Base address + 2h

Bit	R/W	Default	Description
7	R	0b	**Busy / -Ready** Shows the present status of SmartMediaTM 0: Ready. 1: Busy.
6	R	0b	**SmartMedia Model** Shows the model of SmartMedia 0: 3.3V Vcc SmartMedia. 1: 5V Vcc SmartMedia.
5	R	0b	Reserved
4	R	0b	**SmartMedia Power ON** Only when the SmartMedia card is inserted, power can be turned on. If the card is ejected during power supply, the power will be cut off. 0: Power OFF. 1: Power ON.
3	R	0b	**Card Status Change** Shows changing to a different status. Actually, this means the cases of card inserting and card ejecting. This bit will be reset by writing on the mode register.
2	R	0b	**Card Enable** Shows inserting status of SmartMedia. 0: No SmartMedia. 1: SmartMedia Ready.
1	R	0b	**Card EJECT Request** Shows the interrupting by eject command (Ex. switch on/off) This bit will be reset by writing 1 on bit-3 of the mode register. 0: None. 1: EJECT Request.
0	R	0b	**Write Protect Seal Detected** Shows writing protected or not (Protection seals detected). 0: Write Enabled. 1: Write Protected

8.6.3.4 Interrupt Status Register (INTSTSR)

Address: Base address + 4h

Bit	R/W	Default	Description
7 – 4	R	0h	**Reserved.**
3	R	0b	***Card Insert Request*** If SmartMedia card is inserted in a connector, this bit is set. When writing, "1", this bit is changed to "0".
2	R	0b	**Card Out Request** When SmartMediaTM card is ejected from a connector, this bit is set. When writing, "1", this bit is changed to "0".
1	R	0b	**Card EJECT Request** Shows there is interrupting of EJECT request by switch during locked mode. When writing, "1", this bit is changed to "0".
0	R	0b	**SmartMedia Ready Request** When R/-B signal of SmartMedia is changed from "Low" to "High", this bit is set. When writing, "1", this bit is changed to "0".

8.6.3.5 Interrupt Mask Register (INTMSKR)

Address: Base address + 6h

Bit	R/W	Default	Description
7	R/W	0b	**Interrupt Enable** The setting of permission / prohibition of -INT signal.
6 – 4	--	0h	**Reserved.**
3	R/W	0b	**Card Insert Request Mask** Generation of interrupt depends on Interrupt Status Register [3]. 0: None. 1: Enable Card Insert Request.
2	R/W	0b	**Card Out Request Mask** Generation of interrupt depends on Interrupt Status Register [2]. 0: None. 1: Enable Card out Request.
1	R/W	0b	**Card EJECT Request Mask** Generation of interrupt depends on Interrupt Status Register [1]. 0: None. 1: Enable Card EJECT Request.
0	R/W	0b	**SmartMedia Ready Request Mask** Generation of interrupt depends on Interrupt Status Register [0]. 0: None. 1: Enable Ready Request.

8.7 Memory Stick Host Controller

8.7.1 Overview

The Memory Stick Host Controller provides the interface between a host processor and Memory Stick I/F. The Memory Stick Interface complies with Sony Memory Stick Standard Ver 1.3. It supports up to 20MHz clock.

8.7.2 Features

- Memory Stick V1.3 Specifications compliant
- Up to 20MHz interface serial clock
- Built-in 16-byte FIFO buffers for transmit and receive respectively
- Built-in CRC circuit
- DMA supported
- Interrupt polling transmission supported
- Automatic command execution (can be turned on/off) when INT from the Memory Stick is detected

8.7.3 Register Descriptions

Table 8-6. Memory Stick Register List

Address	R/W	Default	Name
Base + 0h	R/W	01h	MS Command 1 Register
Base + 1h	R/W	00h	MS Command 2 Register
Base + 2h	R	0Ah	MS Status Register
Base + 3h	R/W	05h	MS Control Register
Base + 4h	R	00h	MS Receive Data Buffer Register
Base + 4h	W	00h	MS Transmit Data Buffer Register
Base + 5h	R/W	70h	MS ACD Command Register
Base + 6h	R/W	00h	MS Interrupt Control Register
Base + 7h	R	80h	MS Interrupt Data Register

8.7.3.1 MS Command 1 Register

The MS Command 1, an 8-bit **read/write** register, is the data size [7:0] for Command.

Address: Base address + 0h

Bit	R/W	Default	Description
7 – 0	R/W	01h	**Data Size [7:0] Register** This register is Data size [7:0] (total 10 bits). The value is determined for each PID code.

8.7.3.2 MS Command 2 Register

The MS Command 2, an 8-bit **read/write** register, determines PID code (4 bits) and the data size [9:8] for Command.

Address: Base address + 1h

Bit	R/W	Default	Description
7 – 4	R/W	0h	**Packet ID (PID) Register** PID code (4 bits).
3 – 2	-	-	**Reserved for ITE use.**
1 – 0	R/W	0h	**Data Size [9:8] Register** This register is Data size [9:8] (total 10 bits). The value is determined for each PID code.

8.7.3.3 MS Status Register

The MS Status, an 8-bit **read only** register, is used to respond the status of the MS controller.

Address: Base address + 2h

Bit	R/W	Default	Description
7	R	0b	**Interrupt (INT)** This bit is “1” when an interrupt condition is generated. Otherwise, “0”. Change even when the INTEN bit of the Interrupt Control Register is “0”.
6	R	0b	**Data Request (DARQ)** This bit is “1” when data transfer is requested. Otherwise, “0”.
5 – 4	-	-	**Reserved for ITE use.**
3	R	1b	**Receive Buffer Empty (RBE)** This bit is “1” when receive data buffer is empty. It is “0” when there are data in receive data buffer.
2	R	0b	**Receive Buffer Full (RBF)** This bit is “1” when receive data buffer is full. It is “0” when there is space in receive data buffer.
1	R	1b	**Transmit Buffer Empty (TBE)** This bit is “1” when transmit data buffer is empty. It is “0” when there are data in transmit data buffer.
0	R	0b	**Transmit Buffer Full (TBF)** This bit is “1” when transmit data buffer is full. It is “0” when there is space in transmit data buffer.

8.7.3.4 MS Control Register

The MS Control, an 8-bit **read/write** register, is used to determine some parameters for the MS controller.

Address: Base address + 3h

Bit	R/W	Default	Description
7	R/W	0b	**Reset (RST)** Internal reset when “1”, canceled when “0”.
6	R/W	0b	**Power Save (PWS)** Power save mode when “1”, canceled when “0”. During PWS=1, the clock of Memory Stick I/F side logic is stopped. MS Command 1, 2, MS ACD registers are not performed to write.
5	R/W	0b	**Serial I/F Enable (SIEN)** Serial IF output enabled when “1”, disabled when “0”. Normally set to “1” during operation.
4	R/W	0b	**DMA Enable (DMAEN)** DMA enabled when “1”, disabled when “0”.
3	R/W	0b	**No CRC (NOCRC)** CRC is off when “1” and on when “0”. In mode, data are transmitted/received without adding a CRC (16-bit) at the end of the data array.
2 – 0	R/W	5h	**Busy Count (BSYCNT)** RDY timeout time setting (serial clock count). These bits are set to the maximum BSY timeout time (set value X 4 + 2) to wait until the RDY signal is output from the card. RDY timeout error detection is not performed when BSYCNT = 0.

8.7.3.5 MS Receive Data Buffer Register

The MS Receive Data Buffer with 16 bytes FIFO holds receive incoming data byte.

Address: Base address + 4h

Bit	R/W	Default	Description
7 – 0	R	00h	**Receive Data Buffer Register** When RBE is "1", invalid data is read.

8.7.3.6 MS Transmit Data Buffer Register

The MS Transmit Data Buffer with 16 bytes FIFO contains the data byte to be transmitted.

Address: Base address + 4h

Bit	R/W	Default	Description
7 – 0	W	00h	**Receive Data Buffer Register** When TBF is "1", writing data is ignored.

8.7.3.7 MS ACMD Register

The MS ACMD, an 8-bit **read/write** register, determines APID code (4 bits) and the ADATASIZE for Auto Command.

Address: Base address + 5h

Bit	R/W	Default	Description
7 – 4	R/W	7h	**Auto Command Packet ID (APID) Register** APID code (4 bits).
3	-	-	**Reserved for ITE use.**
2 – 0	R/W	0h	**Auto Command Data Size [2:0] Register** This register is Data size [2:0]. The value is determined for each APID code.

8.7.3.8 MS Interrupt Control Register

The MS Interrupt Control, an 8-bit **read/write** register, is used to enable some interrupt events for the MS controller.

Address: Base address + 6h

Bit	R/W	Default	Description
7	R/W	0b	**Interrupt Enable (INTEN)** Interrupt is enabled when "1" and disabled when "0". An interrupt is generated when an interrupt condition occurs after INTEN has been set to "1".
6	R/W	0b	**Data Request Interrupt Enable (DRQSL)** Interrupt during data transfer request is enabled when "1" and disabled when "0". An interrupt is generated when an interrupt condition occurs after INTEN has been set to "1".
5	R/W	0b	**Card Detect Interrupt Enable (CDIEN)** Interrupt for MSDET (MSDET_S) level changing is enabled when "1" and disabled when "0".
4	R/W	0b	**Power On (PWRON)** MSPWR (MSPWR_S) is low when "1" and High-Z when "0".
3 – 2	-	-	**Reserved for ITE use.**

[cont'd]

Bit	R/W	Default	Description
1	R/W	0h	**Auto Command (ACD)** When this bit is set to "1", an ACD command is automatically executed after an INT is detected. When "0", disable the ACD command.
0	R/W	0h	**Rise Edge Data (RED)** When this bit is set to "1", serial data are loaded at the falling edge of the clock. When "0", loaded at the rising edge.

8.7.3.9 MS Interrupt Data Register

The MS Status, an 8-bit **read only** register, is used to respond the Interrupt event data of the MS controller.

Address: Base address + 7h

Bit	R/W	Default	Description
7	R	1b	**Ready (RDY)** This bit is “1” when the Protocol is ended and “0” when it communicates with Memory Stick.
6	R	0b	**Serial I/F Interrupt (SIF)** This bit is “1” when the Serial I/F receives INT, otherwise “0”. An interrupt output for SIF is separated from one for RDY.
5	R	0b	**Data Request (DARQ)** This bit is “1” when data transfer is requested, otherwise “0”. DARQ can be changed only when the DRQSL of Interrupt Control register is “1”.
4	R	0b	**Card Detect Interrupt (CDI)** This bit is “1” when MSDET (MSDET_S) level change is occurred, otherwise “0”. Reading this register will clear this bit.
3 – 2	-	-	**Reserved for ITE use.**
1	R	0b	**CRC Error (CRC)** This bit is “1” when a CRC error occurs while receiving data and “0” when normal. It is cleared to “0” when data are written to the MS Command Register. BS output is set to Low level when a CRC error occurs.
0	R	0b	**Timeout Error (TOE)** This bit is “1” when BSY timeout error occurs and “0” during normal operations. It is cleared to “0” when data are written to the MS Command Register. Exceeding the number of clocks set using BSYCNT of the MS Control Register and BSY from the Memory Stick continues, it is taken as a card malfunction and an RDY timeout error (TOE) is set out.

8.8 Smart Card Reader

8.8.1 Features

As an IFD (InterFace Device) built in IT8228E, the Smart Card Reader (SCR) includes a standard UART (Either Serial Port 1 or Serial Port 2 is set in SCR mode) to control Smart Card interface handshaking and then performs data transfers and can be connected to the smart card socket directly. The Smart Card is capable of providing secured storage facilities for sensitive personal information (such as Private keys, Account numbers, Passwords, Medical information, …etc.). Then the SCR can be used for a wide range of applications in GSM, ID, pay TV, banking (refer to EMV'96 Spec.), … and so forth. It also provides a Smart Card clock divider for those ICC (Integrated Circuit Card) without internal clocks.

8.8.2 Operation

The SCR is a low-power consumption design. Whenever the IFD is inactive, the clock divider will turn off internal clocks even when the clock of IFD controlling / monitoring state machine is turned off to save power consumption. Also it could be waked up immediately when IC card is removed in case of an emergency or when the FET control function is turned on/off.

The VCC power of IC card interface is powered from an external FET to protect the smart card interface. Also, the charge/discharge time for FET to reach 5V/0V is programmable and FET performs automatically to meet ISO 7816 activation and deactivation sequences. The UART's modem control lines: DTR#, RTS# and DCD# are used for controlling FET on/off, Smart Card Reset signal and IC card insertion detection respectively. When an IC card is being inserted, it will switch the SCRPRES# (Smart Card Present Detect#) and then cause the DCD# signal to trigger an interrupt to the system. Then in the Smart Card interrupt service routine, the driver can assert the DTR# signal to power on the external FET (SCRPFET#) and the RTS# signal to control the Smart Card Reset signal (SCRRST). In the mean time, IT8228E will generate a proper clock frequency to allow the IC card with default serial transfer baud rate to send back an ATR (Answer-To-Reset) sequence. The interface signals are enabled after VCC reaches enough voltage level. Then transfer protocol may be negotiated to promote more efficient transfers. In the same way, when the IC card is removed in case of an emergency or when the ICC processing is finished, the driver can de-assert the DTR# to turn off the FET power. However, before the FET power-off and the reset, clock and data signals will be de-active, followed by a sufficient FET discharge time guaranteed to protect IC card and IFD.

8.9 Connection of IFD to ICC Socket

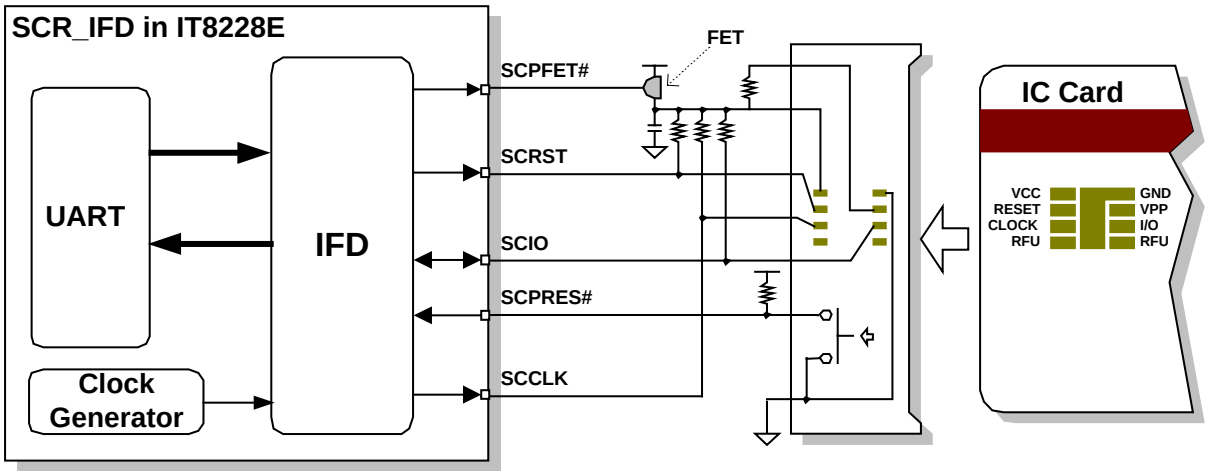


Figure 8-4. Smart Card Reader Application

8.9.1 Baud Rate Relationship Between UART and Smart Card Interface

To perform serial transfers correctly, the baud rate of UART must be set in ways similar to the ICC card.

- **Formula (Variation < 2%)**

$$\text{Baud Rate} = \frac{\text{UART}}{\frac{\frac{24\ \text{MHz}}{13}}{16 * N}} \approx \frac{\text{Smart Card}}{\frac{SCRCLK * D}{F}}$$

N =Divisor of UART, assigned by programming the DLM (Divisor Latch MSB) and DLL (Divisor Latch LSB).
F =Clock Rate Conversion Factor, default = 372.
D =Bit Rate Adjustment Factor, Default is 1.
SCRCLK duty cycle is 45%-55%.

- **ICC With Internal Clock**

ICC may use built-in internal clock, then the Baud rate is 9600 baud, just programming the Divisor Latch Registers of UART in the IT8228E for SCR IFD.

- **ICC Without Internal Clock**

Baud rate is SCRCLK/372 before negotiating and SCRCLK is limited within 1 MHz - 5MHz. During the ATR sequence, the default F value (Clock Rate Conversion Factor) is 372 and the default D value (Bit Rate Adjustment Factor) is 1.

8.9.2 Waveform Relationship

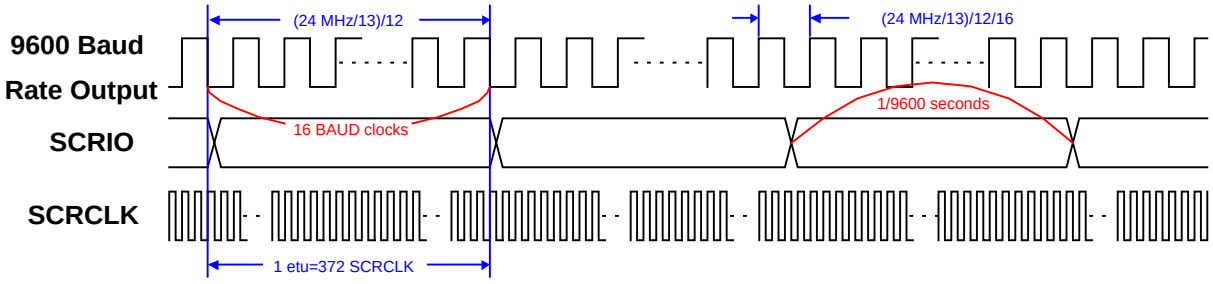


Figure 8-5. 9600 Baud Rate Example

8.9.3 Clock Divider

The SCRCLK is generated as the selection of SCR_CLKSEL1-0, which is determined in the SCR Special Configuration register 2 (LDN4_F1h).

Table 8-7. SCRCLK Selections

SCR_CLKSEL1-0	Selections
00	Stop
01	3.5 MHz
10	7.1 MHz
11	96 MHz / SCR DIV96M Note

8.9.4 Waveform Example of Activation/Deactivation Sequence

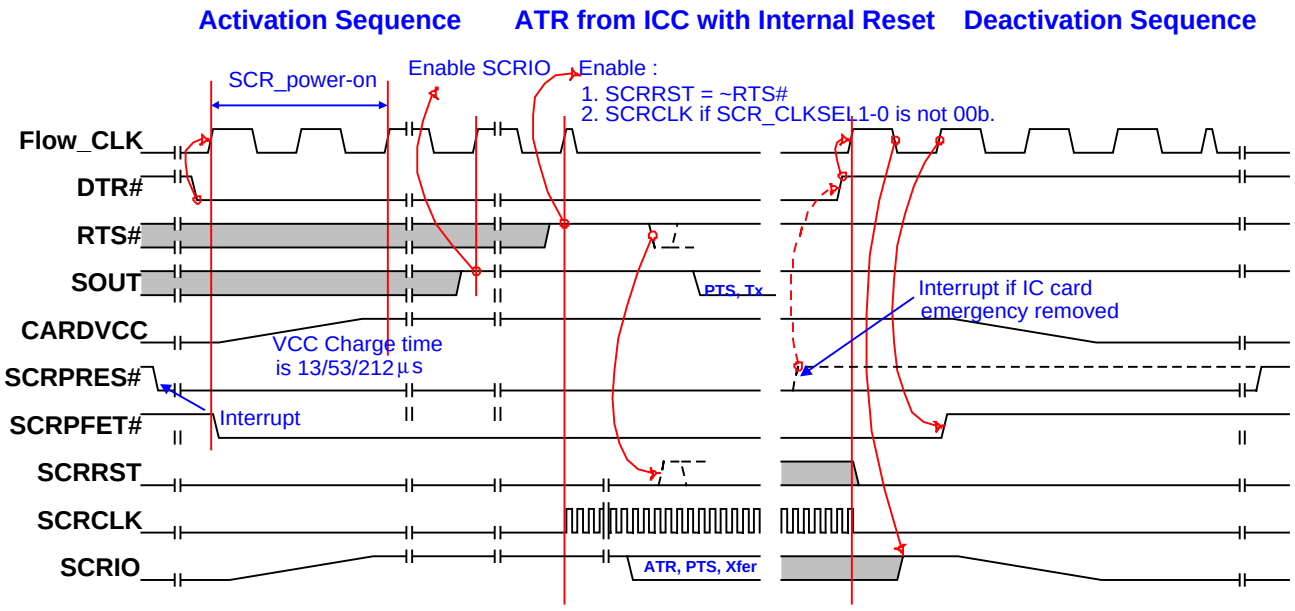


Figure 8-6. Waveform Example of IFD

- **Activation Sequence**

Refer to the waveform above. The SCR IFD in the IT8228E will make sure the IFD is in data receive mode (i.e. the SOUT from UART is high) and the RTS# should be programmed to high. The SCRCLK is then enabled to output to the IC card (which means that the IC card can count SCRCLK clock numbers to start ATR responses), the data transfer is then enabled, and the SCRRST is the inverse logic state of RTS#. Also, the operation procedure guarantees the correct activation sequence even if the driver cannot program the SCRCLK and SCRRST in the precise time points. In this way, the hardware meets the ICC specification.

- **ATR**

For the IC card with its own internal reset, its ATR begins within 400-40000 SCRCLK cycles. If no ATR is detected, the Smart Card IFD driver can then program the RTS# to low and cause the SCRRST to high.
For some types of IC cards without internal reset signals, it will check out the SCRRST as active low reset, and begins its ATR within 400-40000 SCRCLK cycles from the time point of SCRRST rising edge.
The IT8228E does not support the type of IC Card that may send synchronous ATRs.

- **Deactivation and PTS Structure**

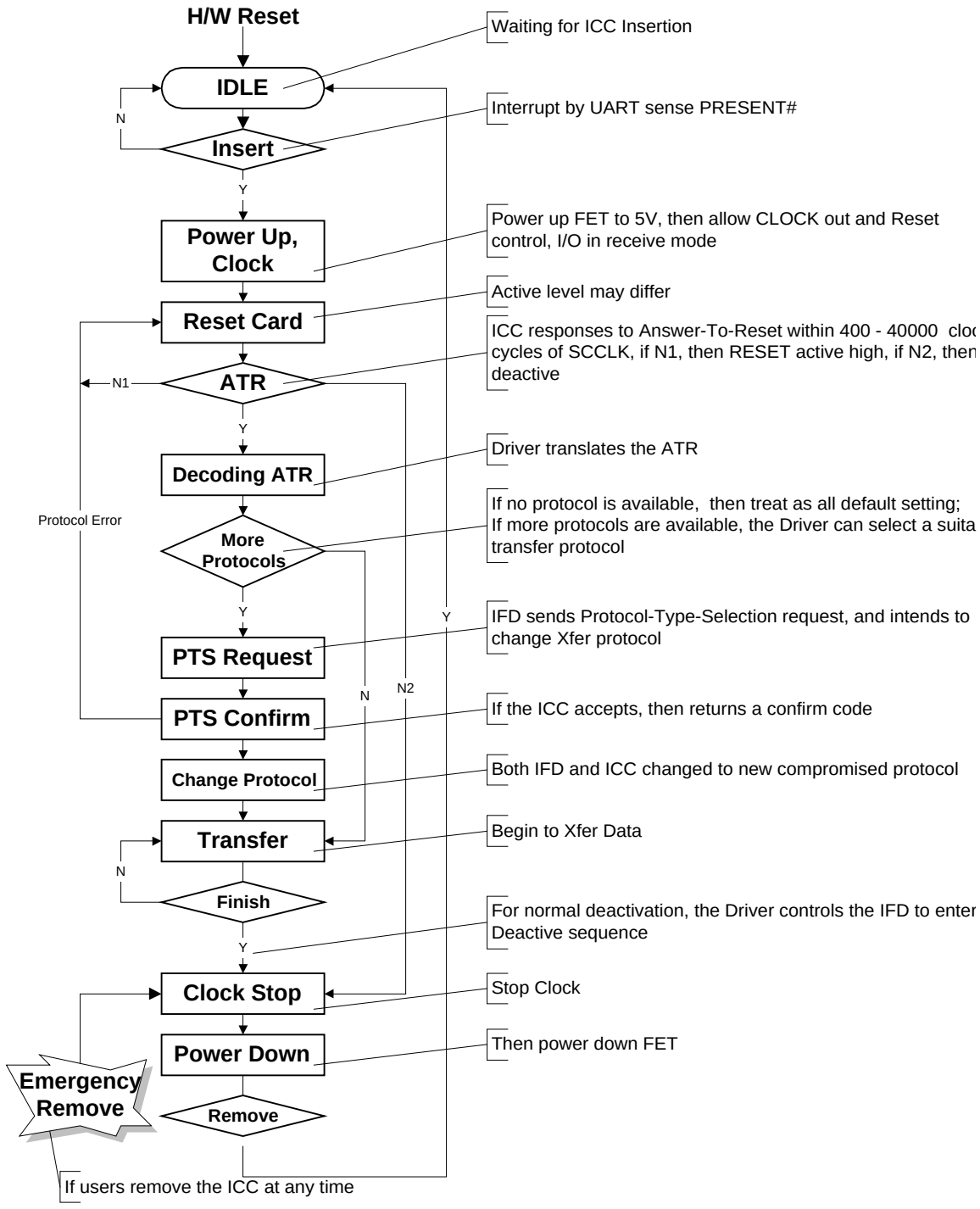
Whenever the IC card is removed or when the IFD driver intends to power off the SCR interface, the IFD will enter the deactivation sequence.

8.9.5 ATR and PTS Structure

The contents of the ATR (Answer-To-Reset) and PTS (Protocol-Type-Select) are defined in ISO/IEC 7816-X standard, which must be fully communicated by the ICC Resource manager, the ICC Service provider or the ICC application software.

After finalizing the coherent protocol, the SCR IFD enters the normal transfer mode. Since the SCRIO is the only data channel for both data transmit and receive as defined in the ICC Specification, the IT8228E can only support the half-duplex function. The SCRRST can be resent when a data transfer error occurs and then the IFD driver will select a safer, lower-speed protocol to perform the data transfer again.

8.9.6 Smart Card Operating Sequence Example



9. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage..... -0.5V to 3.6V

Input Voltage (Vi) ..... -0.5V to 5.5V

Output Voltage (Vo) ..... -0.5V to VCC + 0.3V

Operation Temperature (Topt)..... 0°C to +70°C

Storage Temperature..... -55°C to +125°C

Power Dissipation 100mW

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability

DC Electrical Characteristics (VCC = 3.3V ± 5%, Ta = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DO8 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -8 mA
DOD8 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
DO16 Buffer						
VOL	Low Output Voltage			0.4	V	I_{OL} = 16 mA
VOH	High Output Voltage	2.4			V	I_{OH} = -16 mA
DO24 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -24 mA
DIO8 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -8 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DIOD8 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	

DC Electrical Characteristics (VCC =3.3V ± 5%, Ta = 0°C to + 70°C) [cont'd]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DIO16 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -16 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DIOD16 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	µA	
DI Type Buffer						
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		µA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	µA	V_{IN} = VCC

10. AC Characteristics (VCC = 3.3V ± 5%, Ta = 0°C to + 70°C)

10.1 Clock Input Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock High Pulse Width when CLKIN=48 MHz[1]	8			nsec
t_2	Clock Low Pulse Width when CLKIN=48 MHz[1]	8			nsec
t_3	Clock Period when CLKIN=48 MHz[1]	20	21	22	nsec
t_4	Clock High Pulse Width when CLKIN=24 MHz[1]	18			nsec
t_5	Clock Low Pulse Width when CLKIN=24 MHz[1]	18			nsec
t_6	Clock Period when CLKIN=24 MHz[1]	40	42	44	nsec

Not tested. Guaranteed by design.

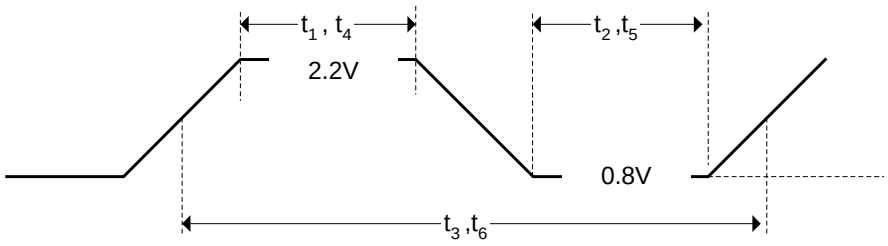


Figure 10-1. Clock Input Timings

10.2 LCLK (PCICLK) and LRESET Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			µsec

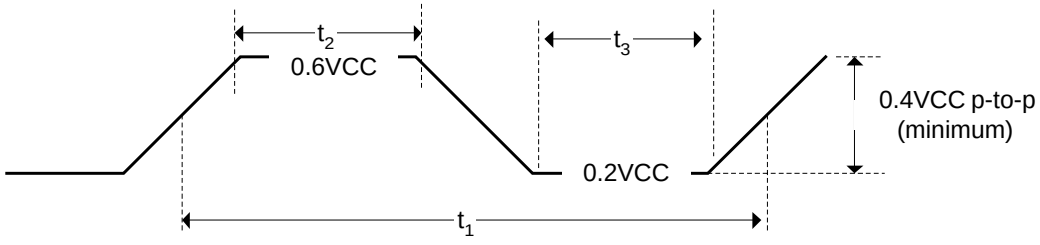


Figure 10-2. LCLK (PCICLK) and LRESET Timings

10.3 LPC and SERIRQ Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

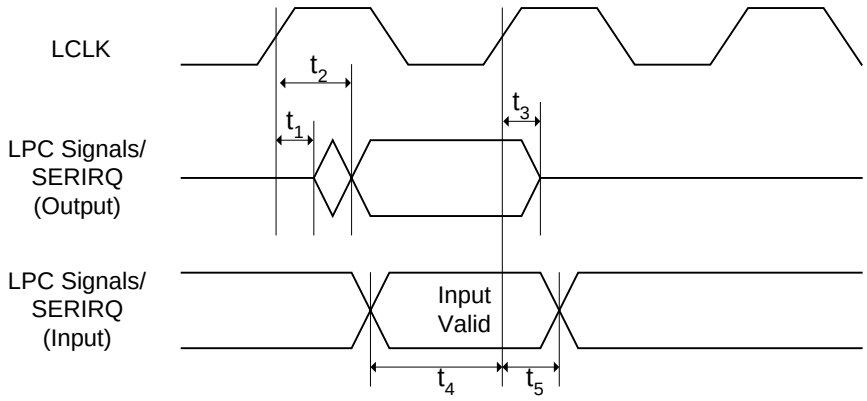
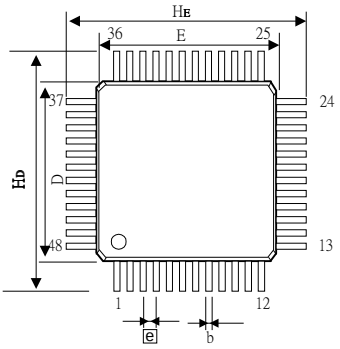
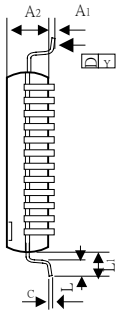


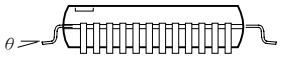
Figure 10-3. LPC and SERIRQ Timings

11. Package Information

LQFP 48 Outline Dimensions **Unit: inches/mm**







Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	-	0.008	0.09	-	0.20
D	0.274	0.276	0.278	6.95	7.00	7.05
E	0.274	0.276	0.278	6.95	7.00	7.05
e	0.02BSC			0.50BSC		
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039REF			1.00REF		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Note:
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
Total in excess of the b dimension at maximum material condition.
Dambar cannot be located on the lower radius of the foot.

12. Ordering Information

Part No.	Package
IT8228E	48 LQFP