INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8712F

Preliminary Environment Controller (EC)

Programming Guide V0.2

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1. Overview

The Environment Controller (EC), built in the IT8712F, includes eight voltage inputs, three temperature sensor inputs, three FANs' tachometer inputs, and three sets of advanced FAN Controllers. The EC monitors the hardware environment and implements environmental control for personal computer systems.

The IT8712F contains an 8-bit ADC (Analog-to-Digital Converter) responsible for monitoring the voltages and temperatures. The ADC converts the analog inputs, ranging from 0V to 4.096V, to 8-bit digital bytes. Thanks to the additional external components, the analog inputs are able to monitor different voltage ranges, in addition to monitoring the fixed input range of 0V to 4.096V. Through the external thermistors, the temperature sensor inputs can be converted to 8-bit digital bytes, enabling the sensor inputs, and monitoring the temperature around the thermistors or thermal diode. A built-in ROM is also provided to adjust the non-linear characteristics of thermistors.

FAN Tachometer inputs are digital inputs with an acceptable range of 0V to 5V, and are responsible for measuring the FAN's tachometer pulse periods. FAN_TAC1 and FAN_TAC2 are included with programmable divisors, and can be used to measure different fan speed ranges. FAN_TAC3 is included in the fixed divisor, and can only be used in the default range.

The EC of the IT8712F provides multiple internal registers and an interrupt generator for programmers to monitor the environment and control the FANs. Both the LPC bus and Serial Bus interfaces are supported to accommodate the various applications' needs.

2. Flow Chart

The coding flow chart of the voltage monitor of the EC is illustrated in Figure 2-1. The coding flow chart of the Temperature monitor of the EC flow charts is illustrated in Figure 2-2. The flow chart of the Fan monitor and control of the EC is illustrated in Figure 2-3.

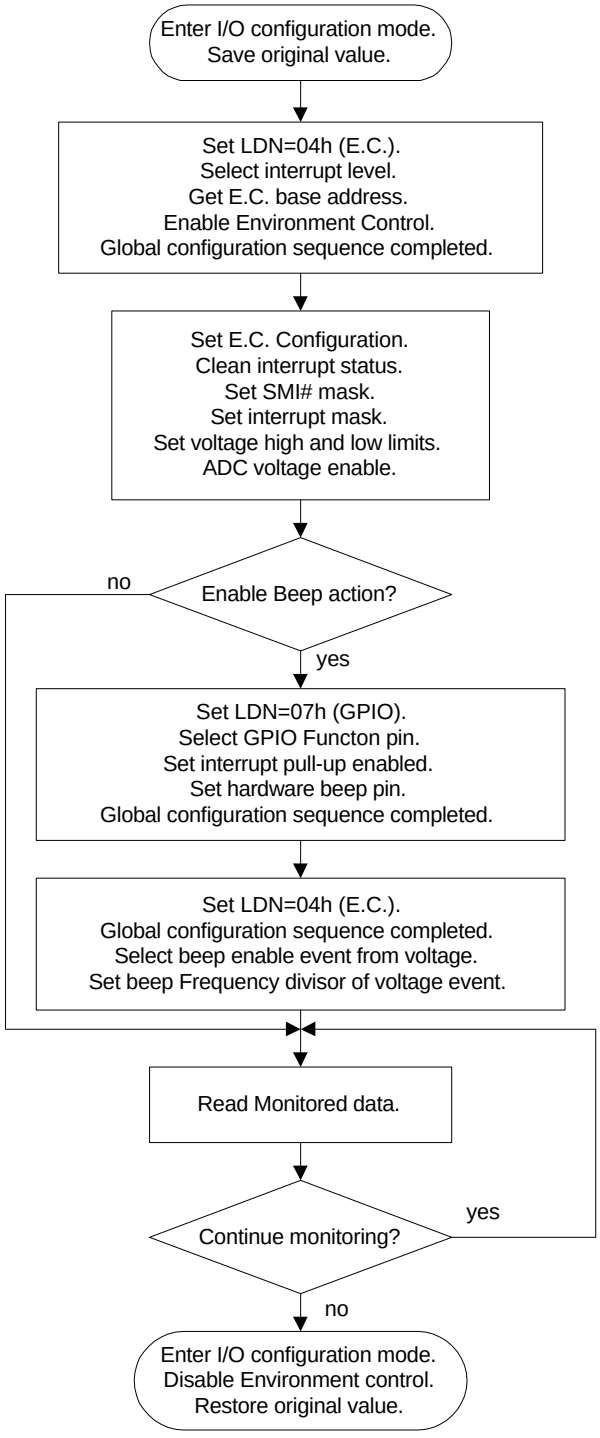

Figure 2-1. Voltage Monitor Control Flow Chart

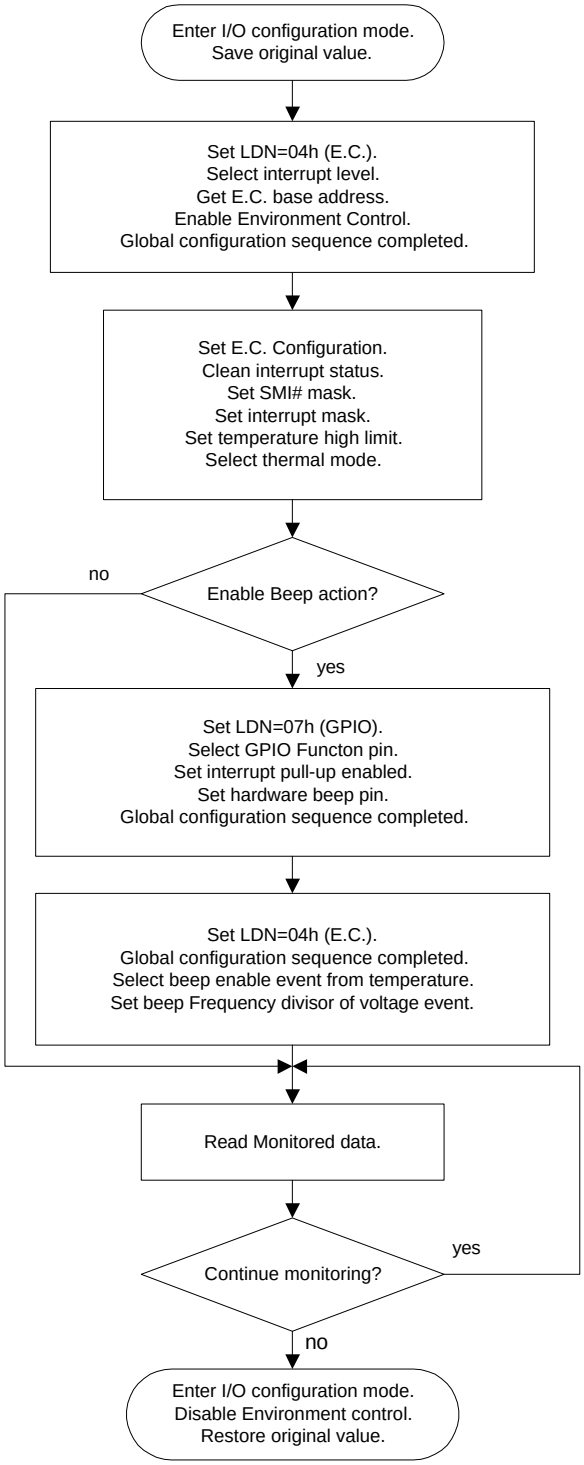

Figure 2-2. Temperature Monitor Control Flow Chart

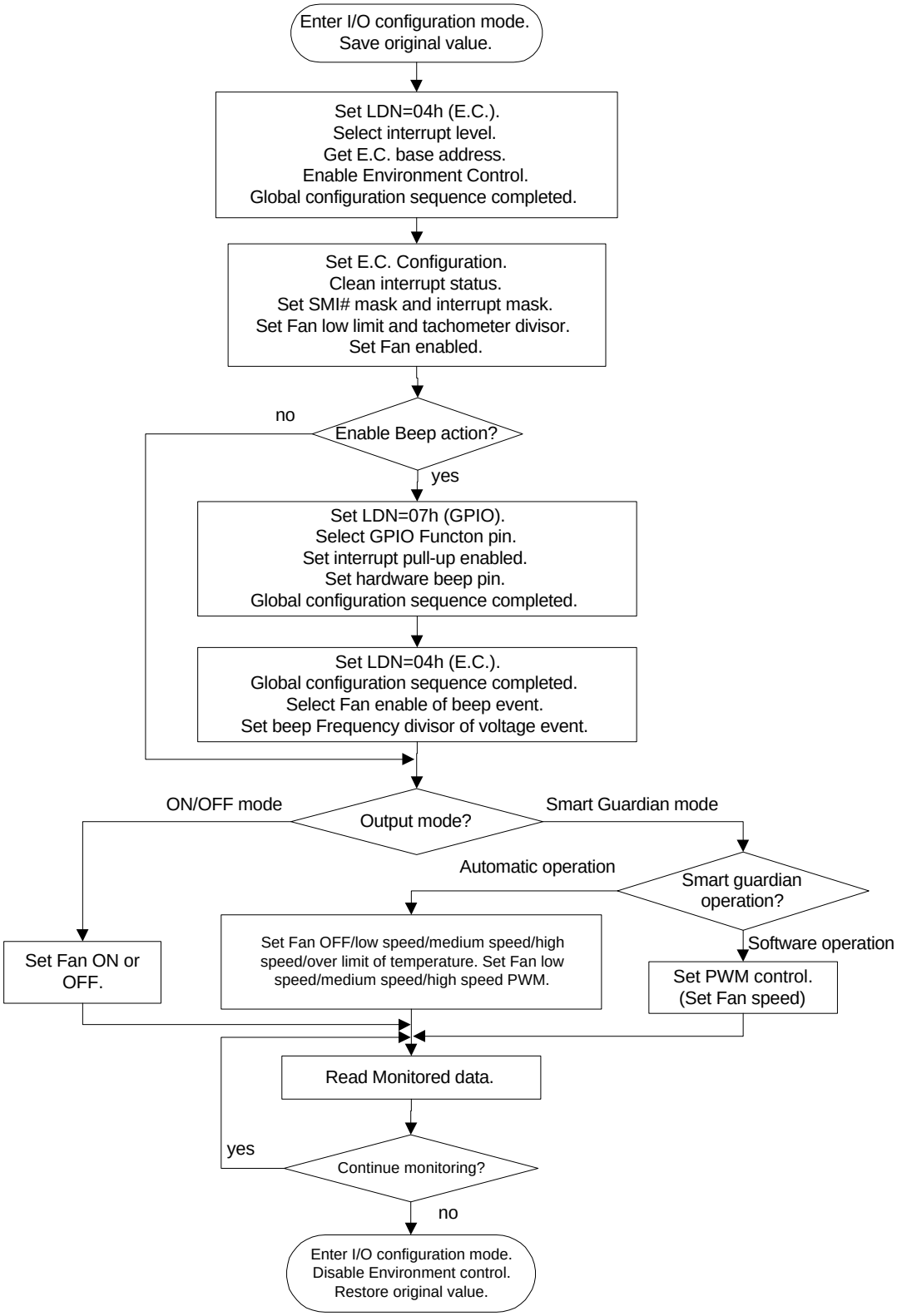

Figure 2-3. Fan Monitor Control Flow Chart

3. Programming Guide

a. Interfaces

The Environment Controller of the IT8712F decodes two addresses.

Table 3-1. Address Map on the LPC Bus

Register or Ports	Address
Address register of the EC	Base+05H
Data register of the EC	Base+06H

Note 1. The Base Address is determined by the Logical Device configuration registers of the Environment Controller (LDN=04h, registers index= 60h, 61h).

To access an EC register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

b. Set Configuration Registers:

The configuration registers must be set first: set LDN=04h for IT8712F. Activate the Environment Controller. Select the base address from Environment Controller Base Address MSB register (Index: 60h) and Base Address LSB register (Index=61h). Select the Environment Controller interrupt level from the register of Environment Controller Interrupt Level Select (Index=70h). Make sure to hook the operation system interrupt and create the interrupt service routine too.

Table 3-2. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	Environment Controller Activate.
04h	60h	R/W	03h	Environment Controller Base Address MSB Register.
04h	61h	R/W	10h	Environment Controller Base Address LSB Register.
04h	70h	R/W	0Bh	Environment Controller Interrupt Level Select.
04h	F0h	R/W	00h	Environment Controller Special Configuration Register.

c. Starting Conversion

The monitoring function in the EC is activated when the bit 3 of Configuration Register is cleared (low) and bit 0 of Configuration Register is set (high). Otherwise, several enable bits should be set to enable the monitoring function. Those enable bits are categorized into three groups: positive voltages, temperatures and FAN Tachometers. Before the EC monitoring function can be used, the steps below should be followed:

1. Set the Limits
2. Set the interrupt Masks
3. Set the Enable bits

The EC monitoring process can be then started.

Note 1. Please refer to Figure 2-1 (Voltage monitor control flow chart) to set the Voltage monitor of the hardware monitor controller.
Note 2. Please refer to Figure 2-2 (Temperature monitor control flow chart) to set the Temperature Controller/Monitor of the hardware monitor controller.
Note 3. Please refer to Figure 2-3 (Fan monitor control flow chart) to set the Fan Controller/Monitor of the hardware monitor controller.
Note 4. Please refer to Table 4-1 Global Configuration Registers and Table 4-2 GPIO Configuration Registers for GPIO setting.

d. Register Description:

1. Configuration Register (Index=00h, Default=18h)

Bit	R/W	Description
7	R/W	Initialization. A one restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is zero.
6	R/W	Update VBAT Voltage Reading
5	R/W	COPEN# cleared; Write 1 to clear COPEN#
4	R	Read Only, Always “1”
3	R/W	INT_Clear. A one disables the SMI# and IRQ outputs with the contents of interrupt status bits remain unchanged.
2	R/W	IRQ enables the IRQ Interrupt output
1	R/W	SMI# Enable. A one enables the SMI# Interrupt output.
0	R/W	Start. A one enables the startup of monitoring operations while a zero sends the monitoring operation in the STANDBY mode.

2. Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-6	R	Reserved
5	R	A one indicates a WTI# signal has been activated.
4	R	A one indicates a Case Open event has occurred.
3	R	Reserved
2-0	R	A one indicates the FAN_TAC3-1 Count limit has been reached.

3. Interrupt Status Register 2 (Index=02h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-0	R	A one indicates a High or Low limit of VIN7-0 has been reached.

4. Interrupt Status Register 3 (Index=03h, Ddfault=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	R	Reserved
2-0	R	A one indicates a High or Low limit of Temperature 3-1 has been reached.

5. SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7-6	R/W	Reserved
5	R/W	A one disables the WTI# Intrusion interrupt status bit for SMI#.
4	R/W	A one disables the Case Open Intrusion interrupt status bit for SMI#.
3	R/W	Reserved
2-0	R/W	A one disables the FAN_TAC3-1 interrupt status bit for SMI#.

6. SMI# Mask Register 2 (Index=05h, Default=00h)

Bit	R/W	Description
7-0	R/W	A one disables the VIN7-0 interrupt status bit for SMI#.

7. SMI# Mask Register 3 (Index=06h, Default=00h)

Bit	R/W	Description
7-3	R/W	Reserved
2-0	R/W	A one disables the Temperature 3-1 interrupt status bit for SMI#.

8. Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7-6	R/W	Reserved
5	R/W	A one disables the WTI# Intrusion interrupt status bit for IRQ.
4	R/W	A one disables the Case Open Intrusion interrupt status bit for IRQ.
3	R/W	Reserved
2-0	R/W	A one disables the FAN_TAC3-1 interrupt status bit for IRQ.

9. Interrupt Mask Register 2 (Index=08h, Default=00h)

Bit	R/W	Description
7-0	R/W	A one disables the VIN7-0 interrupt status bit for IRQ.

10. Interrupt Mask Register 3 (Index=09h, Default=00h)

Bit	R/W	Description
7-3	R/W	Reserved
2-0	R/W	A one disables the Temperature 3-1 interrupt status bit for IRQ.

11. VID Register (Index=0Ah)

Bit	R/W	Description
7-5	-	Reserved
4-0	R	VID4-0 inputs

12. Fan Tachometer Divisor Register (Index=0Bh, Default=09h)

Bit	R/W	Description
7-6	-	Reserved
5-3	R/W	FAN_TAC2 Counter Divisor. 000 – divided by 1; 100 – divided by 16; 001 – divided by 2; 101 – divided by 32; 010 – divided by 4; 110 – divided by 64; 011 – divided by 8; 111 – divided by 128.
2-0	R/W	FAN_TAC1 Counter Divisor. 000 – divided by 1; 100 – divided by 16; 001 – divided by 2; 101 – divided by 32; 010 – divided by 4; 110 – divided by 64; 011 – divided by 8; 111 – divided by 128.

13. Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	R	The number of counts of the internal clock per revolution.

14. Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R	Limit value.

15. Fan Controller Main Control Register (Index=13h, Default=00h)

Bit	R/W	Description
7	R	Reserved
6-4	R/W	FAN_TAC3-1 enable
3	R/W	Reserved
2-0	R/W	FAN_CTL3-1 output mode selection. 0: ON/OFF mode. 1: SmartGuardian mode

16. FAN_CTL Control Register (Index=14h, Default=00h)

Bit	R/W	Description
7	R	FAN_CTL Parity
6-3	R/W	Reserved
2-0	R/W	FAN_CTL3-1 ON/OFF mode control. These bits are only available when the relative output modes are selected in ON/OFF mode. 0: OFF. 1: ON

17. FAN_CTL1 PWM Control Register (Index=15h, Default=00h)

Bit	R/W	Description
7	R/W	FAN_CTL1 PWM mode Automatic/Software operation selection 0: Software operation 1: Automatic operation
6-0	R/W	128 steps of PWM control when in Software operation. (bit 7=0) or Temperature input selection when in Automatic operation. (bit 7=1) Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

18. FAN_CTL2 PWM Control Register (Index=16h, Default=00h)

Bit	R/W	Description
7	R/W	FAN_CTL2 PWM mode Automatic/Software operation selection 0: Software operation 1: Automatic operation
6-0	R/W	128 steps of PWM control when in Software operation. (bit 7=0) or Temperature input selection when in Automatic operation. (bit 7=1) Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

19. FAN_CTL3 PWM Control Register (Index=17h, Default=00h)

Bit	R/W	Description
7	R/W	FAN_CTL3 PWM mode Automatic/Software operation selection 0: Software operation 1: Automatic operation
6-0	R/W	128 steps of PWM control when in Software operation. (bit 7=0) or Temperature input selection when in Automatic operation. (bit 7=1) Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

20. VIN7-VIN0 Voltage Reading Registers (Index=27h-20h)

Bit	R/W	Description
7-0	R/W	Voltage Reading value

21. VBAT Voltage Reading Register (Index=28h)

Bit	R/W	Description
7-0	R/W	VBAT Voltage Reading value

22. TMPIN3-1 Temperature Reading Registers (Index=2Bh-29h)

Bit	R/W	Description
7-0	R/W	Temperature Reading value

23. VIN7-0 High Limit Registers (Index=3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h)

Bit	R/W	Description
7-0	R/W	High Limit value

24. VIN7-0 Low Limit Registers (Index=3Fh, 3Dh, 3Bh, 39h, 37h, 35h, 33h, 31h)

Bit	R/W	Description
7-0	R/W	Low Limit value

25. TMPIN3-1 High Limit Registers (Index=44h, 42h, 40h)

Bit	R/W	Description
7-0	R/W	High Limit value

26. TMPIN3-1 Low Limit Registers (Index=45h, 43h, 41h)

Bit	R/W	Description
7-0	R/W	Low Limit value

27. Serial Bus Interface Address Register (Index=48h, Default=2Dh)

Bit	R/W	Description
7	R/W	Reserved
6-0	R/W	Serial Bus Interface Address

28. ADC Voltage Channel Enable Register (Index=50h, Default=00h)

Bit	R/W	Description
7-0	R/W	ADC VIN7-VIN0 scan enable

29. ADC Temperature Channel Enable Register (Index=51h, Default=00h)

TMPIN3-1 cannot be enabled in both Thermal Resistor mode and Thermal Diode (Diode connected Transistor) mode.

Bit	R/W	Description
7-6	R/W	Reserved
5-3	R/W	TMPIN3-1 are enabled in Thermal Resistor mode.
2-0	R/W	TMPIN3-1 are enabled in Thermal Diode (or Diode connected Transistor) mode.

30. TMPIN3-1 Thermal Output Limit Registers (Index=54h-52h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Thermal Output Limit value.

31. Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	R	ITE Vendor ID. Read Only.

32. Thermal Diode Zero Degree Adjust Register (Index=59h, Default=56h)

This register is read-only unless the bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	Thermal Diode Zero Degree Voltage value (default: 0.664V 156h).

33. Beep Event Enable Register (Index=5Ch, Default=00h)

Bit	R/W	Description
7	R/W	Thermal Diode Zero Degree Adjust register write enable.
6-3	R/W	Reserved
2	R/W	Enables Beep action when TMPINs exceed limit.
1	R/W	Enables Beep action when VINs exceed limit.
0	R/W	Enables Beep action when FAN_TACs exceed limit.

34. Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone divisor. Tone=500/(bits[7:4]+1).
3-0	R/W	Frequency divisor. Frequency=10K/(bits[3:0]+1).

35. Beep Frequency Divisor of Voltage Event Register (Index=5Eh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone divisor. Tone=500/(bits[7:4]+1).
3-0	R/W	Frequency divisor. Frequency=10K/(bits[3:0]+1).

36. Beep Frequency Divisor of Temperature Event Register (Index=5Fh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone divisor. Tone=500/(bits[7:4]+1).
3-0	R/W	Frequency divisor. Frequency=10K/(bits[3:0]+1).

37. FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of OFF Registers (Index=70h, 68h, 60h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit value of Fan OFF.

38. FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Low Speed Registers (Index=71h, 69h, 61h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit value of Fan Low speed.

39. FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Medium Speed Registers (Index=72h, 6Ah, 62h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit value of Fan Medium speed.

40. FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of High Speed Registers (Index=73h, 6Bh, 63h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit value of Fan High speed.

41. FAN_CTL3-1 SmartGuardian Automatic Mode Over Temperature Limit Registers (Index=74h, 6Ch, 64h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Over Temperature Limit value.

42. FAN_CTL3-1 SmartGuardian Automatic Mode Low Speed PWM Registers (Index=75h, 6Dh, 65h, Default=00h)

Bit	R/W	Description
7	R/W	Reserved
6-0	R/W	PWM value of Low speed.

43. FAN_CTL3-1 SmartGuardian Automatic Mode Medium Speed PWM Registers (Index=76h, 6Eh, 66h, Default=00h)

Bit	R/W	Description
7	R/W	Reserved
6-0	R/W	PWM value of Medium speed.

44. FAN_CTL3-1 SmartGuardian Automatic Mode High Speed PWM Registers (Index=77h, 6Fh, 67h, Default=00h)

Bit	R/W	Description
7	R/W	Reserved
6-0	R/W	PWM value of High speed.

4. Operation

a. Power On RESET and Software RESET

When the system power is first applied, the EC performs a "power on reset" on the registers with default values (due to system hardware reset), and the EC will acquire a monitored value before it goes inactive. The ADC is active to monitor the VBAT pin and then goes inactive. Except the function of the Serial Bus Interface Address register, a software reset (bit 7 of Configuration register) is able to accomplish all the functions as the hardware reset does.

b. Voltage and Temperature Inputs

The 8-bit ADC has a 16mV LSB, with a 0V to 4.096V input range. The 2.5V and 3.3V supplies of PC applications can be directly connected to the inputs. The 5V and 12V inputs should be divided to the acceptable range. When the dividing circuit is used to measure the positive voltage, the recommended range for Ra and Rb is from 10KΩ to 100KΩ. The negative voltage can be measured by the same divider unless the divider is connected to VREF (constant voltage, 4.096V), not ground. The temperature measurement system of the EC converts the voltage of the TMPINs to 8-bit two's-complement. The system also includes an OP amp providing a constant voltage. It also additionally includes an external thermistor, a constant resistance, the ADC and a conversion table ROM.

Temperature	Digital Output Format	
	Binary	Hex
+ 125°C	01111101	7Dh
+ 25°C	00011001	19h
+ 1°C	00000001	01h
+ 0°C	00000000	00h
- 1°C	11111111	FFh
- 25°C	11100111	E7h
- 55°C	11001001	C9h

With the addition of the external application circuit, the actual voltages are calculated as below:

Positive Voltage: Vs = Vin X (Ra+Rb) / Rb
Negative Voltage: Vs = (1+Rin/Rf)XVin – (Rin/Rf)XVREF

All the analog inputs are equipped with the internal diodes that clamps the input voltage exceeding the power supply and ground. But, the limiting input current resistor is recommended when no dividing circuit is available.

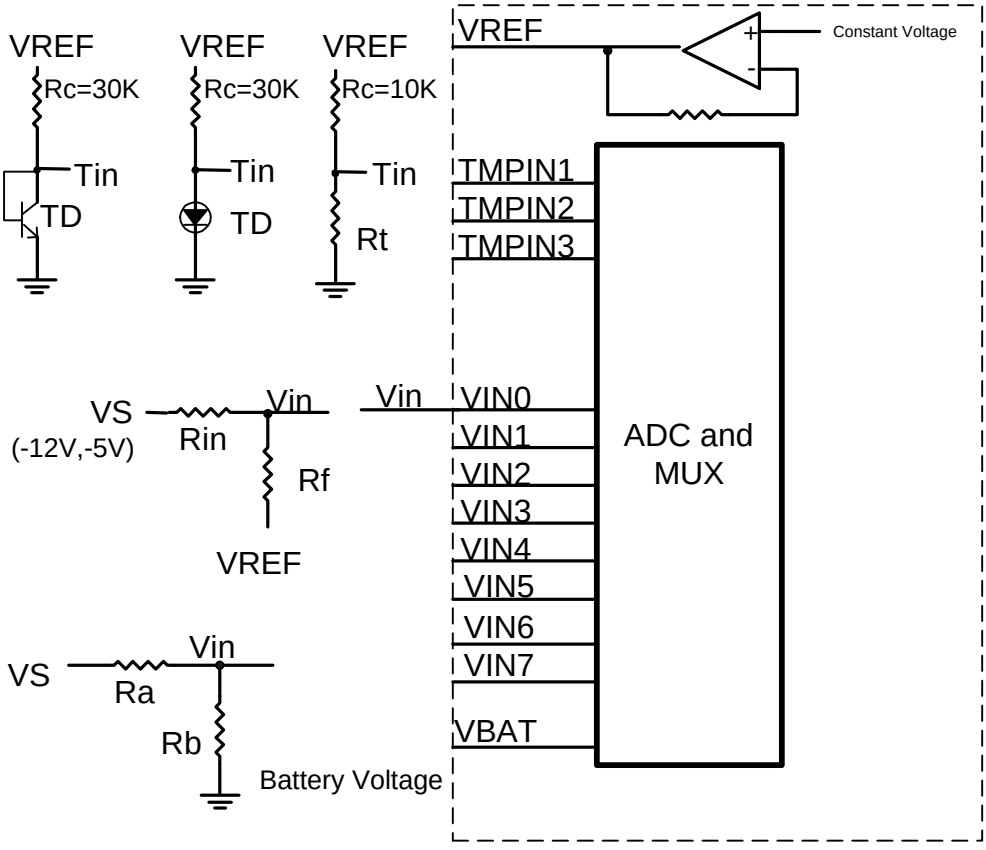

Figure 4-1. Application Example. Resistor should provide approximately 2V at the Analog Inputs

c. Layout and Grounding

A separate and low-impedance ground plane for analog ground is needed in achieving accurate measurement. The analog ground also provides a ground point for the voltage dividers including the temperature loops and analog components. Analog components such as voltage dividers, feedback resistors and the constant resistors of the temperature loops should be located as close as possible to the IT8712F. But, the thermistors of the temperature loops should be positioned at the measuring area. In addition, the power supply bypass, and the parallel combination of 10μF and 0.1μF bypass capacitors connected between VCC and analog ground, should also be located as close as possible to the IT8712F.

Due to the small differential voltage of thermal diode (diode connected transistor), there are many PCB layout's recommendations:
- Place the sensor as close as possible
- Ground of the sensor should be directly short to GNDA with excellent noise immunity
- Keep trace away from the noise source. (High voltage, fast data bus, fast clock, CRTs ..)
- Wider trace width (10mil at least) and guard ground (flanking and under) are recommended
- Place the noise filter and 0.1μF bypass capacitors as close to IT8712F as possible

d. Fan Tachometer

The Fan Tachometers gate a 22.5kHz clock into an 8-bit counter (maximum count=255) for one period of the input signals. Several divisors, located in VID/FAN Divisor Register, are provided for FAN_TAC1 and FAN_TAC2, and are used to modify the monitoring range. FAN_TAC3 is not adjustable, and its Divisor value is always set to 2. Counts are based on 2 pulses per revolution tachometer output.

RPM = 1.35 X 10^6 / (Count X Divisor)

The maximum input signal range is 0 to VCC. The additional application is needed to clamp the input voltage and current.

e. Interrupt of the EC

The EC generates interrupts as a result of each of its Limit registers on the analog voltage, temperature, and FAN monitor. All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled in the Configuration Register. The Interrupt Status Registers will be reset after being read. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. Due to slow monitoring sequence, the EC needs 1.5 seconds to allow all the Registers to be safely updated between completed read operations. When the bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume when this bit is cleared.

All the analog voltage inputs have high and low Limit Registers that generate Interrupts, except that the FAN monitoring inputs only have low Limit Register to warn the host. The IT8712F provides two modes dedicated to temperature interrupts in the EC: "Interrupt" mode and "Comparator" mode.

In "Interrupt" mode, an interrupt will be generated whenever the temperature exceeds Th limit, and the corresponding Interrupt status bits will be set to high until being reset by reading Interrupt Status Register. Once an interrupt event has occurred by crossing Th limit, then after being reset, an interrupt will only occur again when the temperature goes below TL limit. Again, it will set the status bit to high until being reset by reading the Interrupt Status Register.

When the TL limit register is set to 127°C, the temperature interrupts enter the **"Comparator" mode**. In this mode, an interrupt will be generated whenever the temperature exceeds the Th limit. The interrupt will also be cleared by reading the Interrupt Status Register, but the interrupt will be set again following the completion of another measurement cycle. It will remain set until the temperature goes below the Th limit.

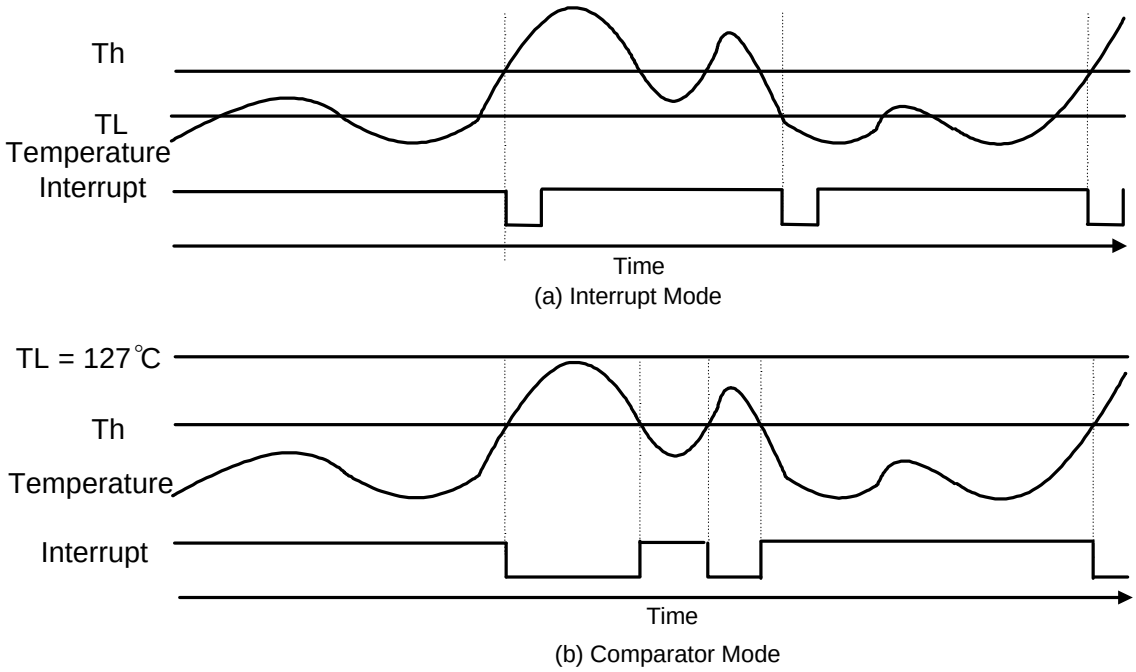

Figure 4-2. Temperature Interrupt Response Diagram

f. Fan Controller FAN_CTL's ON-OFF and SmartGuardian Modes

The IT8712F provides advanced FAN Controllers. Two modes are provided for each controller: ON_OFF and SmartGuardian modes. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application, the Fan's voltage values can be varied easily. There are also two mode options in the SmartGuardian mode: software and automatic modes. In the software mode, the PWM value is subject to the changes in the values of bits 6-0 of FAN_CTL PWM Control Registers (Index=15h, 16h, 17h). With the application circuit, FAN_CTL can generate 128 steps of voltage. So, the FAN_CTL1-3 PWM Control Registers can vary the voltage by changing the PWM value. Fan speed or other voltage control cooling device can be varied in 128 steps.

In the automatic mode, the PWM value is subject to the specific temperature inputs by five stages (OFF, Low Level, Medium Level, High Level and Full ON). The PWM values of the Low, Medium and High Levels are pre-loaded. Each of FAN's control sources (temperature inputs) can be any of the three temperature inputs, and are determined by bits 1-0 of FAN_CTL PWM Control Registers (Index=15h, 16h, 17h). When the source temperature is below the Low Temperature (Index=71h, 69h, 61h), the FAN_CTL output will enter OFF state. When the temperature is between Low and Medium Temperatures (Index=72h, 6Ah, 62h), the output will perform Low Level PWM; Medium Level PWM when between Medium and High Temperatures (Index=73h, 6Bh, 63h); High Level PWM when between the High and Over Temperatures (Index=74h, 6Ch, 64h). When any of the Over Temperatures is exceeded, all the FAN_CTL outputs will be full ON. The FAN_CTL output will not return to the OFF state until the source temperature goes below the OFF Temperature limit (Index=70h, 68h, 60h).

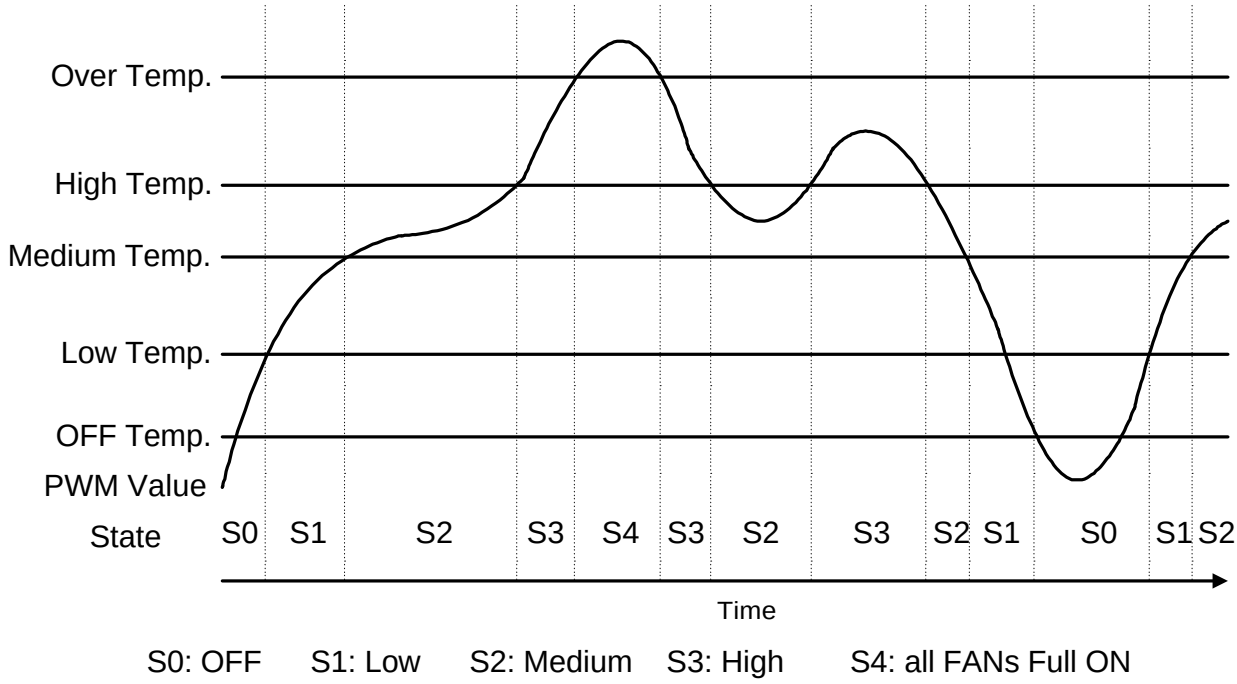

Figure 4-3. SmartGuardian Automatic Mode

Table 4-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number(LDN)
All	20h	R	87h	Chip ID Byte 1
All	21h	R	12h	Chip ID Byte 2
All	22h	R	00h	Chip Version
All	23h	R/W	00h	Clock Selection Register
All	24h	R/W	00h	Software Suspend
07h*	25h	R/W	00h	GPIO Set 1 Multi-Function Pin Selection Register
07h*	26h	R/W	00h	GPIO Set 2 Multi-Function Pin Selection Register
07h*	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
07h*	28h	R/W	00h	GPIO Set 4 Multi-Function Pin Selection Register
07h*	29h	R/W	00h	GPIO Set 5 Multi-Function Pin Selection Register
F4h*	2Eh	R/W	00h	Test 1 Register
F4h*	2Fh	R/W	00h	Test 2 Register

Note: *: All these registers can be read from all LDNs.

Table 4-2. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Registers or Action
07h	60h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
07h	61h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
07h	62h	R/W	00h	Simple I/O Base Address MSB Register
07h	63h	R/W	00h	Simple I/O Base Address LSB Register
07h	64h	R/W	00h	Panel Button De-bounce Base Address MSB Register
07h	65h	R/W	00h	Panel Button De-bounce Base Address LSB Register
07h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
07h	71h	R/W	00h	Watch Dog Timer Control Register
07h	72h	R/W	00h	Watch Dog Timer Configuration Register
07h	73h	R/W	00h	Watch Dog Timer Time-out Value Register
07h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
07h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
07h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
07h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
07h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
07h	B8h	R/W	00h	GPIO Set 1 Pin Internal Pull-up Enable Register
07h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
07h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
07h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
07h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
07h	C0h	R/W	00h	Simple I/O Set 1 Enable Register
07h	C1h	R/W	00h	Simple I/O Set 2 Enable Register
07h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
07h	C3h	R/W	00h	Simple I/O Set 4 Enable Register
07h	C4h	R/W	00h	Simple I/O Set 5 Enable Register
07h	C8h	R/W	00h	Simple I/O Set 1 Output Enable Register
07h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
07h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
07h	CBh	R/W	00h	Simple I/O Set 4 Output Enable Register
07h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register
07h	D0h	R/W	00h	Panel Button De-bounce Control Register
07h	D1h	R/W	00h	Panel Button De-bounce Set 1 Enable Register
07h	D2h	R/W	00h	Panel Button De-bounce Set 2 Enable Register
07h	D3h	R/W	00h	Panel Button De-bounce Set 3 Enable Register
07h	D4h	R/W	00h	Panel Button De-bounce Set 4 Enable Register
07h	D5h	R/W	00h	Panel Button De-bounce Set 5 Enable Register
07h	E3h	R/W	00h	IRQ3 External Routing Input Pin Mapping Register
07h	E4h	R/W	00h	IRQ4 External Routing Input Pin Mapping Register

Table 4-2. GPIO Configuration Registers (continued)

LDN	Index	R/W	Reset	Configuration Registers or Action
07h	E5h	R/W	00h	IRQ5 External Routing Input Pin Mapping Register
07h	E6h	R/W	00h	IRQ6 External Routing Input Pin Mapping Register
07h	E7h	R/W	00h	IRQ7 External Routing Input Pin Mapping Register
07h	E9h	R/W	00h	IRQ9 External Routing Input Pin Mapping Register
07h	EAh	R/W	00h	IRQ10 External Routing Input Pin Mapping Register
07h	Ebh	R/W	00h	IRQ11 External Routing Input Pin Mapping Register
07h	ECh	R/W	00h	IRQ12 External Routing Input Pin Mapping Register
07h	EEh	R/W	00h	IRQ14 External Routing Input Pin Mapping Register
07h	EFh	R/W	00h	IRQ15 External Routing Input Pin Mapping Register
07h	F0h	R/W	00h	SMI# Control Register 1
07h	F1h	R/W	00h	SMI# Control Register 2
07h	F2h	R/W	00h	SMI# Status Register 1
07h	F3h	R/W	00h	SMI# Status Register 2
07h	F4h	R/W	00h	SMI# Pin Mapping Register
07h	F5h	R/W	00h	Hardware Monitor Thermal Output Pin Mapping Register
07h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
07h	F7h	R/W	00h	Keyboard Lock Pin Mapping Register
07h	F8h	R/W	00h	GP LED Blinking 1 Pin Mapping Register
07h	F9h	R/W	00h	GP LED Blinking 1 Control Register
07h	FAh	R/W	00h	GP LED Blinking 2 Pin Mapping Register
07h	FBh	R/W	00h	GP LED Blinking 2 Control Register

INTEGRATED TECHNOLOGY EXPRESS, INC. TERMS AND CONDITIONS OF SALE(Rev: May98)

These Terms and Conditions of Sale apply to all items designed, sold and/or made by Integrated Technology Express, Inc. ("ITE Taiwan") and/or Integrated Technology Express, Inc. ("ITE California"), and Buyer agrees they apply to all such items.

0. PARTIES

ITE Taiwan is a company headquartered in the Republic of China, Taiwan, and incorporated under Taiwan law, and ITE California is a separate company incorporated under California law and headquartered in California. These two companies are independent, and, except as to the entity which invoices for goods delivered to it, Buyer holds no rights against and has no commitments from ITE California and/or ITE Taiwan. Subject to the foregoing, "Seller" refers to the entity which invoices Buyer for product, provided however that both ITE Taiwan and ITE California shall each be entitled to claim protection under paragraphs 4(b)-4(f), 5, 8, 9, 10, 11, 12 and 13 below.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Taiwan (if Seller is ITE Taiwan or ITE California) or Santa Clara, California (if Seller is ITE California).
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.
(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

(a) The contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).
(b) In no event will Buyer have rights in partially completed goods.

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under this purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.
Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in a writing signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed where Seller is ITE Taiwan by the laws of Taiwan, Republic of China or, where Seller is ITE California, by the laws of California and the United States of America, in either event without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under U.S. law or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under U.S. laws and regulations.

12. JURISDICTION AND VENUE

Where Seller is ITE Taiwan, the courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Where Seller is ITE California, the courts located in Santa Clara County, California, USA, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.

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