PRELIMINARY

Dual High Speed MOSFET/IGBT Drivers T-52-13-90

IXLD4423/4424/4425
• 3 A Peak Drive Current

IXLD4426/4427/4428
• 1.5 A Peak Drive Current

General Description

The IXLD4423-28 family of buffer/drivers are CMOS devices which are durable, efficient and easy to use. They are improved versions of the earlier IXLD426/427/428 family of buffer/drivers (with which they are pin-compatible) and are capable of giving reliable service in far more demanding electrical environments: They will not latch under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking, of either polarity, occurs on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (of either polarity) being forced back into their outputs. All terminals are also fully protected against up to 2KV of Electro-static discharge.

In addition, we use a custom-developed molding epoxy for our plastic packages which, in tests, produced 0 device failures after 10,000 hours in an 85°C-85% R.H. environment, and contains 50% less Sodium and Chlorine contamination than standard commercial compounds, which increase device lifetimes.

As a result, the IXLD4423-28 series drivers are much easier to use, more flexible in operation, and much more forgiving than any other driver, CMOS or bipolar, currently available. Because they are fabricated in CMOS, they dissipate a minimum of power, and provide rail-to-rail voltage swings to better insure the logic state of any load they are driving.

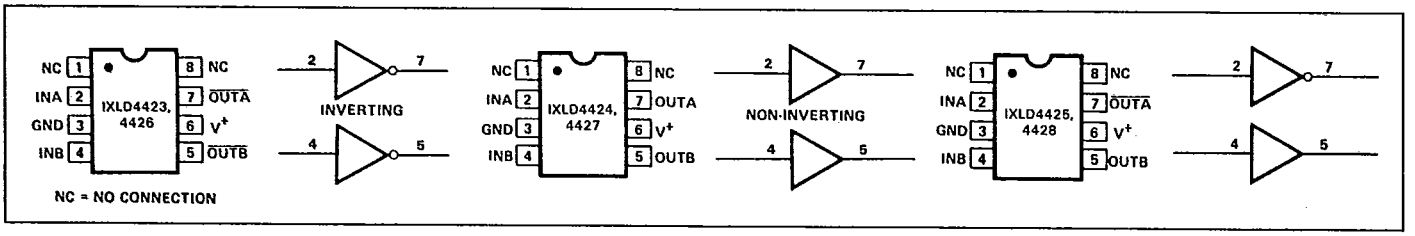
Although primarily intended for driving power MOSFETs and IGBTs, the 4423-28 series drivers are equally well suited to driving any other load (capacitive, resistive, or inductive) which requires a low-impedance driver capable of high peak currents and fast switching times. For example, heavily loaded clock lines, coaxial cables, or piezoelectric transducers all can be driven from the IXLD4423-28. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the packages.

As MOSFET/IGBT drivers, the IXLD4426-28 can easily switch 1000pf gate capacitances in under 30nsec, and provide low enough impedances in both the ON and OFF states to assure that a MOSFET/IGBT's intended state will not be affected even by large transients. The IXLD4423-25 can drive 1800pf gate capacitance in under 30nS.

Features

- Latch Up Protected. Withstand >500mA Reverse Current
- Input Will Withstand Negative Inputs up to −5V
- ESD Protected 2KV
- High Peak Output Current (4423-25) .... 3.0 A Peak
  (4426-28) .....1.5 A Peak
- Wide Operating Range ..... 4.5 V to 18 V
- High Capacitive Load Drive Capability (4423-25) 1800 pF in 25 nS
  (4426-28) 1000 pF in 25 nS
- Low Delay Time ..... <40 nS Typ.
- Consistent Delay Times with Changes in Supply Voltage
- Matched Rise and Fall Times
- Logic High Input for Any Voltage from 2.4 V to V_S^+
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - with Logic 1 Input (4423-25) ..... 1.5 mA
    (4426-28) ..... 3.5 mA
  - with Logic 0 Input (4423-25) ..... 150 µA
    (4426-28) ..... 350 µA
- Low Output Impedance (4423-25) ..... 2.8 Ω
  (4426-28) ..... 7 Ω
- Output Voltage Swing to Within 25 mV of Ground or V_S^+
- Pin-Out Same as IXLD426-428
- Available in Inverting & Non-Inverting Configurations

Pin Configuration



Applications

- Switch Mode Power Supplies
- CCD Drivers
- Pulse Transformer Drivers
- Class D Switching Amplifiers
- Motor Controls
- Print Hard Drive
- Tungsten Lamp Driver
- Capacitive, Resistive or Inductive Load Drive

IXLD4423-28

Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

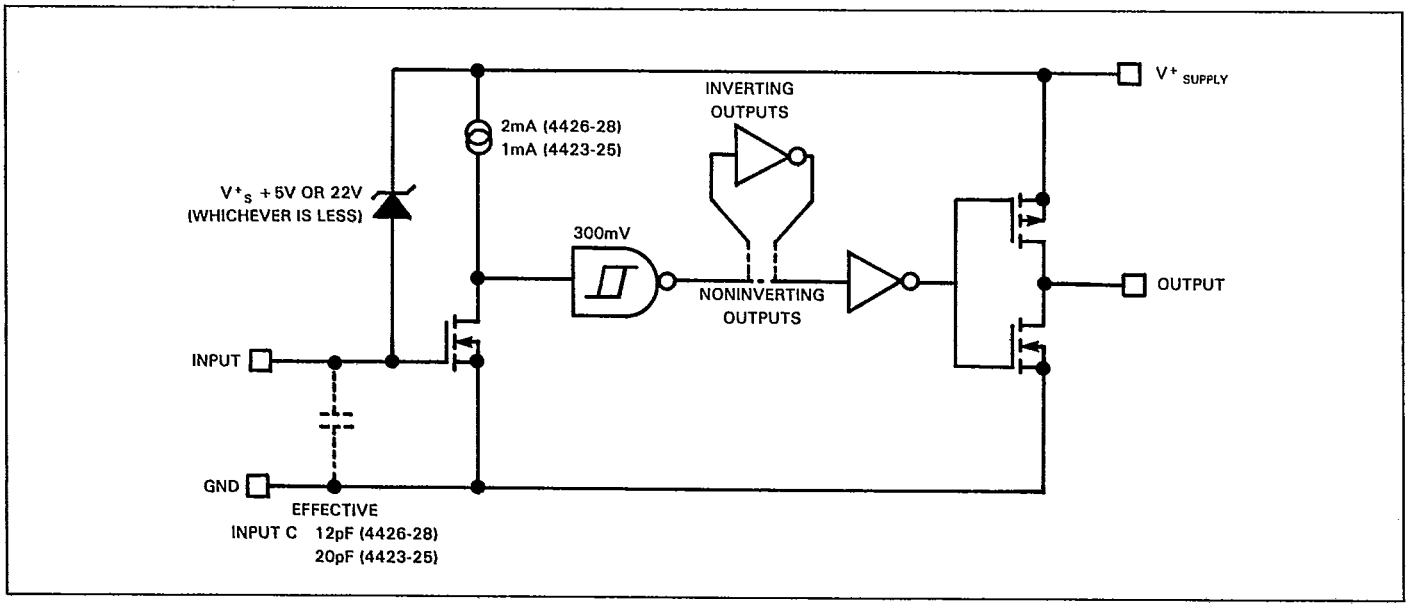
Ordering Information

Part No.	Package	Temperature Range
IXLD4423COE	16-Pin SO Wide	0°C to +70°C
IXLD4423CPA	8-Pin Plastic DIP	0°C to +70°C
IXLD4423IJA	8-Pin CerDIP	−25°C to +85°C
IXLD4423MJA	8-Pin CerDIP	−55°C to +125°C
IXLD4423MJA/883	8-Pin CerDIP	−55°C to +125°C
IXLD4424COE	16-Pin SO Wide	0°C to +70°C
IXLD4424CPA	8-Pin Plastic DIP	0°C to +70°C
IXLD4424IJA	8-Pin CerDIP	−25°C to +85°C
IXLD4424MJA	8-Pin CerDIP	−55°C to +125°C
IXLD4424MJA/883	8-Pin CerDIP	−55°C to +125°C
IXLD4425COE	16-Pin SO Wide	0°C to +70°C
IXLD4425CPA	8-Pin Plastic DIP	0°C to +70°C
IXLD4425IJA	8-Pin CerDIP	−25°C to +85°C
IXLD4425MJA	8-Pin CerDIP	−55°C to +125°C
IXLD4425MJA/883	8-Pin CerDIP	−55°C to +125°C

Part No.	Package	Configuration	Temperature Range
IXLD4426COA	8-Pin SO		0°C to +70°C
IXLD4426CPA	8-Pin Plastic DIP		0°C to +70°C
IXLD4426IJA	8-Pin CerDIP		−25°C to +85°C
IXLD4426MJA	8-Pin CerDIP		−55°C to +125°C
IXLD4426MJA/883	8-Pin CerDIP		−55°C to +125°C
IXLD4427COA	8-Pin SO		0°C to +70°C
IXLD4427CPA	8-Pin Plastic DIP		0°C to +70°C
IXLD4427IJA	8-Pin CerDIP		−25°C to +85°C
IXLD4427MJA	8-Pin CerDIP		−55°C to +125°C
IXLD4427MJA/883	8-Pin CerDIP		−55°C to +125°C
IXLD4428COA	8-Pin SO		0°C to +70°C
IXLD4428CPA	8-Pin Plastic DIP		0°C to +70°C
IXLD4428IJA	8-Pin CerDIP		−25°C to +85°C
IXLD4428MJA	8-Pin CerDIP		−55°C to +125°C
IXLD4428MJA/883	8-Pin CerDIP		−55°C to +125°C

* For devices with 125°C, 160 Hour Burn In add /BI to part number suffix.

Functional Diagram



Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

IXLD4423-4428

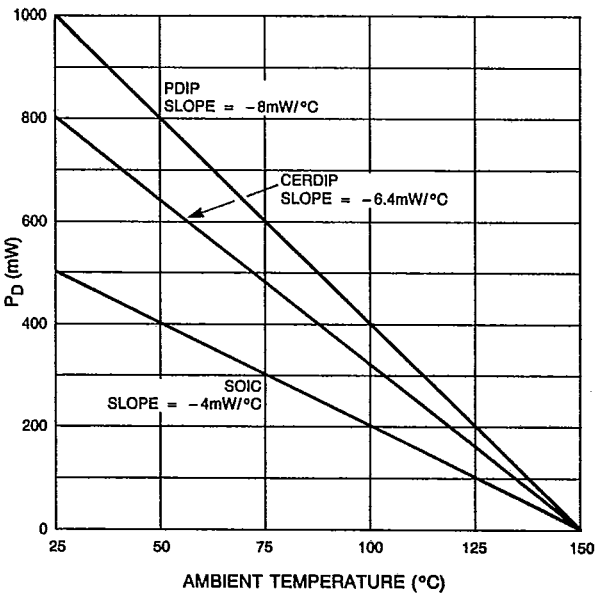
Absolute Maximum Ratings (Notes 1, 2, 3)

Power Dissipation
- SOIC ..... 500 mW
- CerDIP ..... 800 mW
- PDIP ..... 1000 mW

Supply Voltage ..... 20 V
Input Voltage Any Terminal ..... Vs + 0.8 V to Ground −5.0 V
Operating Temperature
- M Version ..... −55°C to +125°C
- I Version ..... −25°C to +85°C
- C Version ..... 0°C to +70°C

Maximum Junction Temperature ..... +150°C
Storage Temperature ..... −55°C to +150°C
Lead Temperature (10 Sec) ..... 300°C
Package Thermal Resistance
- PDIP θ_{JA} ..... 125°C/W
- PDIP θ_{JC} ..... 42°C/W
- CerDIP θ_{JA} ..... 150°C/W
- CerDIP θ_{JC} ..... 50°C/W
- SOIC θ_{JA} ..... 250°C/W
- SOICθ_{JC} ..... 75°C/W

Package Power Dissipation



IXLD4423/4424/4425 Electrical Characteristics:

T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	$0 \leq V_{IN} \leq V_S$	−1	—	1	µA
OUTPUT	V_{OH}	High Output Voltage		V_S−0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance HI State	I_{OUT} = 10 mA, V_S = 18V	—	2.8	5	Ω
	R_O	Output Resistance LO State	I_{OUT} = 10 mA, V_S = 18V	—	3.5	5	Ω
	I_{PK}	Peak Output Current		—	3	—	A
	I	Latch-Up Protection Withstand Reverse Current		>500	—	—	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 1800 pF	—	23	35	nS
	T_F	Fall Time	Test Figure 1, C_L = 1800 pF	—	25	35	nS
	T_{D1}	Delay Time	Test Figure 1, C_L = 1800 pF	—	33	75	nS
	T_{D2}	Delay Time	Test Figure 1, C_L = 1800 pF	—	38	75	nS
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	1.5	2.5	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	150	250	µA

IXLD4423-4428

Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

IXLD4423/4424/4425 Electrical Characteristics:

Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−10	—	10	μA
OUTPUT	V_{OH}	High Output Voltage		V_S−0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance	Hi State I_{OUT} = 10 mA, V_S = 18 V	—	3.7	8	Ω
	R_O	Output Resistance	Low State I_{OUT} = 10 mA, V_S = 18 V	—	4.3	8	Ω
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 1800 pF	—	28	60	nS
	T_F	Fall Time	Test Figure 1, C_L = 1800 pF	—	32	60	nS
	T_{D1}	Delay Time	Test Figure 1, C_L = 1800 pF	—	32	100	nS
	T_{D2}	Delay Time	Test Figure 1, C_L = 1800 pF	—	38	100	nS
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	2.0	3.5	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	200	300	μA

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Switching Time Test Circuits

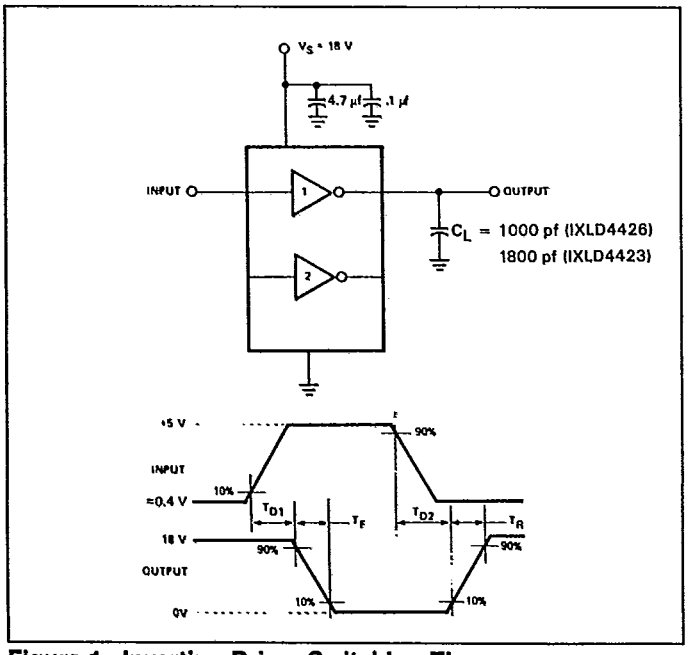


Figure 1: Inverting Driver Switching Time

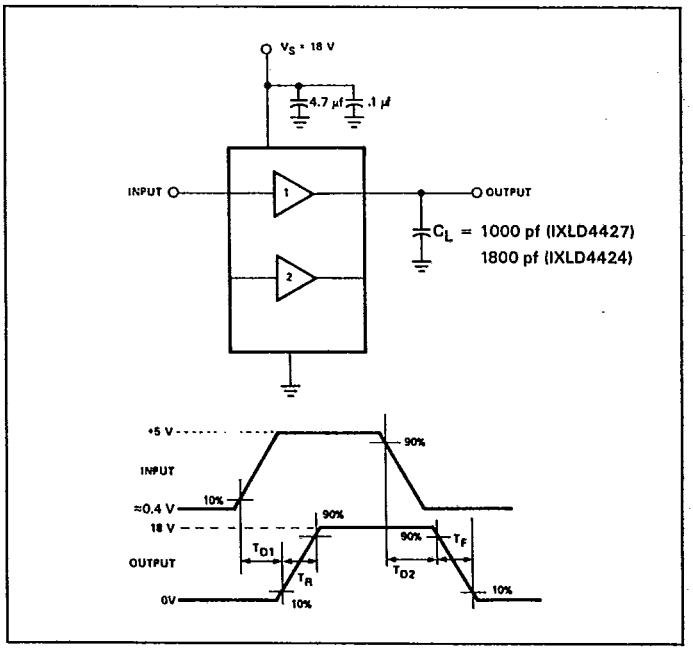


Figure 2: Non-Inverting Driver Switching Time

Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

IXLD4426/4427/4428 Electrical Characteristics:

Specifications measured at T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	SYMBOL	PARAMETER	CONDITIONS	IXLD4426 MIN	IXLD4426 TYP	IXLD4426 MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	–1	—	1	µA
OUTPUT	V_{OH}	High Output Voltage		V_S–0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance	Hi State I_{OUT} = 10 mA, V_S = 18V	—	7	10	Ω
	R_O	Output Resistance	Low State I_{OUT} = 10 mA, V_S = 18V	—	7	10	Ω
	I_{PK}	Peak Output Current		—	1.5	—	A
	I	Latch-Up Protection Withstand Reverse Current		>500	—	—	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 1000 pF	—	25	30	ns
	T_F	Fall Time	Test Figure 1, C_L = 1000 pF	—	25	30	ns
	T_{D1}	Delay Time	Test Figure 1, C_L = 1000 pF	—	—	30	ns
	T_{D2}	Delay Time	Test Figure 1, C_L = 1000 pF	—	—	50	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	3.5	4.5	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	0.35	0.4	mA

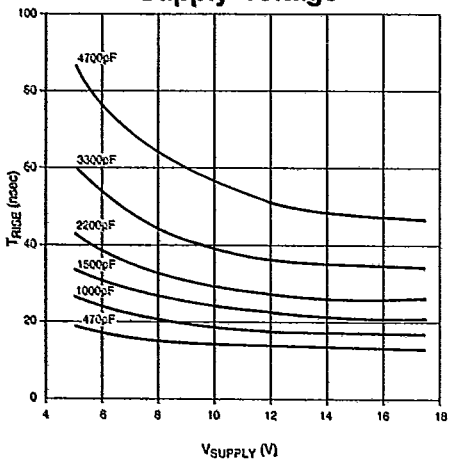
IXLD4426/4427/4428 Electrical Characteristics:

Specifications measured over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

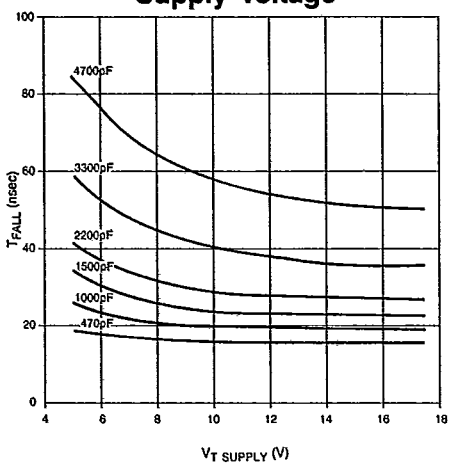
TYPE	SYMBOL	PARAMETER	CONDITIONS	IXLD4426 MIN	IXLD4426 TYP	IXLD4426 MAX	UNIT
INPUT	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	–1	—	1	µA
OUTPUT	V_{OH}	High Output Voltage		V_S–0.025	—	—	V
	V_{OL}	Low Output Voltage		—	—	0.025	V
	R_O	Output Resistance	Hi State I_{OUT} = 10 mA, V_S = 18V	—	9	12	Ω
	R_O	Output Resistance	Low State I_{OUT} = 10 mA, V_S = 18V	—	9	12	Ω
	I_{PK}	Peak Output Current		—	1.5	—	A
	I	Latch-Up Protection Withstand Reverse Current		>500	—	—	mA
SWITCHING TIME	T_R	Rise Time	Test Figure 1, C_L = 1000 pF	—	—	40	ns
	T_F	Fall Time	Test Figure 1, C_L = 1000 pF	—	—	40	ns
	T_{D1}	Delay Time	Test Figure 1, C_L = 1000 pF	—	—	40	ns
	T_{D2}	Delay Time	Test Figure 1, C_L = 1000 pF	—	—	60	ns
POWER SUPPLY	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8	mA
	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

Typical Characteristic Curves (IXLD4423/24/25)

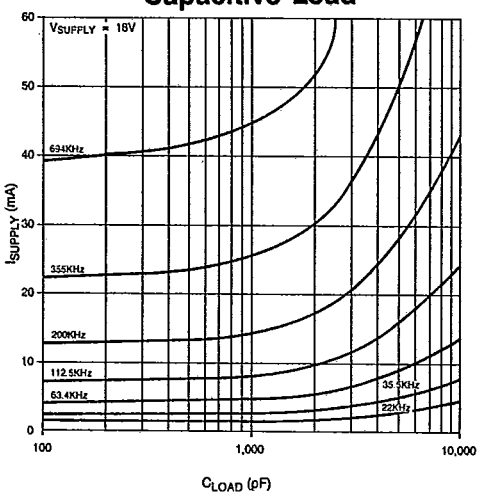
Rise Time vs Supply Voltage



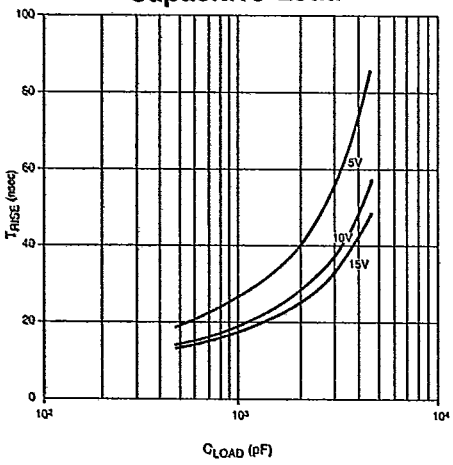
Fall Time vs Supply Voltage



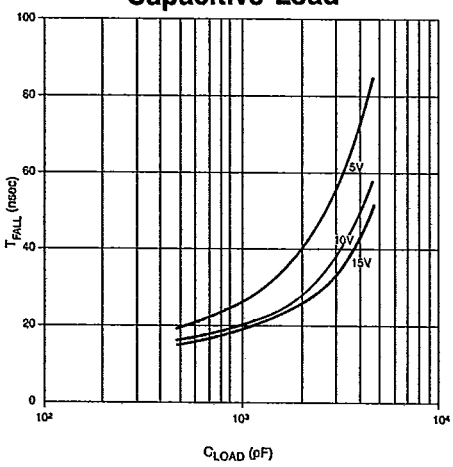
Supply Current vs Capacitive Load



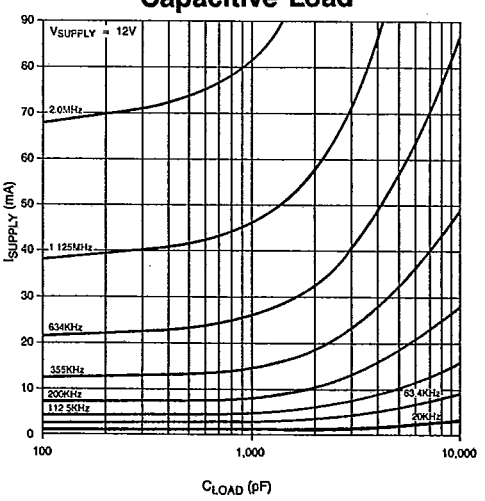
Rise Time vs Capacitive Load



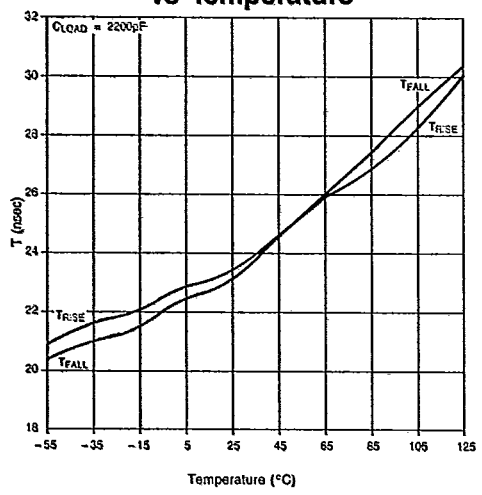
Fall Time vs Capacitive Load



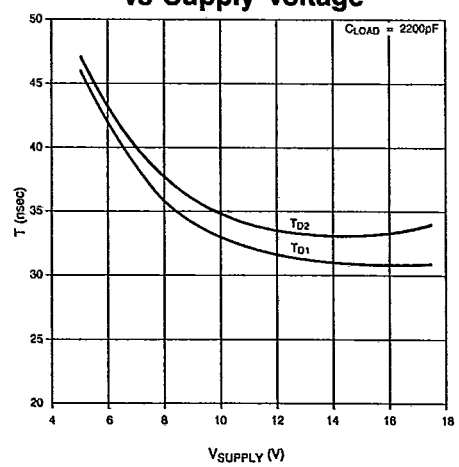
Supply Current vs Capacitive Load



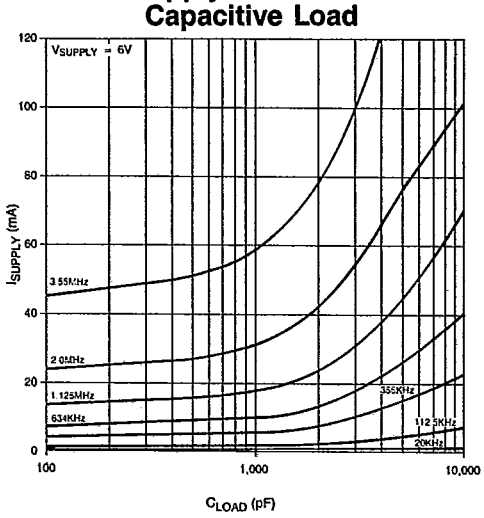
Rise and Fall Time vs Temperature



Propagation Delay Time vs Supply Voltage



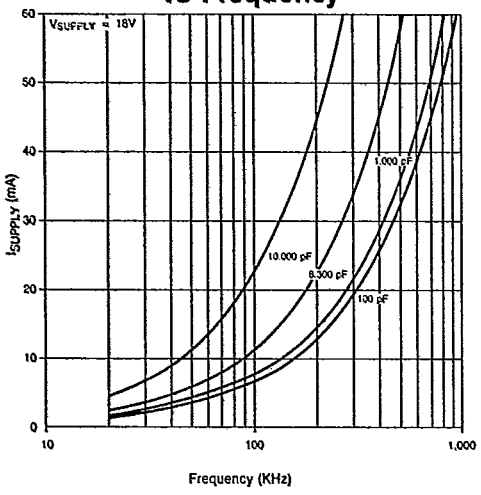
Supply Current vs Capacitive Load



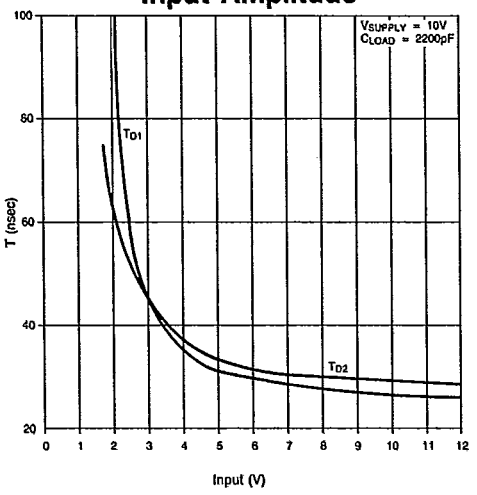
Dual High Speed MOSFET/IGBT Drivers
1.5A/3.0A Peak Drive Current

Typical Characteristic Curves (IXLD4423/24/25) (Continued)

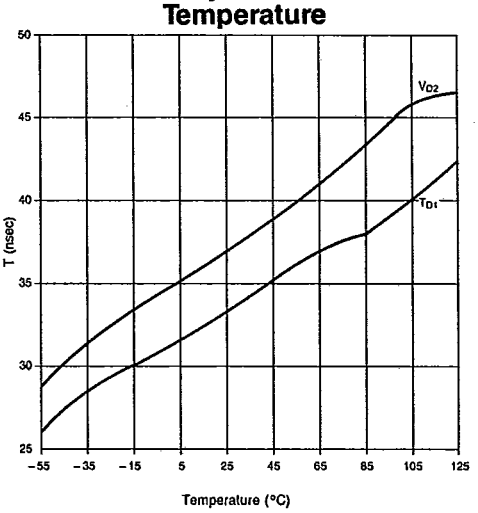
Supply Current vs Frequency



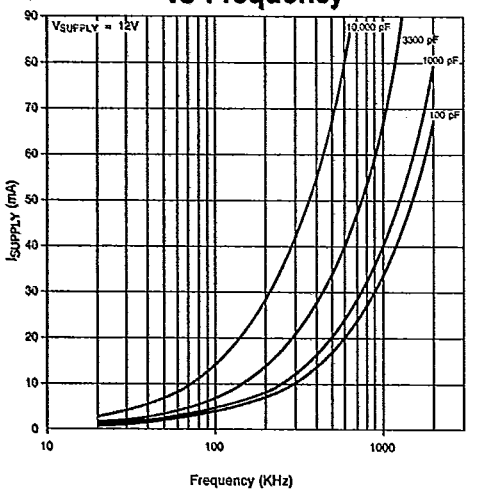
Propagation Delay vs Input Amplitude



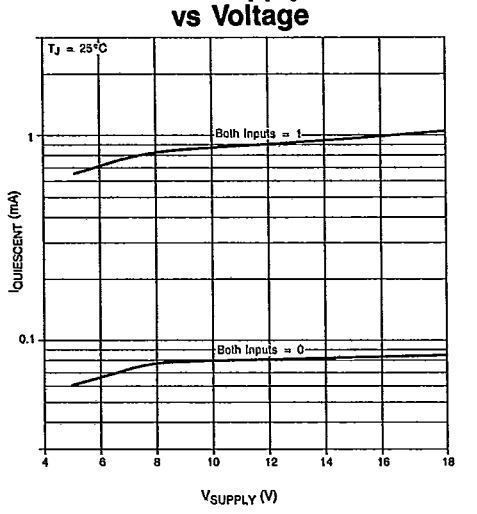
Delay Time vs Temperature



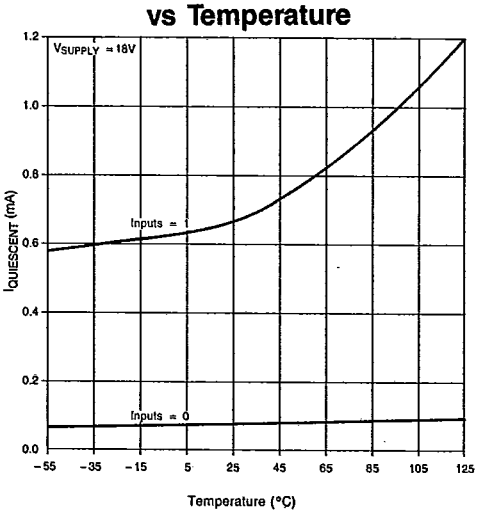
Supply Current vs Frequency



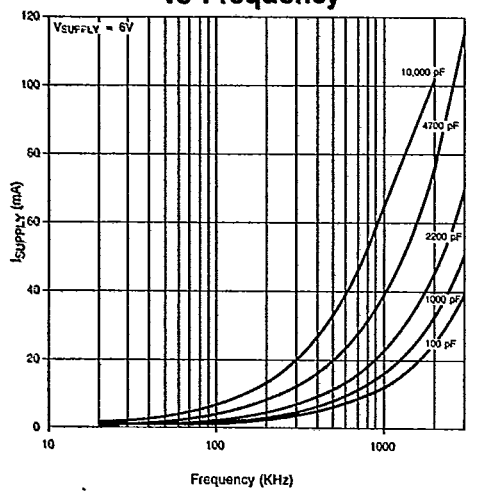
Quiescent Supply Current vs Voltage



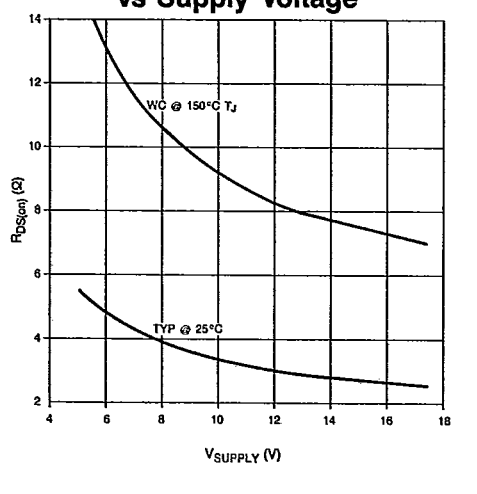
Quiescent Current vs Temperature



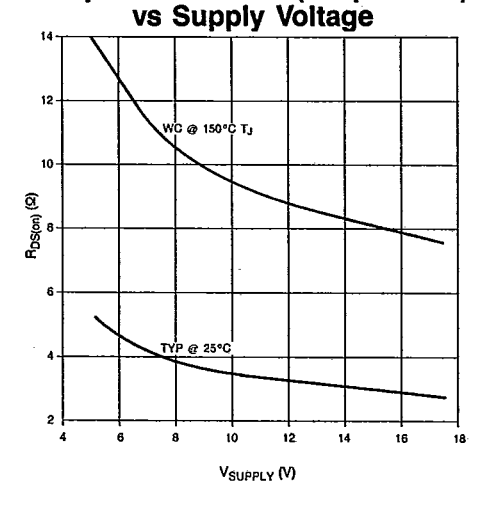
Supply Current vs Frequency



Output Resistance (Output High) vs Supply Voltage



Output Resistance (Output Low) vs Supply Voltage

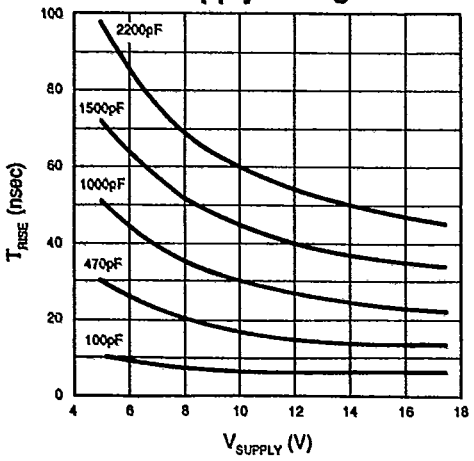


IXLD4423-4428

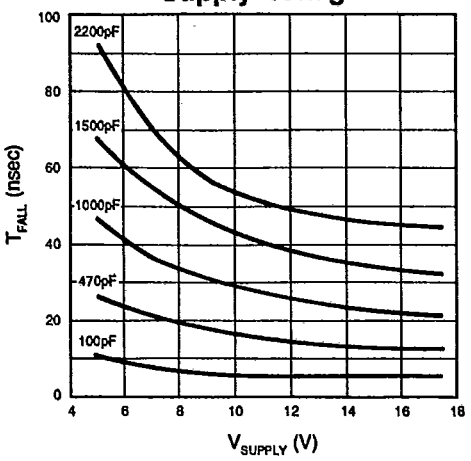
Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

Typical Characteristic Curves (IXLD4426/27/28)

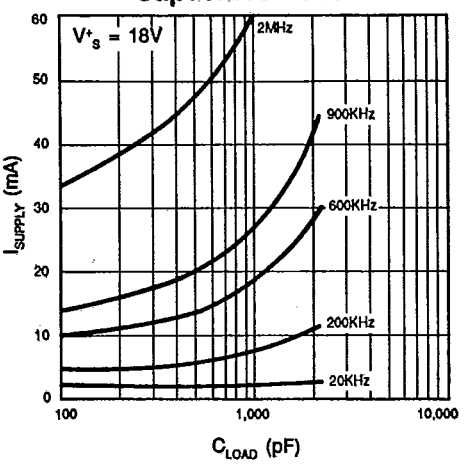
Rise Time vs Supply Voltage



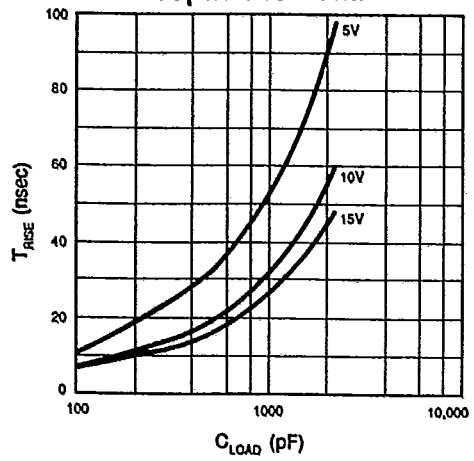
Fall Time vs Supply Voltage



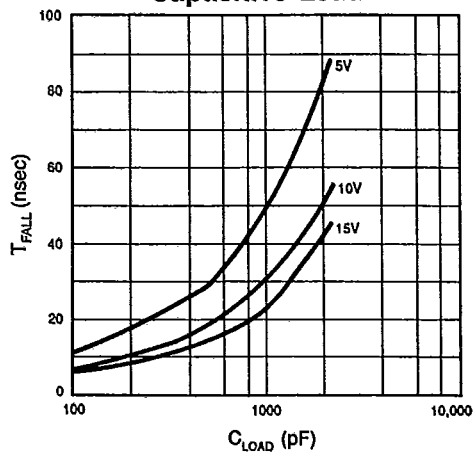
Supply Current vs Capacitive Load



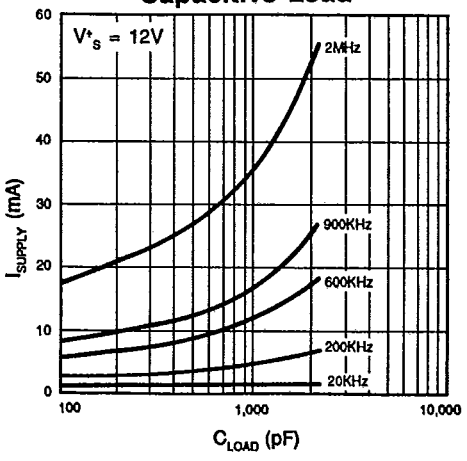
Rise Time vs Capacitive Load



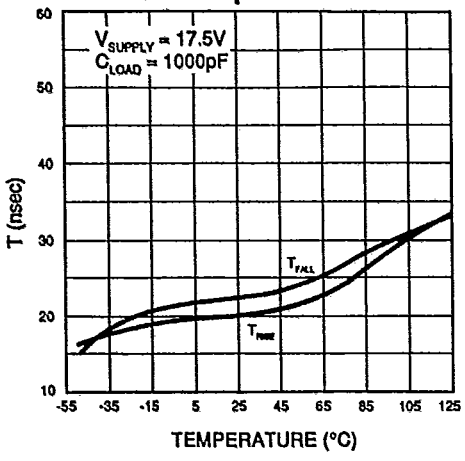
Fall Time vs Capacitive Load



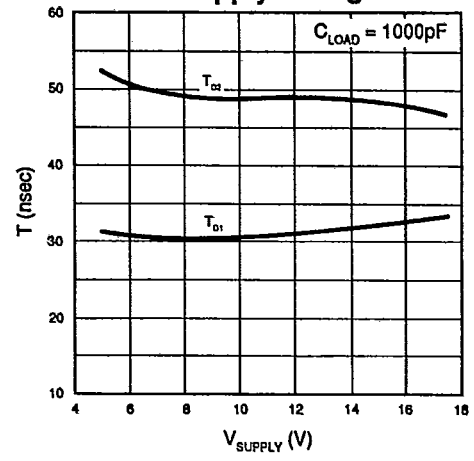
Supply Current vs Capacitive Load



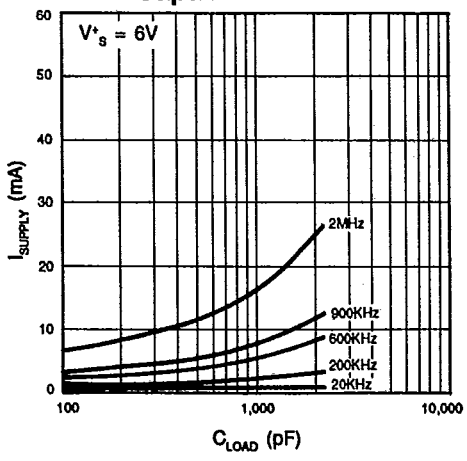
Rise And Fall Time vs Temperature



Propagation Delay Time vs Supply Voltage



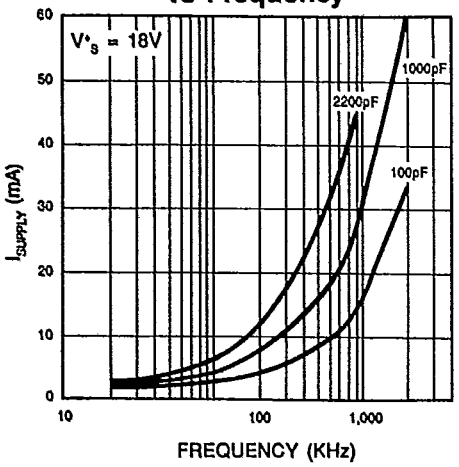
Supply Current vs Capacitive Load



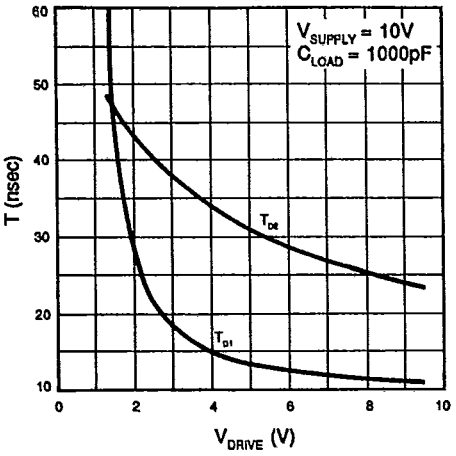
Dual High Speed MOSFET/IGBT Drivers
1.5A/3.0A Peak Drive Current

Typical Characteristic Curves (IXLD4426/27/28) (Continued)

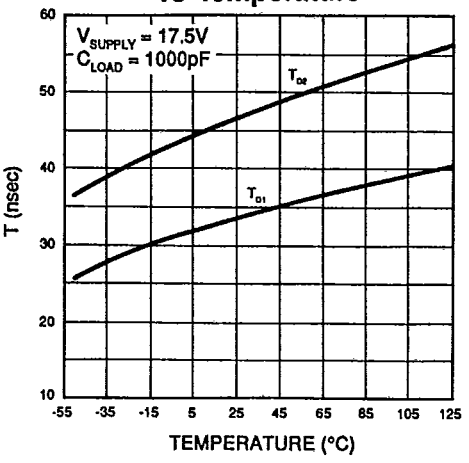
Supply Current vs Frequency



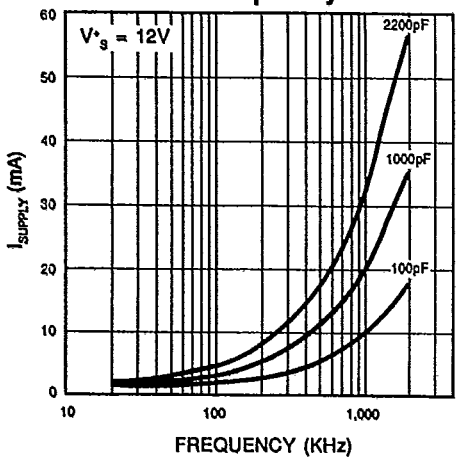
Effect of Input Amplitude on Delay Time



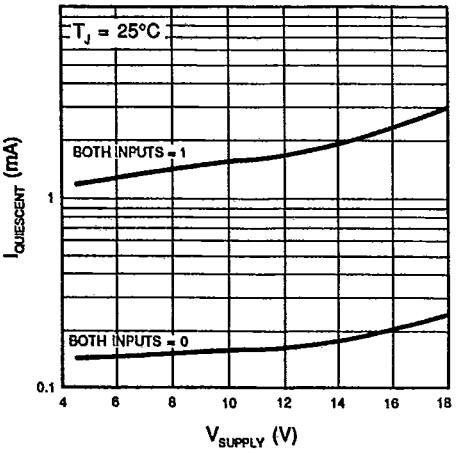
Propagation Delay Time vs Temperature



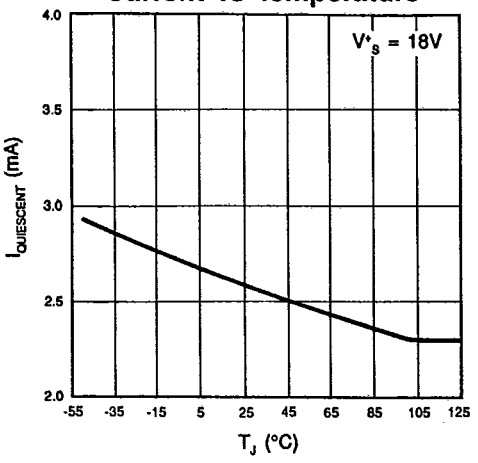
Supply Current vs Frequency



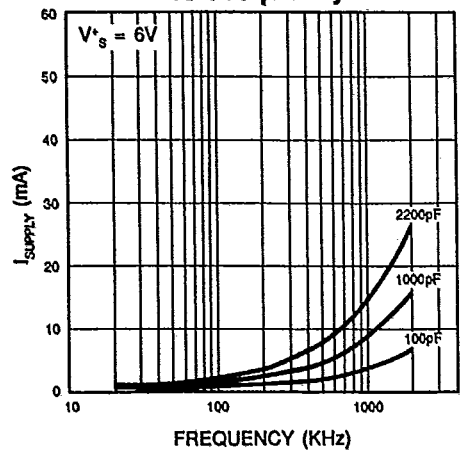
Quiescent Power Supply Current vs Supply Voltage



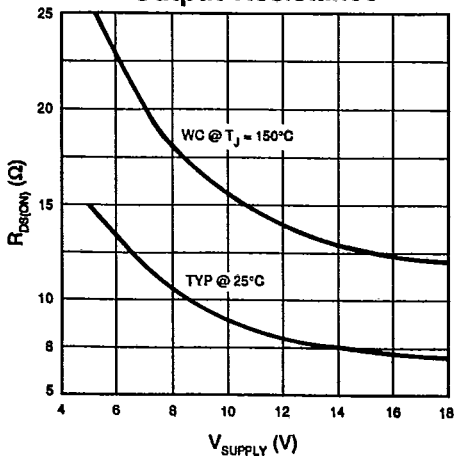
Quiescent Power Supply Current vs Temperature



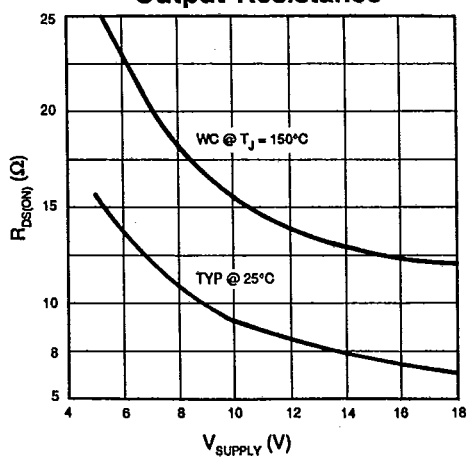
Supply Current vs Frequency



High State Output Resistance



Low State Output Resistance



Application of IXLD4423-4428 Drivers

Although the IXLD4423-4428 drivers have been specifically constructed to operate reliably under any practical circumstances, there are nonetheless details of usage which will, when attended to, provide better operation of the device:

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 1000pf from 0 to 15 volts in 20 nanoseconds requires a constant current of 0.75A. In practice, the charging current is not constant, and will usually peak at around 1.5A. Also charging 2000pf from 0 to 15V in 20ns requires a constant current of 1.5A, which will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that as far as the driver is concerned, the system power supply, as seen by the driver, must have a VERY low impedance.

As a practical matter, this means that the power supply bus must be capacitively bypassed at the driver with at least 100X the load capacitance in order to achieve optimum driving speed. It also implies that the bypassing capacitor must have very low internal inductance and resistance at all frequencies of interest. Generally, this means using two capacitors, one a high-performance low ESR film, the other a low internal resistance ceramic, as together the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. Note please that many film capacitors can be sufficiently inductive as to be useless for this service. Likewise, many multilayer ceramic capacitors have unacceptably high internal resistance. Use capacitors intended for high pulse current service. (In house we use WIMA™film capacitors and AVX Ramguard™ceramics. Several other manufacturers of equivalent devices exist.) The high pulse current demands of capacitive drivers also mean that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PWB land inductance from nullifying what you are trying to accomplish. For optimum results the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 3cm or less.

Bypass capacitance, and its close mounting to the driver serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large ΔI) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. Good bypassing practice is essential to proper operation of high speed driver IC's!

Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load ON. Eventually (except in rare circumstances) it is necessary to turn a load OFF. This requires attention to the Ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: The adequacy of the grounding available for the driver, and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

Best practice for a ground path is obviously a well laid out ground plane. However this in not always practical, and a poorly laid-out ground plane can be worse than none. Attention to the paths taken by return currents, even in a ground plane, is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to the logic driving it, should all be as low in resistance and inductance as possible. Of the three paths, the ground path from the driver to the logic driving it is most sensitive to resistance or inductance, and gound currents from the load are what is most likely to cause disruption. Thus these two ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

To illustrate what can happen, consider the following: The inductance of a 2cm long land, 1.59mm (.062") wide on a 1.59mm (.062") thick PWB with no ground plane is approximately 45nH. Assuming a dI/dt of 0.15A/nS (which will allow a current of 1.5A to flow after 10nS, and is thus slightly slow for our purposes) a voltage of 6.75 Volts will develop along this land in response to our postulated ΔI. For a 1cm land, (approximately 15nH) 2.25 volts is developed in case of dI/dt of 0.3A/nS the voltage will double. Either way, anyone using TTL-level input signals to the driver will find that the response of their driver has been seriously degraded by a common ground path of the given dimensions. Note that this is before accounting for any resistive drops in the circuit. The resistive drop in a 1.59mm (.062") land carrying 1.5A will be about 2mV/cm (5mV/in) at DC, and double that (4mV/cm) for 3A. The resistance will increase with frequency as skin effect comes into play.

The problem is most obvious in inverting drivers where the input and output currents are in phase so that any attempt to raise the driver's input voltage (in order to reduce the driver's output voltage) is countered by the voltage developed on the common ground path as the driver attempts to discharge the load capacitance. It takes very little common ground path, under these circumstances, to alter circuit operation drastically.

Output Lead Inductance

The same descriptions just given for PWB land inductance apply equally well for the output leads from a driver to its load, except that commonly the driver's load is located much further away from the driver than its ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4cm (1.5") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are more than an order of magnitude lower than the impedance of common coax, using coax is seldom a cost effective solution. A twisted pair works about as well, is generally lower in cost, and allows use of a wider variety of connectors. The second wire of the twisted pair should carry common, from as close as possible to the ground pin of the driver, directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver, as this does not provide a complete current path for either driver. Likewise, do not use a twisted triad with two outputs and a common

Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

return unless both of the loads to be driven are mounted extremely close to each other, and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines; i.e. minimize sharp bends, or narrowings in the land, as these will cause ringing. For a rough estimate, on a 1.59mm (.062") thick G-10 PWB a pair of opposing lands each 2.36mm (.093") wide translates to a characteristic impedance of about 50Ω. Half that width suffices on a .787mm (.031") thick board. For accurate impedance matching with a IXLD4426/27/28 driver, on a 1.59mm (.062") thick board, a land width of 24.4mm (.962") would be required, due to the low impedance of the driver and (usually) its load. With an IXLD4423/24/25 driver, a width of 42.75mm (1.683") would be required. This is obviously impractical under most circumstances. Generally the tradeoff point between lands and wires comes when lands narrower than 1.59mm (.062") would be required on a 1.59mm (.062") thick board for the IXLD4426/27/28 drivers and 3.18mm (.125") for the IXLD4423/24/25 drivers.

While one could, in theory, use matching transformers at both ends of a piece of coax, or a dozen or so matched pieces of coax in parallel for transmission between a driver and a distant load, in practice, in situations where the absolute minimum in delay between the driver and the load must be obtained, it is generally easiest to relocate the driver as close as possible to the load (using adequate power supply bypassing of course) and then connect the input of the driver back to the logic using a single piece of coax.

Driving At Controlled Rates

Occasionally, there are situations where a controlled rise or fall time, which may be considerably longer than the normal rise or fall time of the driver output are desired for a load. In such cases it is still prudent to employ best possible practice in terms of bypassing, grounding, and PWB layout, and then reduce the switching speed of the load (NOT the driver) by adding a noninductive series resistor of appropriate value between the output of the driver and the load. For situations where only rise or only fall should be slowed, the resistor can be parallelled with a fast diode so that switching in the other direction remains fast. Due to the schmitt trigger action of the driver's input it is not possible to slow the rate of rise of the input signal and expect the output to react correspondingly.

Input Stage

The input stage of the IXLD4426/27/28 consists of a single-MOSFET class A stage with an input capacitance of 20pF. The IXLD4423/24/25 input capacitance is ⩽38pF. This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is an ≅2mA for IXLD4426/27/28 and ≅1mA for IXLD4423/24/25 current source. Thus, the quiescent current drawn by the driver varies, depending on the logic state of the input.

Following the input stage is a buffer stage which provides ≈300mV of hysteresis for the input, to prevent oscillations when slowly-changing input signals are used, or when noise is present on the input. Input voltage switching threshold is ≈1.5V which makes the driver directly compatible with TTL signals, or with CMOS powered from any supply voltage between 3V and 15V.

The IXLD4426/27/28 and IXLD4423/24/25 drivers can also be driven directly by the IXMS150, IXDP610, SG1524/25/26/27, TL494/95 TL594/95, NE5560/61/62/68, TSC170, TSC38C42, and similar switchmode power supply IC's. By relocating the main switch drive function into the driver rather than using the somewhat limited drive capabilities of a PWM IC, the PWM IC runs cooler, which generally improves its performance and longevity, and the main switches switch faster, reducing switching losses and increasing system efficiency.

The input protection circuitry of the IXLD4423-4428, in addition to providing 2KV or more of ESD protection, also works to prevent latchup or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed, or rendered inoperable until the power supply is cycled OFF and ON. The IXLD4423-4428 drivers have been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC. Because the excess voltage is simply conducted to the power supply terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30mA can be conducted through the IC from the input terminal to the power supply terminal. This may overload the output of whatever is driving the driver, and may cause other devices which share the driver's power supply, as well as the driver, to operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the driver. T_{d2} for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver so that spiking and ringing are minimized, will always result in faster and more reliable operation of the device, leave less EMI to be filtered elsewhere in the circuit, be less stressful to other components in the circuit, and leave less chance of unintended modes of operation.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 series and 74Cnnn have outputs which can only source or sink a few milliamps of current, and even shorting the output of the device to ground or V_{CC} may not damage the device. CMOS drivers, on the other hand, are intended to source or sink several amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver IC's can easily be exceeded when driving large loads at high frequencies. Care must therefore be paid to device dissipation when operating in this domain.

The Supply Current vs Frequency and Supply Current vs Load characteristic curves furnished with this data sheet aid in estimating power dissipation in the driver. Table 1 lists the maximum safe operating frequency for several power supply voltages when driving a 1000pF load. Operating frequency, power supply voltage, and load all affect power dissipation. Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin CERDIP package, from the datasheet, is 150°C/W. In

a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 800 mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

Load Power Dissipation (P_L)
Quiescent power dissipation (P_Q)
Transition power dissipation (P_T)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where: I = the current drawn by the load
R_O = the output resistance of the driver when the output is high, at the power supply voltage used.
D = fraction of time the load is conducting (duty cycle)

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$P_L = F\ C\ (V^+_S)^2$$

where: F = Operating Frequency
C = Load Capacitance
V^+_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads, the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

however in this instance the R_O required may be either the on resistance of the driver when its output is in the high state, or its on resistance when the driver is in the low state, depending on how the inductor is connected. This is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as

$$P_{L2} = I\ V_D\ (1\text{-}D)$$

where Vd is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed to produce P_L.

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (P_Q), as described in the input section, depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2mA. A logic high will result in a current drain of ≤2.0mA. Quiescent power can therefore be found from:

$$P_Q = V^+_S\ [D\ I_H + (1\text{-}D)\ I_L]$$

where: I_H = quiescent current with input high
I_L = quiescent current with input low
D = fraction of time input is high (duty cycle)
V^+_S = power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P- channel MOSFETs in the output totem-pole are ON simultaneously, and a small current is conducted through them from V^+_S to ground. The transition power dissipation is approximately:

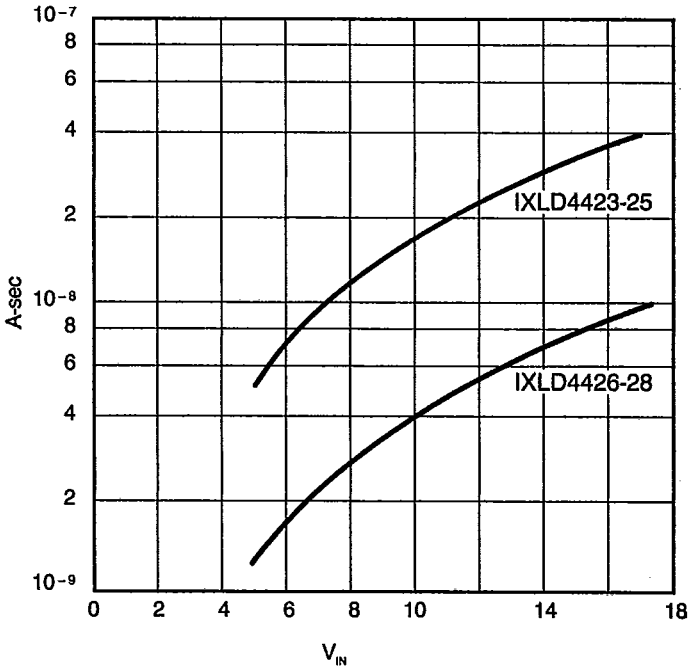
$$P_T = F\ V^+_S\ (A{\cdot}S)$$

where (A•S) is a time-current factor derived from Figure 3.

Total power (P_D) then, as previously described is just

$$P_D = P_L + P_Q + P_T$$

Examples shows the relative magnitude for each term.



NOTE: THE VALUES ON THIS GRAPH REPRESENT THE LOSS SEEN BY BOTH DRIVERS IN A PACKAGE DURING ONE COMPLETE CYCLE. FOR A SINGLE DRIVER DIVIDE THE STATED VALUES BY 2. FOR A SINGLE TRANSITION OF A SINGLE DRIVER, DIVIDE THE STATED VALUE BY 4.

Figure 3. Total nA•S Crossover Energy

Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

EXAMPLE 1: An IXLD4426 operating on a 12V supply, driving two capacitive loads of 820pF each, operating at 450KHz, with a duty cycle of 50%, in a maximum ambient of 60°C.

First calculate load power loss:

$P_L = F \times C_L \times (V^+_S)^2$

$P_L = 450{,}000 \times (820 \times 10^{-12} + 820 \times 10^{-12}) \times 12^2$

$= 0.1063$ W

Then transition power loss:

$P_T = F \times V^+_S \times (A \cdot S)$

$= 450{,}000 \cdot 12 \cdot 5.5 \times 10^{-9} = 0.0297$ W

Then quiescent power loss:

$P_Q = V^+_S \times [D \times I_H + (1\text{-}D) \times I_L]$

$= 12 \times [(0.5 \times 0.004) + (0.5 \times 0.0004)]$

$= 0.0264$ W

Total power dissipation, then is:

$P_D = 0.1063 + 0.0297 + 0.0264$

$= 0.1624$ W

Assuming a plastic package, with an $R_{\theta j\text{-}a}$ of 170°C/W, this will result in the junction running

$0.1624 \times 170 = 27.6°C$

above ambient, which, given a maximum ambient temperature of 60°C, will result in a maximum junction temperature of 87.6°C.

EXAMPLE 2: An IXLD4426 operating on a 15V input, with one half driving a 50Ω resistive load at 1MHz, with a duty cycle of 67%, and the other side quiescent, in a maximum ambient temperature of 40°C:

$P_L = I^2 \times R_O \times D$

First, I_O must be determined.

$$I_O = \frac{V^+_S}{R_O + R_{LOAD}}$$

Given R_O from the data sheet, then,

$$I_O = \frac{15}{12.5 + 50}$$

$I_O = 0.240$ A

and: $P_L = 0.240^2 \times 12.5 \times 0.67$

$= 0.4824$ W

$P_T = F \times V^+_S$ A•S/2
(because only one side is operating)

$$= 1{,}000{,}000 \times 15 \times \frac{9 \times 10^{-9}}{2}$$

$= 0.0675$ W

and: $P_Q = \{15 \times [(0.67 \times .002) + (0.33 \times .0002) + (1 \times 0.0002)]\}$
(this assumes that the unused side of the driver has its input grounded, which is more efficient)

$= 0.0241$ W

and: $P_D = 0.4824 + 0.0675 + 0.0241$

$= 0.5740$ W

In a ceramic package with a $R_{\theta j\text{-}a}$ of 150°C/W, this amount of power results in a junction temperature, given the maximum 40°C ambient, of:

$(0.5740 \times 150) + 40 = 126.1°C$

The actual junction temperature will be lower than calculated both because duty cycle is less than 100% and because the graph lists $R_{DS(on)}$ at a T_j of 150°C, and the $R_{DS(on)}$ at 125°C T_j will be somewhat lower.

Definitions:

C_L = Load Capacitance, in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

F = Operating Frequency of the driver, in Hertz.

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_O = Output current from a driver, in Amps.

P_D = Total power dissipated in a driver, in Watts.

P_L = Power dissipated in the driver due to the driver's load, in Watts.

P_Q = Power dissipated in a quiescent driver, in Watts.

P_T = Power dissipated in a driver when the output changes states (''shoot-through current''), in Watts.

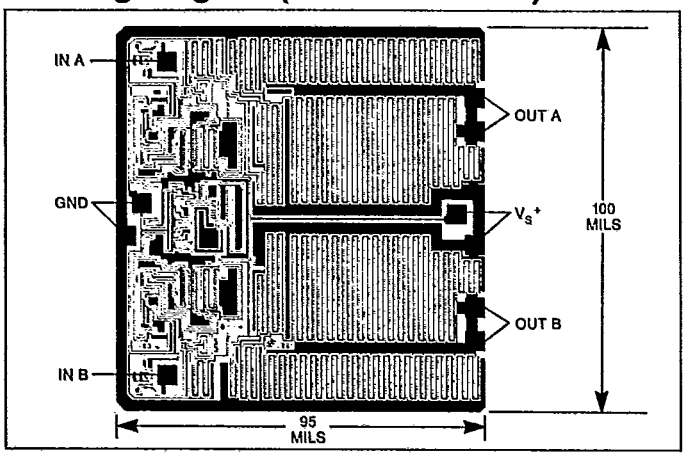
R_O = Output resistance of a driver, in Ohms.

V^+_S = Power supply voltage to the IC, in Volts.

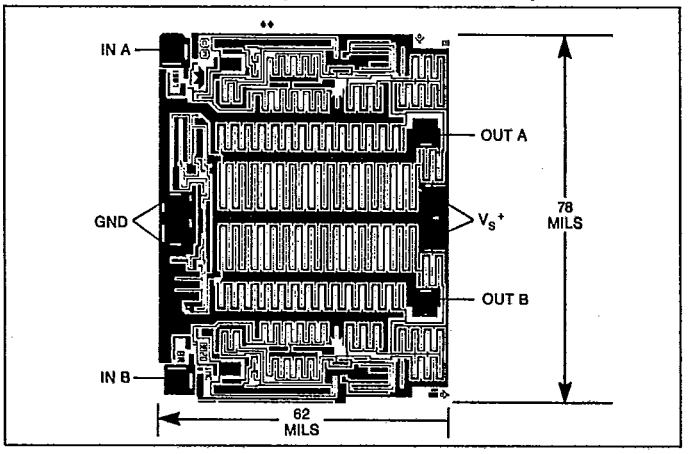
IXLD4423-4428

Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

Bonding Diagram (IXLD4423/24/25)

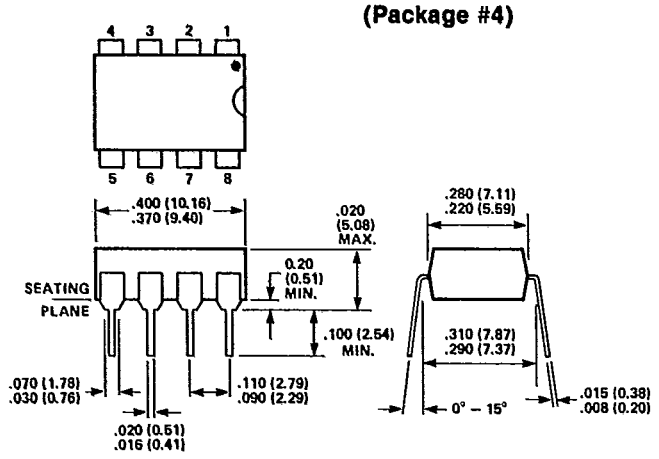


Bonding Diagram (IXLD4426/27/28)

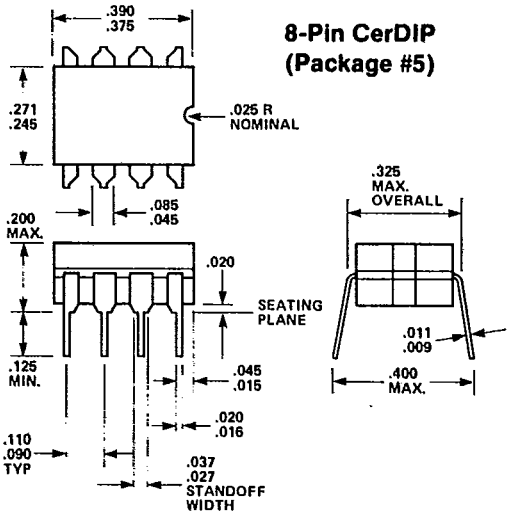


Package Information

8-Pin Plastic DIP (Package #4)

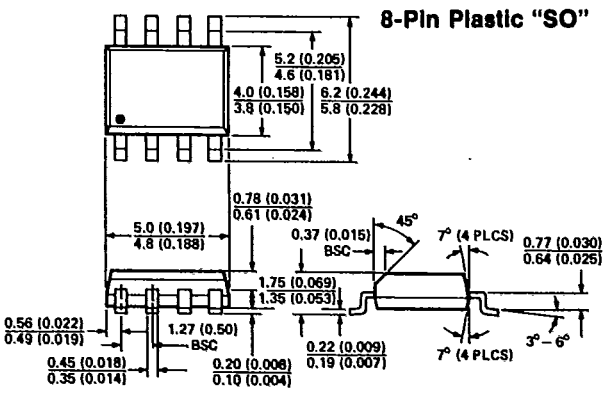


8-Pin CerDIP (Package #5)

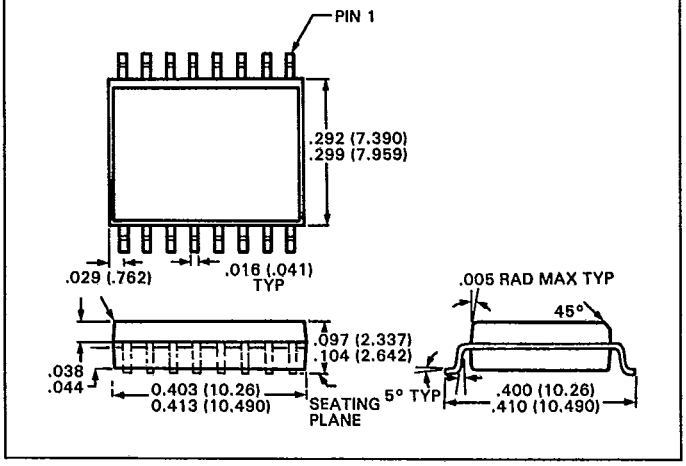


Package Information

8-Pin Plastic "SO"



Package Information



Dual High Speed MOSFET/IGBT Drivers
1.5 A/3 A Peak Drive Current

IXLD4423-4428

The following families of power drivers are made with a CMOS process to inferface between low-level control functions and high-power switching devices, particularly power MOSFETs. The devices are also an optimum choice for capacitive line drivers where 1.2 A-6 A may be switched. With both inverting and non-inverting inputs available, logic signals of either polarity may be accepted.

Selecting MOSFET Drivers

Device	Drive Current	Output No. & Type Invert.	Non-Invert	Rated Load (pF)	Rise Time @ Rated Load (nS)	Fall Time @ Rated Load (nS)	Leading Edge Prop. Delay* (nS)	Trailing Edge Prop. Delay (nS)	Latch	Input Protected to 5 V Below Gnd RAIL
IXLD1426	1.2 A Peak	dual		1000	30	20	55	80	Resistant	NO
IXLD1427	1.2 A Peak		dual	1000	30	20	55	80	Resistant	NO
IXLD1428	1.2 A Peak	single &	single	1000	30	20	55	80	Resistant	NO
IXLD426	1.5 A Peak	dual		1000	30	20	40	75	Resistant	NO
IXLD427	1.5 A Peak		dual	1000	30	20	40	75	Resistant	NO
IXLD428	1.5 A Peak	single &	single	1000	30	20	40	75	Resistant	NO
IXLD4426	1.5 A Peak	dual		1000	30	30	40	55	Immune	YES
IXLD4427	1.5 A Peak		dual	1000	30	30	40	55	Immune	YES
IXLD4428	1.5 A Peak	single &	single	1000	30	30	40	55	Immune	YES
IXLD4423	3.0 A Peak	dual		1800	25	25	40	40	Immune	YES
IXLD4424	3.0 A Peak		dual	1800	25	25	40	40	Immune	YES
IXLD4425	3.0 A Peak	single &	single	1800	25	25	40	40	Immune	YES
IXLD429	6.0 A Peak	single		2500	23	25	53	60	Resistant	NO
IXLD4420	6.0 A Peak		single	2500	25	25	55	55	Immune	YES
IXLD4429	6.0 A Peak	single		2500	25	25	55	55	Immune	YES

MOSFET Die Size vs. Suggested Driver Family

MOSFET Size	Suggested Driver (@ 12 V)	Typical t_r/t_f	Suggested Driver for faster speed (@ 12 V)	Typical t_r/t_f
Size 3	IXLD426/1426/4426	20/30	IXLD4423	10/20
Size 4	IXLD426/1426/4426	30/40	IXLD4423	25/25
Size 5	IXLD426/1426/4426	55/55	IXLD4423	30/35
Size 6	IXLD4423	40/50	IXLD4420/4429	30/35
Size 7	IXLD4420/4429	36/35	—	—
Size 8	IXLD4420/4429	50/50	—	—