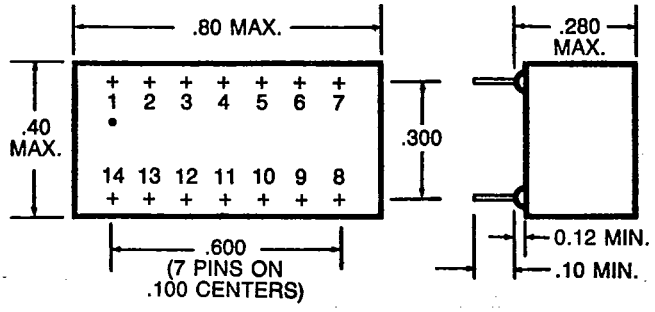
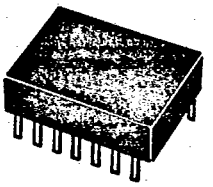
YCL

DIGITAL DELAY LINES
TTL COMPATIBLE
5 TAPS•SINGLE•DUAL•TRIPLE
14 PIN PACKAGE

SERIES J05, J01, J02 AND J03



White Dot locates Pin 1



ONLY ACTIVE PINS ARE SUPPLIED

Intermediate delay values available upon request.

SERIES J05 (5 TAP)		
MODEL NO. (Fig. 1)	Delay ns	Delay/Tap ns
J05025	25	5
J05030	30	6
J05035	35	7
J05040	40	8
J05045	45	9
J05050	50	10
J05060	60	12
J05075	75	15
J05100	100	20
J05125	125	25
J05200	200	40
J05250	250	50
J05300	300	60
J05400	400	80
J05500	500	100

Delay/ line (ns)	MODEL NUMBERS		
	Series J01	Series J02	Series J03
	One output (Fig. 2)	Dual output (Fig. 3)	Triple output (Fig. 4)
5	J01005	J02005	J03005
10	J01010	J02010	J03010
15	J01015	J02015	J03015
20	J01020	J02020	J03020
25	J01025	J02025	J03025
50	J01050	J02050	J03050
75	J01075	J02075	J03075
100	J01100	J02100	J03100
150	J01150	J02150	J03150
200	J01200	J02200	J03200
250	J01250	J02250	J03250
300	J01300		
400	J01400		
500	J01500		

DC PARAMETERS		LIMITS	
		Min.	Max.
Voh	Vcc = min Ioh = 1.0mA	2.5V	—
Vol	Vcc = min Iol = 20mA	—	0.5V
Iih	Vcc = max Vih = 2.7V	—	50μA
Iil	Vcc = max Vil = 0.5V	−2.0mA	—
Ii	Vcc = max Vi = 5.5V	—	1.0mA
Vi	Vcc = min Iin = −18 modc	−1.2vdc	—
Icc	Vcc = max outputs low	Series J05 70mA Series J01 55mA Series J02 100mA Series J03 120mA	

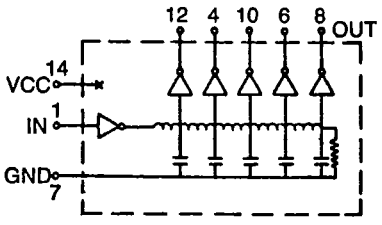


FIG.1

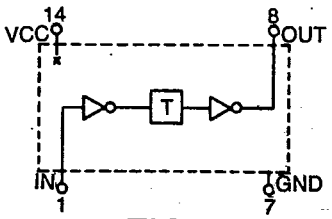


FIG.2

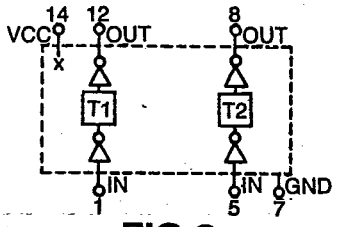


FIG.3

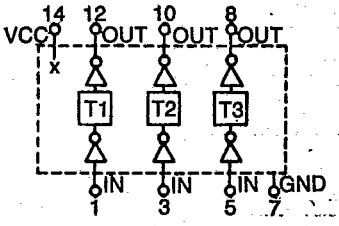


FIG.4

SPECIFICATIONS:

- Supply voltage: 5.0VDC ± 10%
- Delay tolerances: ±2ns or ±5% wig
- Rise time: 4ns max
- Minimum Pulse Width: 40% of Td
- Maximum Duty Cycle: 50%
- Operating temp. range: 0°C to +70°C
- Temp. coeff. of delays: 1.0ns +500ppm/°C
- Terminals: Electro tin plated Alloy 42 .020w × .010th

TEST CONDITIONS:

- Vcc = 5.0VDC, Temp. 25°C ± 5°C
- Time delay measured at the 1.5V level
- Rise time measured from .75V to 2.4V
- All outputs loaded with 15pf
- Input Test Pulse: Pulse Voltage: 3.0V
  Pulse rise time: 2ns
  Pulse width: 1.2 × max Td
  Pulse spacing: 5 × max Td