Am29114

Real-Time Interrupt Controller

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Real-Time Interrupt Servicing
  Supports interrupts at microinstruction boundaries, making interrupt responses virtually instantaneous.
- Expandable
  Cascadable to accept any number of interrupt inputs
- Accepts 8 Interrupt Inputs
  Interrupt request signals may be levels or pulses
- Vector Outputs
  Output is binary code for the highest priority un-masked interrupt request.
- On-Chip Prioritization
  Only interrupts having higher priority than the highest interrupt in service are allowed.
- 8-Bit Mask Register
  Allows particular interrupt inputs to be temporarily disabled.

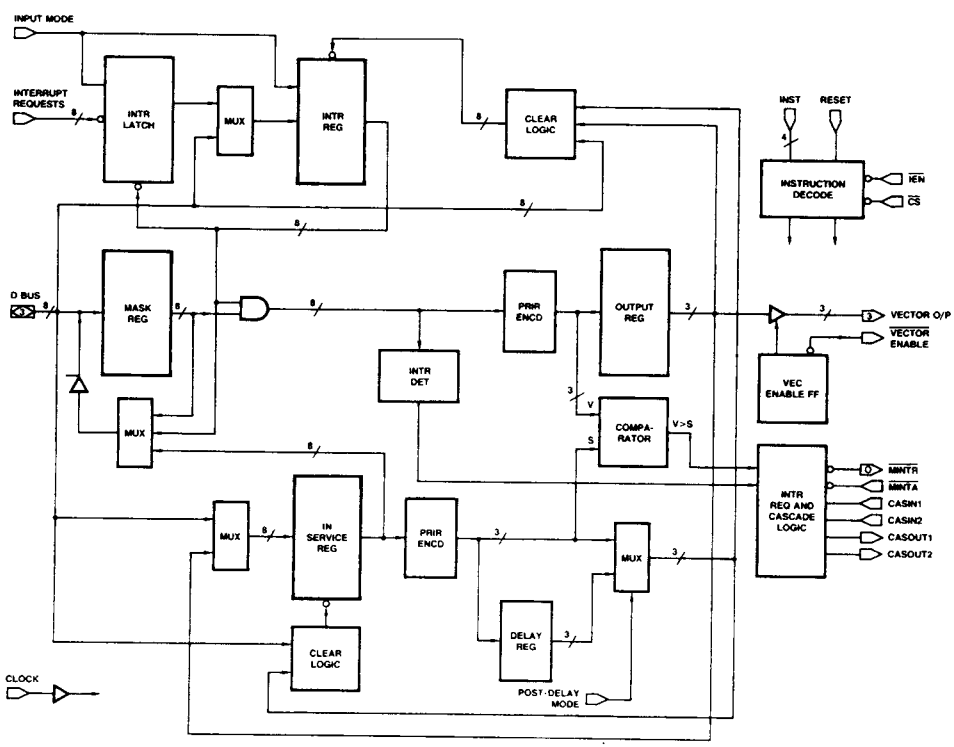
GENERAL DESCRIPTION

The Am29114 is a high-performance 8-bit vectored priority interrupt controller intended for use in very high-speed microprogrammed machines. Its architecture and instruction set are optimized to take full advantage of the real-time interrupt capabilities of state-of-the-art sequencers such as the Am29112.

The Am29114 is designed to operate in 10 MHz microprogrammed systems.

The Am29114 features 16 microinstructions which allow designers to read from and write to key registers for maximum control flexibility.

BLOCK DIAGRAM



BD001941

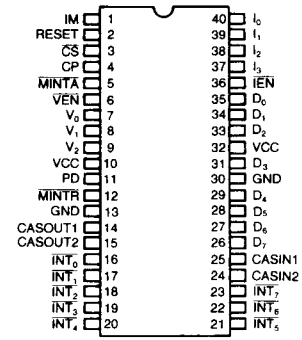
Order # 05190B

June 1986

RELATED PRODUCTS

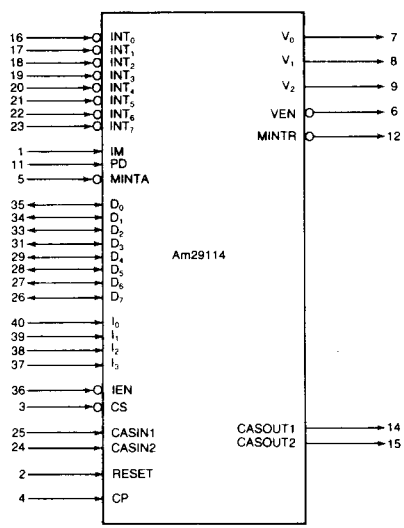
Part No.	Description
Am29112	8-Bit High-Performance Microprogram Sequencer
Am29116	16-Bit Bipolar Microprocessor
Am29117	Two-Port Am29116
Am29118	8-Bit Bidirectional I/O Port/Accumulator
Am29PL141	Fuse-Programmable Controller
Am2950A/ 51A/52A/53A	8-Bit Bidirectional I/O Port
Am2925	System Clock Generator and Driver
Am2904	Status and Shift Control Unit
Am2940	DMA Address Generator
Am2942	Programmable Timer/Counter/DMA

CONNECTION DIAGRAM



CD006010

LOGIC SYMBOL



LS001880

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29114 **D** **C** **B**

- **B**: Optional Processing — Blank = Standard Processing; B = Burn-in
- **C**: Temperature Range — C = Commercial (0 to +70°C)
- **D**: Package — D = 40-Pin Sidebrazed Hermetic DIP (SD-040)
- **Am29114**: AMD Device Type — Real-Time Interrupt Controller

Valid Combinations	
Am29114	DC, DCB,

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$D_0 - D_7$ Data Input/Output Lines.

Used to transfer information between the system data bus and the mask, interrupt and in-service registers of the Am29114.

$\overline{INT_0} - \overline{INT_7}$ Interrupt Inputs.

Accept requests as active-low levels or pulses, depending on the voltage level at the IM pin.

IM Input Mode Select.

When IM is low, $\overline{INT_0} - \overline{INT_7}$ detect asynchronous pulse inputs. When IM is high, $\overline{INT_0} - \overline{INT_7}$ detect level inputs.

$I_0 - I_3$ Instruction Inputs.

$\overline{IEN}$ Instruction Enable.

The instruction on $I_0 - I_3$ is ignored if $\overline{IEN}$ is high.

$\overline{CS}$ Chip Select.

Instructions 4 – 15 (those which use the D-bus) are ignored if $\overline{CS}$ is high.

$\overline{MINTR}$ Maskable Interrupt.

Low level indicates that an unmasked interrupt request which has a priority higher than the request currently being serviced is in the interrupt register waiting for service. $\overline{MINTR}$ is forced high when either $\overline{MINTA}$ is low or CASIN1 or CASIN2 are high. $\overline{MINTR}$ has an open collector output.

$\overline{MINTA}$ Maskable Interrupt Acknowledge.

Active-low signal causes the interrupting request vector in the vector output register to be enabled onto the vector output pins ($V_0 - V_2$). It also causes the bit corresponding to the interrupting request to be cleared in the interrupt register and set in the in-service register. Note: To permit cascading, these operations occur only if the $\overline{VEN}$ output is low (i.e., vector-enable flip-flop is set).

$V_0 - V_2$ Interrupt Vector.

Tristate $V_0 - V_2$ lines are output enabled with the interrupting vector when the $\overline{MINTA}$ input is low and the $\overline{VEN}$ output is low (i.e., vector-enable flip-flop is set.)

$\overline{VEN}$ Vector Enable.

Output of vector-enable flip-flop. The vector-enable flip-flop is cleared ($\overline{VEN}$ high) on the next active clock edge when CASIN2 is high. When CASIN2 is low, the vector-enable flip-flop is set ($\overline{VEN}$ low) on each active clock edge if an unmasked interrupt is waiting in the interrupt register, otherwise it is cleared.

CASIN1 Cascade-in 1.

High level forces $\overline{MINTR}$ high and causes the CHSR and CCIR instructions to have no effect.

CASIN2 Cascade-in 2.

High level forces $\overline{MINTR}$ high and clears the vector-enable flip-flop on the next active clock edge.

CASOUT1 Cascade-out 1.

Forced high if any bit in the in-service register is set or if CASIN1 is high.

CASOUT2 Cascade-out 2.

Forced high if there is an unmasked interrupt request in the interrupt register or if CASIN2 is high.

RESET Master Reset.

High level causes the interrupt latches, interrupt register, in-service register and mask register to be cleared on the next active clock edge.

PD Post-Delay Mode.

Hard-wire high when operating with the Am29112 in post-delay mode. High level causes CASIN1 input and prioritized output of in-service register to be delayed by one clock cycle.

CP Clock Pulse.

All state changes occur on the low-to-high transition of the clock.

FUNCTIONAL DESCRIPTION

The Am29114 receives interrupt requests on 8 interrupt input lines ($INT_0 - INT_7$). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the result is sent to a priority encoder, which produces a 3-bit encoded vector representing the highest numbered input which is not masked. This encoded vector will be held in the vector output register.

An 8-bit in-service register holds a bit for each interrupt request that is currently being serviced. If a new interrupt has a higher priority than the one in process, an interrupt request output will occur and this signal will be sent to the sequencer. Subsequently, an acknowledge signal from the sequencer is used to enable the vector outputs and to set the corresponding bit in the in-service register to prevent the interrupt routine from being interrupted by a lower priority interrupt. When the service routine is complete, an instruction clearing the in-service register bit allows system operation to continue as before.

The Am29114 is controlled by a 4-bit instruction field which allows the three above-mentioned registers to be read or modified under microprogram control.

Architecture Of The Am29114

The Am29114 is a high-performance priority interrupt controller. As shown in the Block Diagram, the device contains four registers: the Interrupt Register, the Mask Register, the In-Service Register, and the Vector Output Register.

Interrupt Latch/Register

The 8-bit Interrupt Register stores pending interrupt requests in clocked D flip-flops. A bit in the register is automatically cleared when the corresponding interrupt request is acknowledged by the system sequencer. Interrupt requests can be accepted via 8 S-R latches in either of two modes depending upon the level of the IM input.

Asynchronous Pulse Mode: Low-going pulses on the $\overline{INT}$ inputs set the latches. The outputs of the latches cause the respective flip-flops to be set on the next active clock edge. The outputs of the flip-flops are then used to clear the latches. Requests remain stored in the register until their interrupts are acknowledged.

Level Mode: The latches become transparent, and the interrupt register contains the interrupt requests only as long as the corresponding $\overline{INT}$ lines are held low. Therefore, in order to be recognized, an interrupt signal must be held low until it is acknowledged.

Bits may also be set in the interrupt register under microprogram control, thus permitting software-generated interrupts.

Mask Register

The 8-bit Mask Register allows selected interrupt inputs to be disabled. When a bit is set, the corresponding output of the Interrupt Latch Register is disabled without affecting the interrupt register itself.

In-Service Register

The 8-bit In-Service Register keeps track of which interrupt requests have been accepted by the system sequencer for servicing. When a bit corresponding to a particular interrupt is set, all equal and lower priority interrupts are masked. Once a bit in the In-Service Register is set, a micro-instruction must be issued to clear it.

Vector Output Register

The 3-bit Vector Output Register is loaded on each active clock edge with the priority code of the highest-priority unmasked interrupt currently in the interrupt register.

Interrupt Detector/Priority Encoder

The Interrupt Detector detects the presence of an unmasked interrupt waiting for service. The Priority Encoder determines the highest-priority unmasked interrupt waiting for service and forms a binary coded interrupt vector.

Comparator

The 3-bit Comparator determines whether or not the priority of the highest unmasked interrupt waiting for service is higher than the priority of the interrupt currently being serviced.

Clear Control Logic

The Clear Control Logic generates clear signals for individual bits of the Interrupt and In-Service Registers. The Clear Control Logic takes inputs from the D-Bus and from the Vector Output Register (after an interrupt acknowledge is received).

Interface Logic

The Interface Logic circuitry generates the interrupt, vector enable and cascade signals.

Instruction Set

The Am29114 is controlled by the 4-bit instruction inputs $I_0 - I_3$. The instruction input is ignored if $\overline{IEN}$ is high, allowing the four I bits in the instruction word to be shared with other functions. Instructions that access the D-Bus (instructions 4 – 15) are ignored if $\overline{CS}$ is high, allowing the D-Buses of several Am29114s in a cascaded system to be tied together (see Table 1).

TABLE 1. INSTRUCTION SET

I_3	I_2	I_1	I_0	Mnemonic	Description
0	0	0	0	MCLR	Master Clear
0	0	0	1	CHSR	Clear highest priority bit in in-service register[1]
0	0	1	0	CCIR	Clear current interrupt bit in interrupt register[2]
0	0	1	1	NOOP	No operation
0	1	0	0	BSMK	Bit set mask register from D-Bus[3]
0	1	0	1	BCMK	Bit clear mask register from D-Bus[4]
0	1	1	0	LDMK	Load mask register from D-Bus
0	1	1	1	RDMK	Read mask register from D-Bus
1	0	0	0	BSSR	Bit set in-service register from D-Bus[3, 5]
1	0	0	1	BCSR	Bit clear in-service register from D-Bus[4, 5]
1	0	1	0	LDSR	Load in-service register from D-Bus[5]
1	0	1	1	RDSR	Read in-service register from D-Bus[5]
1	1	0	0	BSIR	Bit set interrupt register from D-Bus[3, 6]
1	1	0	1	BCIR	Bit clear interrupt register from D-Bus[4, 6]
1	1	1	0	LDIR	Load interrupt register from D-Bus[6]
1	1	1	1	RDIR	Read interrupt register from D-Bus[6]

NOTES:
1. CHSR may be used at the end of an interrupt service routine to restore the previous priority level. In post-delay mode CHSR clears the bit that had the highest priority one clock cycle before the instruction arrived at the instruction inputs.
2. CCIR clears the interrupt register bit corresponding to the highest bit set in the in-service register. In post-delay mode CCIR clears the bit in the interrupt register corresponding to the bit that had the highest priority in the in-service register one clock cycle before the instruction arrived at the instruction inputs.
3. Sets those register bits that have corresponding D-Bus bits equal to one. Other register bits are not affected.
4. Clears those register bits that have corresponding D-Bus bit equal to one. Other register bits are not affected.
5. Overrides the effect of an interrupt request or an interrupt acknowledge on bits being modified if received during the same clock cycle.
6. An interrupt acknowledge received during the same clock cycle will override this instruction where they affect the same bit.

APPLICATIONS

System Implementation

Connection to Am29112

The Am29114 is connected to the Am29112 as shown in Figure 1. The tri-state vector outputs are connected to three bits of the Y-bus of the Am29112. The other five bits of the Y-bus are taken from the outputs of a tri-state buffer. The inputs of the buffer may be hardwired to define the other five bits of the interrupt jump address. The $\overline{MINTA}$ output of the Am29112 is used to enable the vector output onto the Y-bus. The instruction inputs to the Am29114 are taken from the

microinstruction pipeline register, and the D-bus is connected to the data highway of the system. In a system employing only a single Am29114, the CASIN1 and CASIN2 are hardwired low.

Cascading Am29114s

Am29114s are cascaded by connecting the CASOUT1 and CASOUT2 signals of one chip to the CASIN1 and CASIN2 of the next-most-significant chip. See Figures 2 and 3. CASIN1 and CASIN2 of the most significant chip are usually tied low, but open-collector CASIN2 may be forced high in order to disable all interrupts. The $\overline{\text{MINTR}}$ outputs are tied together to form one common interrupt line. Also common to all chips are the instruction enable, instruction, acknowledge, reset and clock lines. The D-bus pins of each chip may either be tied together or left separate if the width of the system bus allows. If tied together, the chip-select inputs may be used to select a particular chip for D-bus operations.

The vector outputs of each chip are tied together to form the least-significant three bits of the interrupt vector. There are two ways of forming the most-significant bits of the interrupt vector. In Method 1 (Figure 2), a priority encoder with tri-state outputs is used to priority encode the vector-enable outputs. In Method 2 (Figure 3), the priority encode of the CASOUT2 outputs is clocked into a register with tri-state outputs. Method 2 may be useful where it is necessary to remove the priority encoder from a critical timing path that includes the microprogram memory. If only two Am29114s are cascaded, the vector-enable output of the least significant chip may be used directly as the fourth bit of the interrupt vector (Figure 4).

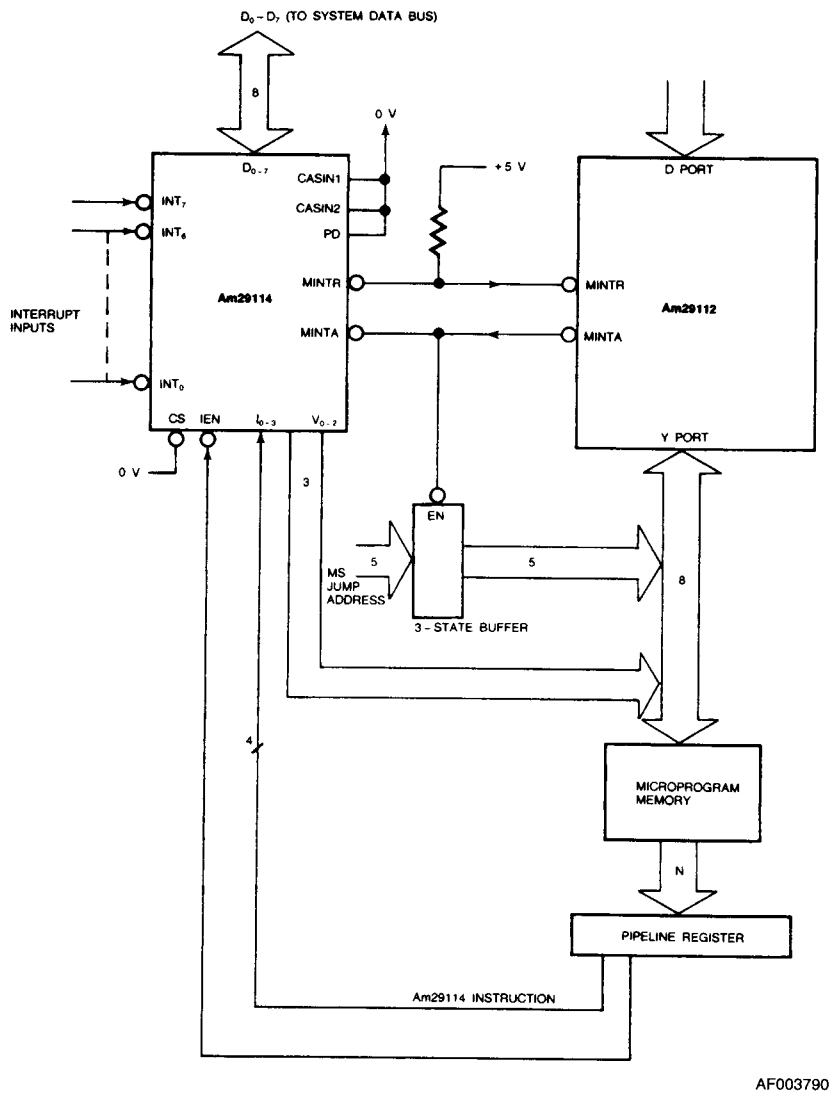


Figure 1. Connection of Am29114 to Am29112

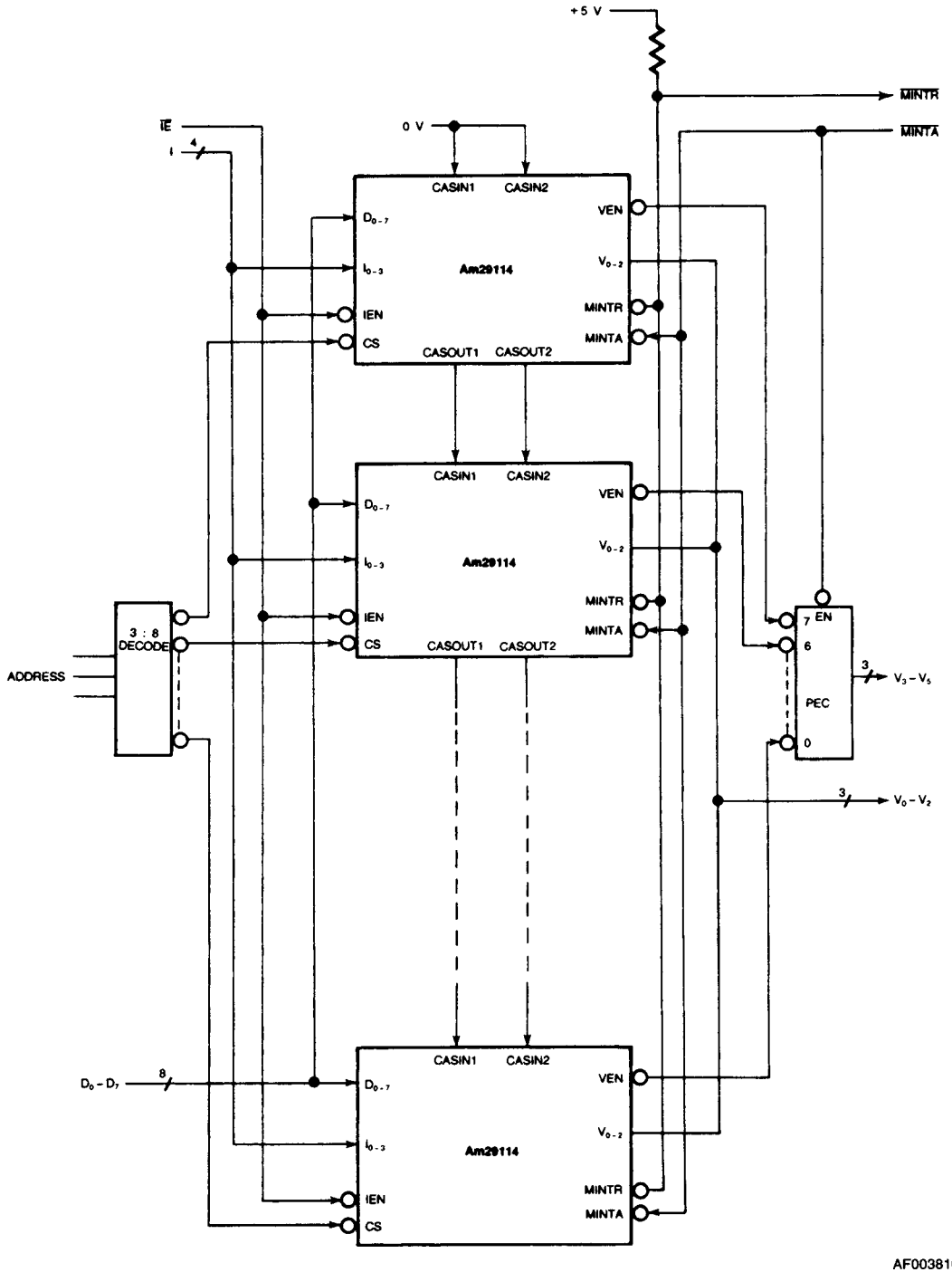


Figure 2. Cascading the Am29114 – Method 1

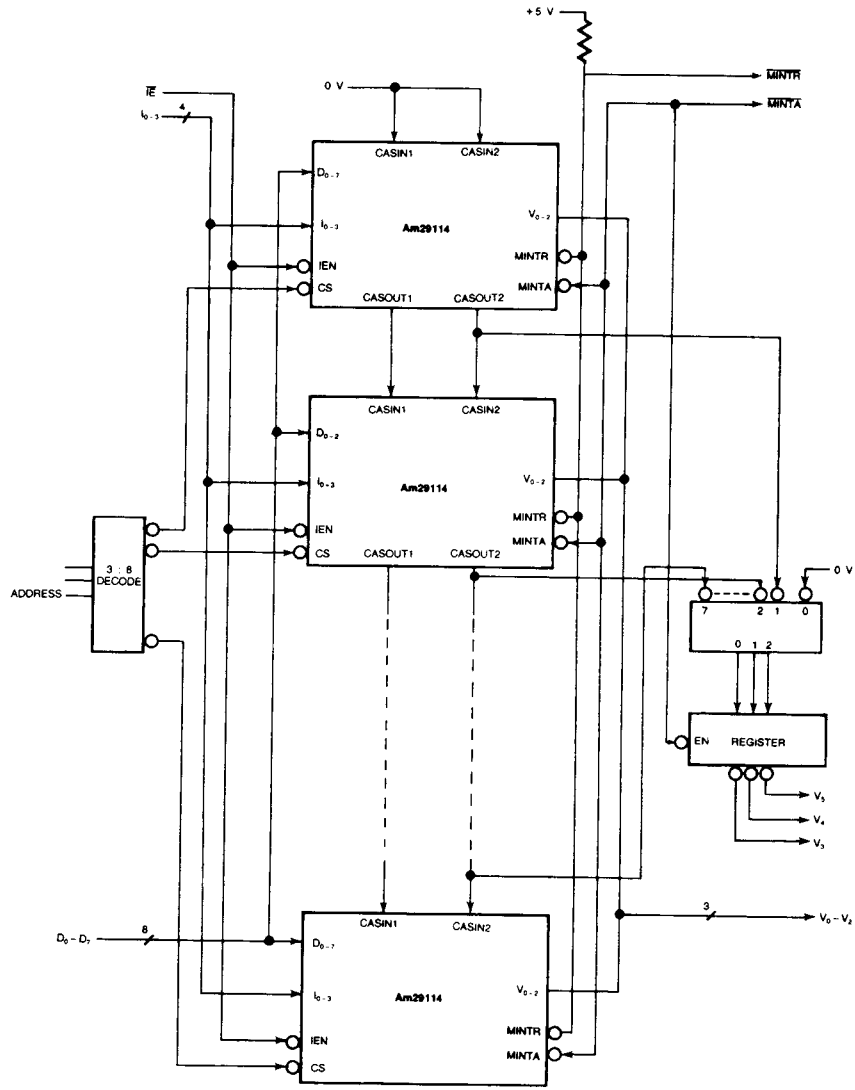


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Figure 3. Cascading the Am29114 – Method 2

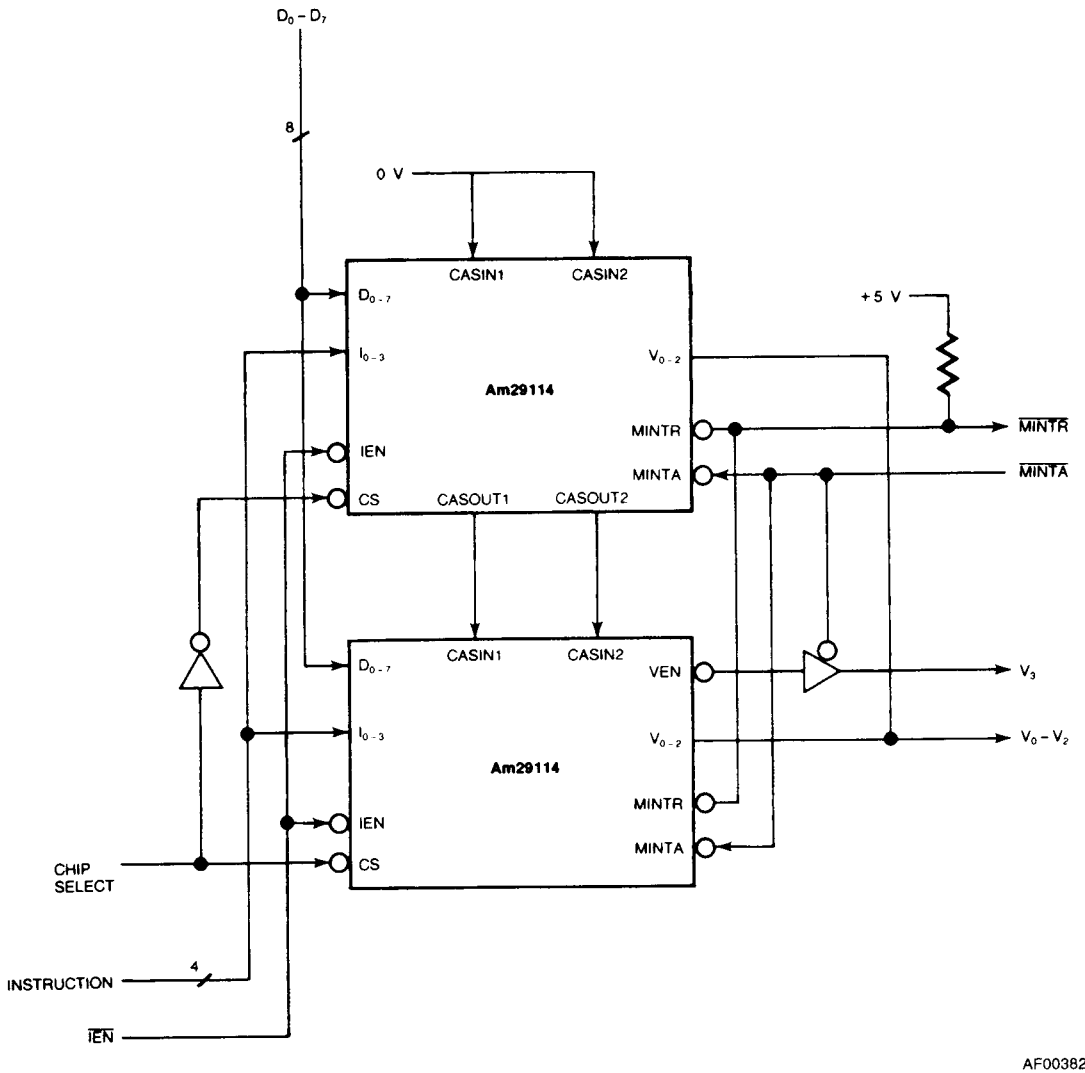
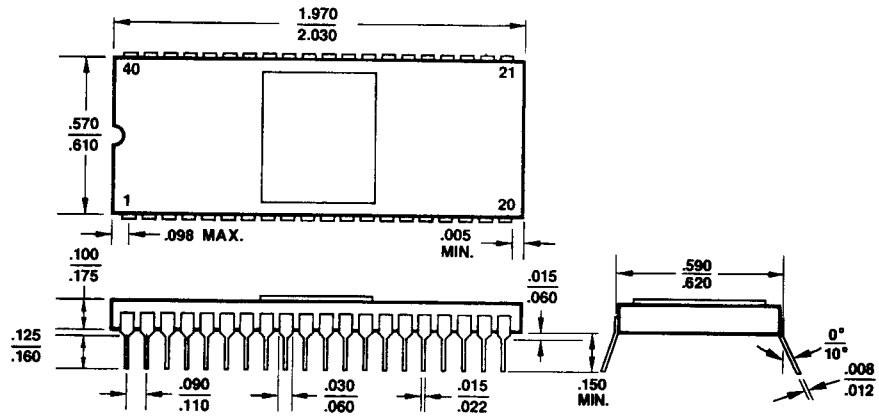


Figure 4. Cascading the Am29114 – 16-Bit Configuration

PHYSICAL DIMENSIONS

SD 040



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