


**HEWLETT
PACKARD**

FOUR CHARACTER 6.9 mm (0.27 INCH) 5x7 ALPHANUMERIC DISPLAYS

STANDARD RED	HDSP-2490
YELLOW	HDSP-2491
HIGH EFFICIENCY RED	HDSP-2492
HIGH PERFORMANCE GREEN	HDSP-2493

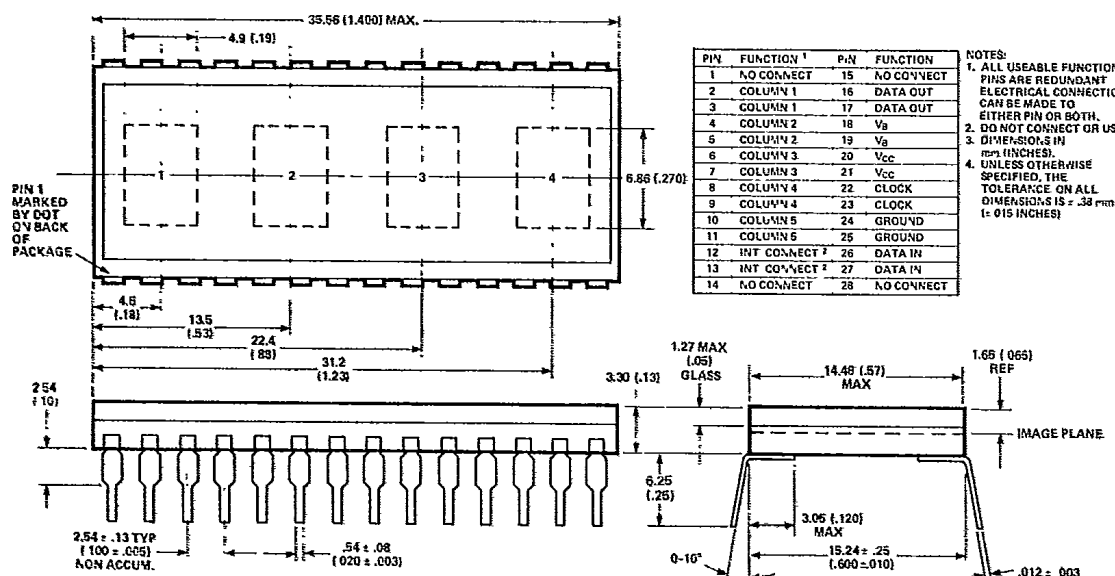
Features

- FOUR COLORS
Standard Red
Yellow
High Efficiency Red
High Performance Green
- INTEGRATED SHIFT REGISTERS WITH
CONSTANT CURRENT DRIVERS
- COMPACT CERAMIC PACKAGE
- WIDE VIEWING ANGLE
- END STACKABLE FOUR CHARACTER
PACKAGE
- TTL COMPATIBLE
- 5 x 7 LED MATRIX DISPLAYS FULL ASCII SET
- CATEGORIZED FOR LUMINOUS INTENSITY
- HDSP-2491/2493 ALSO CATEGORIZED FOR
COLOR

Description

The HDSP-2490/-2491/-2492/-2493 series of displays are 6.9 mm 0.27 inch 5 x 7 LED arrays for display of alphanumeric information. These devices are available in standard red, yellow, high efficiency red, and high performance green.

Package Dimensions



Absolute Maximum Ratings (HDSP-2490/-2491/-2492/-2493)

Supply Voltage V_{CC} to Ground -0.5V to 6.0V
 Inputs, Data Out and V_B -0.5V to V_{CC}
 Column Input Voltage, V_{COL} -0.5V to +6.0V
 Free Air Operating
 Temperature Range, T_A ^[1,2] -20°C to +85°C

Storage Temperature Range, T_s -55°C to +100°C
 Maximum Allowable Power Dissipation
 at $T_A = 25^\circ\text{C}$ ^[2,3] 1.46 Watts
 Maximum Solder Temperature 1.59 mm (0.063 in.)
 Below Seating Plane $t < 5$ sec 260°C

Recommended Operating Conditions (HDSP-2490/-2491/-2492/-2493)

T-41-37

Parameter	Symbol	Min.	Nom.	Max.	Units	Fig.
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Data Out Current, Low State	I_{OL}			1.6	mA	
Data Out Current, High State	I_{OH}			-0.5	mA	
Column Input Voltage, Column On HDSP-2490	V_{COL}	2.4		3.5	V	4
Column Input Voltage, Column On HDSP-2491/-2492/-2493	V_{COL}	2.75		3.5	V	4
Setup Time	t_{setup}	70	45		ns	1
Hold Time	t_{hold}	30	0		ns	1
Width of Clock	$t_{w(Clock)}$	75			ns	1
Clock Frequency	f_{clock}	0		3	MHz	1
Clock Transition Time	t_{rHL}			200	ns	1
Free Air Operating Temperature Range ^{1,2}	T_A	-20		85	°C	2

Electrical Characteristics Over Operating Temperature Range

Unless otherwise specified

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Supply Current	I_{CC}	$V_{CC} = 5.25\text{V}$ $V_{CLOCK} = V_{DATA} = 2.4\text{V}$ All SR Stages = Logical 1	$V_B = 0.4\text{V}$	45	60	mA	
			$V_B = 2.4\text{V}$	73	95	mA	
Column Current at any Column Input	I_{COL}	$V_{CC} = 5.25\text{V}$ $V_{COL} = 3.5\text{V}$	$V_B = 0.4\text{V}$		500	μA	4
Column Current at any Column Input	I_{COL}	All SR Stages = Logical 1	$V_B = 2.4\text{V}$	380	520	mA	
V_B , Clock or Data Input Threshold High	V_{IH}	$V_{CC} = V_{COL} = 4.75\text{V}$	2.0			V	
V_B , Clock or Data Input Threshold Low	V_{IL}				0.8	V	
Input Current Logical 1	V_B , Clock	I_{IH}		20	80	μA	
	Data In	I_{IH}		10	40	μA	
Input Current Logical 0	V_B , Clock	I_{IL}		-500	-800	μA	
	Data In	I_{IL}		-250	-400	μA	
Data Out Voltage	V_{OH}	$V_{CC} = 4.75\text{V}$, $I_{OH} = -0.5\text{ mA}$, $I_{COL} = 0\text{ mA}$	2.4	3.4		V	
	V_{OL}	$V_{CC} = 4.75\text{V}$, $I_{OL} = 1.6\text{ mA}$, $I_{COL} = 0\text{ mA}$		0.2	0.4	V	
Power Dissipation Per Package**	P_D	$V_{CC} = 5.0\text{V}$, $V_{COL} = 3.5\text{V}$, 17.5% DF 15 LEDs on per character, $V_B = 2.4\text{V}$		0.78		W	2
Thermal Resistance IC Junction-to-Case	$R_{\theta J-C}$			20		°C/W/Device	2

*All typical values specified at $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$ unless otherwise noted

**Power dissipation per package with four characters illuminated.

Notes:

1 Operation above 85°C ambient is possible provided the following conditions are met. The junction should not exceed 125°C T_J and the case temperature as measured at pin 1 or the back of the display should not exceed 100°C T_C .

2 The device should be derated linearly above 60°C at 22.2 mW/°C. This derating is based on a device mounted in a socket having a thermal resistance from case to ambient at 25°C: W per device. See Figure 2 for power deratings based on a lower thermal resistance.

3. Maximum allowable dissipation is derived from $V_{CC} = 5.25\text{V}$, $V_B = 2.4\text{V}$, $V_{COL} = 3.5\text{V}$ 20 LEDs on per character, 20% DF.

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Optical Characteristics

STANDARD RED HDSP-2490

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED ^[4,8] (Character Average)	$I_{V\text{Peak}}$	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_1 = 25^\circ C$ ^[6] , $V_B = 2.4V$	220	370		μcd	3
Peak Wavelength	λ_{PEAK}			655		nm	
Dominant Wavelength ^[7]	λ_d			639		nm	

YELLOW HDSP-2491

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED ^[4,8] (Character Average)	$I_{V\text{Peak}}$	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_1 = 25^\circ C$ ^[6] , $V_B = 2.4V$	850	1400		μcd	3
Peak Wavelength	λ_{PEAK}			583		nm	
Dominant Wavelength ^[5,7]	λ_d			585		nm	

HIGH EFFICIENCY RED HDSP-2492

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED ^[4,8] (Character Average)	$I_{V\text{Peak}}$	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_1 = 25^\circ C$ ^[6] , $V_B = 2.4V$	850	1530		μcd	3
Peak Wavelength	λ_{PEAK}			635		nm	
Dominant Wavelength ^[7]	λ_d			626		nm	

HIGH PERFORMANCE GREEN HDSP-2493

Description	Symbol	Test Conditions	Min.	Typ.*	Max.	Units	Fig.
Peak Luminous Intensity per LED ^[4,8] (Character Average)	$I_{V\text{Peak}}$	$V_{CC} = 5.0V$, $V_{COL} = 3.5V$ $T_1 = 25^\circ C$ ^[6] , $V_B = 2.4V$	1280	2410		μcd	3
Peak Wavelength	λ_{PEAK}			568		nm	
Dominant Wavelength ^[5,7]	λ_d			574		nm	

*All typical values specified at $V_{CC} = 5.0V$ and $T_A = 25^\circ C$ unless otherwise noted.

**Power dissipation per package with four characters illuminated.

Notes:

- The characters are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.
- The HDSP-2491/-2493 are categorized for color with the color category designated by a number code on the bottom of the package.
- T_1 refers to the initial case temperature of the device immediately prior to the light measurement.

- Dominant wavelength λ_d is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
- The luminous sterance of the LED may be calculated using the following relationships:
 $L_v \text{ cd/m}^2 = I_v \text{ Candela} / A \text{ Metre}^2$
 $L_v \text{ (Footlamberts)} = \pi I_v \text{ (Candela)} / A \text{ (Foot)}^2$
 $A = 5.3 \times 10^{-8} \text{ M}^2 = 5.8 \times 10^{-7} \text{ Foot}^2$

Electrical Description

The HDSP-249X series of four character alphanumeric displays have been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features DATA IN and DATA OUT terminals arrayed for easy PC board interconnection. DATA OUT represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the displays. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5 x 7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

In the normal mode of operation, input data for digit 4 column 1 is loaded into the 7 on-board shift register locations 1 through 7. Column 1 data for digits 3, 2 and 1 is similarly shifted into the display shift register locations. The

column 1 input is now enabled for an appropriate period of time, T . A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t , then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5 \cdot t + T}$$

The time frame, $t + T$, allotted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time $t + T$ of:

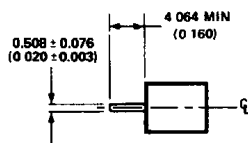
$$1/[5 \times 100] = 2 \text{ msec}$$

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain $t \ll T$. For short display strings, the duty factor will then approach 20%.

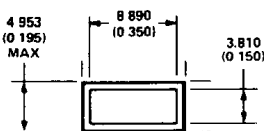
For further applications information, refer to HP Application Note 1016.

**SOLID STATE
DISPLAYS**

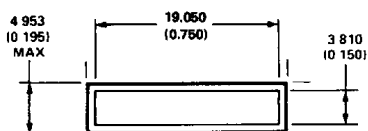
Package Dimensions



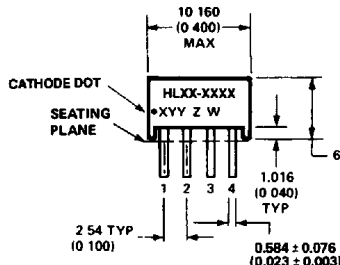
END VIEW A, B



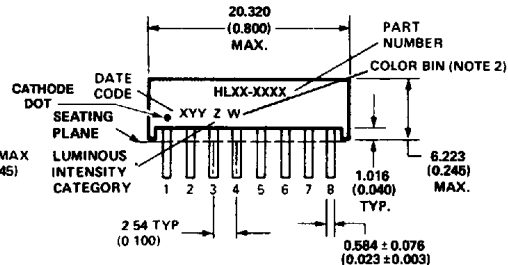
TOP A



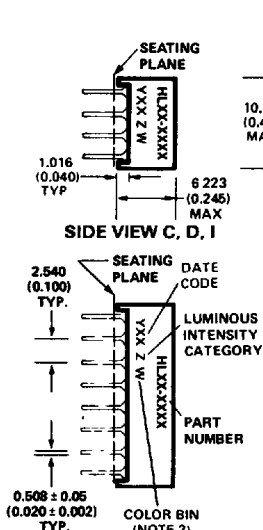
TOP B



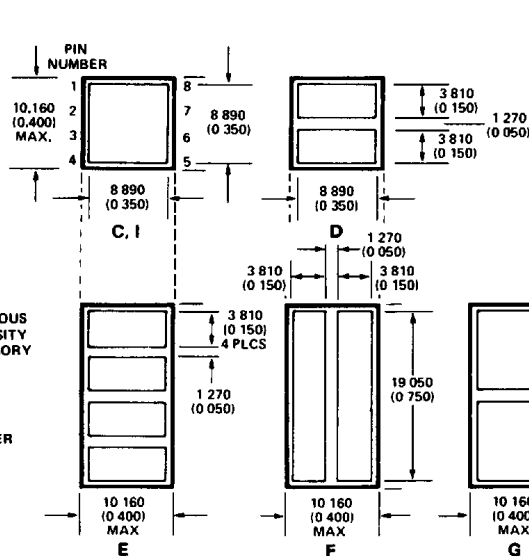
SIDE A



SIDE B



SIDE VIEW C, D, I



END VIEW C, D, E, F, G, H, I

SIDE VIEW E, F, G, H

NOTES:

1. DIMENSIONS IN MILLIMETRES (INCHES). TOLERANCES ± 0.25 mm (± 0.010 IN.) UNLESS OTHERWISE INDICATED.
2. FOR YELLOW AND GREEN DEVICES ONLY.

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