Hermetically Sealed, Very High Speed, Logic Gate Optocouplers

Technical Data

HCPL-540X* HCPL-643X
5962-89570 5962-89571
HCPL-543X

*See matrix for available extensions.

Features

- **Dual Marked with Device Part Number and DESC Drawing Number**
- **Manufactured and Tested on a MIL-PRF-38534 Certified Line**
- **QML-38534, Class H and K**
- **Three Hermetically Sealed Package Configurations**
- **Performance Guaranteed over -55°C to +125°C**
- **High Speed: 40 M bit/s**
- **High Common Mode Rejection 500 V/μs Guaranteed**
- **1500 Vdc Withstand Test Voltage**
- **Active (Totem Pole) Outputs**
- **Three Stage Output Available**
- **High Radiation Immunity**
- **HCPL-2400/30 Function Compatibility**
- **Reliability Data**
- **Compatible with TTL, STTL, LSTTL, and HCMOS Logic Families**

Applications

- **Military and Space**
- **High Reliability Systems**
- **Transportation, Medical, and Life Critical Systems**
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Switching Power Supplies**
- **Isolated Bus Driver (Networking Applications)-(5400/1 Only)**
- **Pulse Transformer Replacement**
- **Ground Loop Elimination**
- **Harsh Industrial Environments**
- **High Speed Disk Drive I/O**
- **Digital Isolation for A/D, D/A Conversion**

Description

These units are single and dual channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DESC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains an AlGaAs light emitting diode which is optically coupled to an integrated high gain photon detector. This combination results in very high

Truth Tables

(Positive Logic)

Multichannel Devices

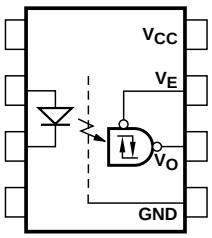
Input	Output
On (H)	H
Off (L)	L

Single Channel DIP

Input	Enable	Output
On (H)	L	L
Off (L)	L	H
On (H)	H	Z
Off (L)	H	Z

Functional Diagram

Multiple Channel Devices Available



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

data rate capability. The detector has a threshold with hysteresis, which typically provides 0.25 mA of differential mode noise immunity and minimizes the potential for output signal chatter. The detector in the single channel units has a three state output stage which eliminates the need for a pull-up resistor and allows for direct drive of a data bus.

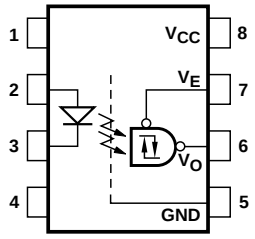
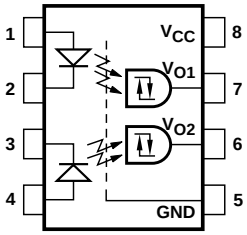
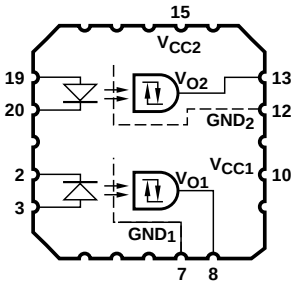
All units are compatible with TTL, STTL, LSTTL, and HCMOS logic families. The 35 ns pulse width distortion specification guarantees a 10 MBd signaling rate at +125°C with 35% pulse width distortion. Figures 13 through 16 show recommended circuits for reducing pulse width distortion and optimizing the signal rate of the product. Package styles for these parts are 8 pin DIP through hole (case outlines P), and leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are similar for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

Selection Guide–Package Styles and Lead Configuration Options

Package	**8 Pin DIP**	**8 Pin DIP**	**20 Pad LCCC**
Lead Style	Through Hole	Through Hole	Surface Mount
Channels	1	2	2
Common Channel Wiring	None	V_{CC}, GND	None
HP Part # & Options			
Commercial	HCPL-5400	HCPL-5430	HCPL-6430
MIL-PRF-38534, Class H	HCPL-5401	HCPL-5431	HCPL-6431
MIL-PRF-38534, Class K	HCPL-540K	HCPL-543K	HCPL-643K
Standard Lead Finish	Gold Plate	Gold Plate	Solder Pads
Solder Dipped	Option #200	Option #200	
Butt Cut/Gold Plate	Option #100	Option #100	
Gull Wing/Soldered	Option #300	Option #300	
SMD Part #			
Prescript for all below	5962-	5962-	5962-
Either Gold or Solder	8957001PX	8957101PX	89571022X
Gold Plate	8957001PC	8957101PC	
Solder Dipped	8957001PA	8957101PA	89571022A
Butt Cut/Gold Plate	8957001YC	8957101YC	
Butt Cut/Soldered	8957001YA	8957101YA	
Gull Wing/Soldered	8957001XA	8957101XA	

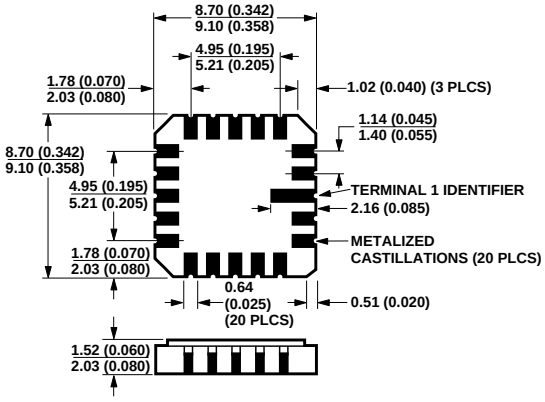
Functional Diagrams

8 Pin DIP	8 Pin DIP	20 Pad LCCC
Through Hole	Through Hole	Surface Mount
1 Channel	2 Channels	2 Channels
		

Note: All DIP devices have common V_{CC} and ground. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections.

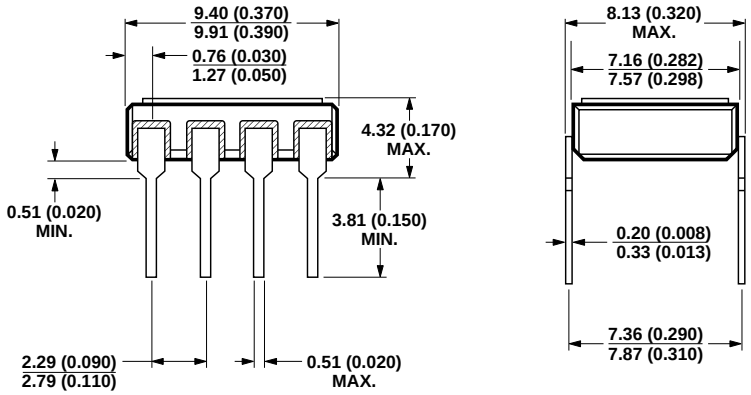
Outline Drawings

20 Terminal LCCC Surface Mount, 2 Channels



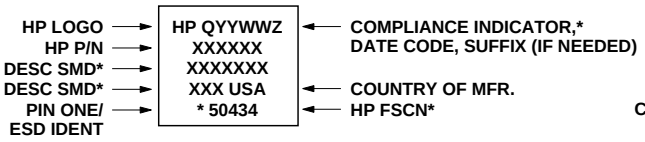
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
SOLDER THICKNESS 0.127 (0.005) MAX.

8 Pin DIP Through Hole, 1 and 2 Channel



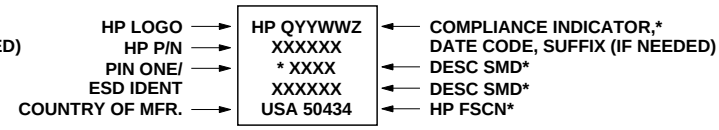
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking



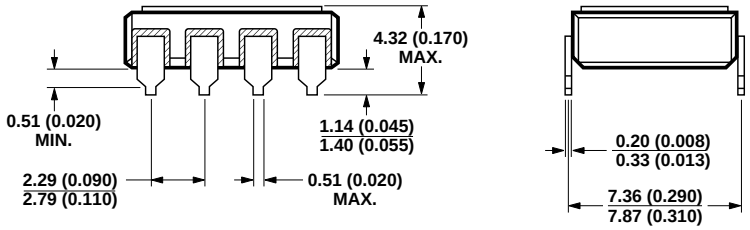
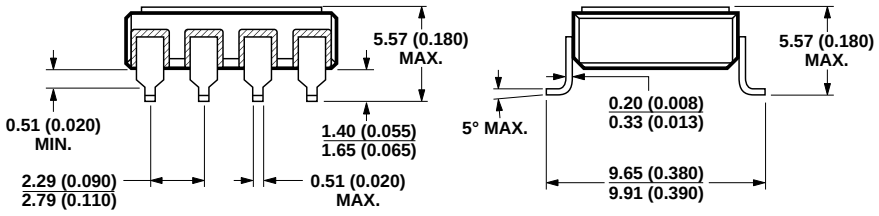
* QUALIFIED PARTS ONLY

Leadless Device Marking



* QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details).  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 pin DIP. DESC Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details). This option has solder dipped leads.  NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

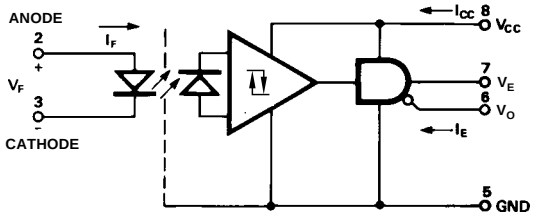
Absolute Maximum Ratings

(No derating required up to +125°C)
Storage Temperature Range, T_S ..... -65°C to +150°C
Operating Temperature, T_A ..... -55°C to +125°C
Case Temperature, T_C ..... +170°C
Junction Temperature, T_J ..... +175°C
Lead Solder Temperature ..... 260°C for 10 s
Average Forward Current, $I_{F\,AVG}$ (each channel) ..... 10 mA
Peak Input Current, $I_{F\,PK}$ (each channel) ..... 20 mA[1]
Reverse Input Voltage, V_R (each channel) ..... 3 V
Supply Voltage, V_{CC} ..... 0.0 V min., 7.0 V max.
Average Output Current, I_O ..... -25 mA min., 25 mA max. (each channel)
Output Voltage, V_O (each channel) ..... -0.5 V min., 10 V max.
Output Power Dissipation, P_O (each channel) ..... 130 mW
Package Power Dissipation, P_D (each channel) ..... 200 mW

Single Channel Product Only

Three State Enable Voltage, V_E ..... -0.5 V min., 10 V max.

8 Pin Ceramic DIP Single Channel Schematic



Note enable pin 7. An external 0.01 µF to 0.1 µF bypass capacitor must be connected between V_{CC} and ground for each package type.

ESD Classification

(MIL-STD-883, Method 3015)
HCPL-5400/01 ..... (ΔΔ), Class 2
HCPL-5430/31 and HCPL-6430/31 ..... (Dot), Class 3

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current (High)	$I_{F(ON)}$	6	10	mA
Supply Voltage, Output	V_{CC}	4.75	5.25	V
Input Voltage (Low)	$V_{F(OFF)}$	–	0.7	V
Fan Out (Each Channel)	N	–	5	TTL Loads
Single Channel Product Only				
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V

Electrical Characteristics

T_A = -55°C to +125°C, 4.5 V ≤ V_{CC} ≤ 5.25 V, 6 mA ≤ $I_{F(ON)}$ ≤ 10 mA, 0 V ≤ $V_{F(OFF)}$ ≤ 0.7 V, unless otherwise specified.

Parameter		Sym.	Test Conditions	Group A[10] Subgroups	Limits			Units	Fig.	Notes
					Min.	Typ.*	Max.			
Low Level Output Voltage		V_{OL}	I_{OL} = 8.0 mA (5 TTL Loads)	1, 2, 3		0.3	0.5	V	1	9
High Level Output Voltage		V_{OH}	I_{OH} = -4.0 mA	1, 2, 3	2.4			V	2	9
Output Leakage Current		I_{OHH}	V_O = 5.25 V, V_F = 0.7 V	1, 2, 3			100	µA		9
Logic High Supply Current	Single Channel	I_{CCH}	V_{CC} = 5.25 V, V_E = 0 V (Single Channel Only)	1, 2, 3		17	26	mA		
	Dual Channel					34	52			13
Logic Low Supply Current	Single Channel	I_{CCL}		1, 2, 3		19	26	mA		
	Dual Channel					38	52			13
Input Forward Voltage		V_F	I_F = 10 mA	1, 2, 3	1.0	1.35	1.85	V	4	9
Input Reverse Breakdown Voltage		V_R	I_R = 10 µA	1, 2, 3	3.0	4.8		V		9
Input-Output Insulation Leakage Current		I_{I-O}	V_{I-O} = 1500 Vdc, RH = 45%, t = 5 s	1			1.0	µA		2, 3
Propagation Delay Time Logic Low Output		t_{PHL}		9, 10, 11		33	60	ns	5, 6, 7	4, 9
Propagation Delay Time Logic High Output		t_{PLH}		9, 10, 11		30	60	ns	5, 6, 7	4, 9
Pulse Width Distortion		PWD		9, 10, 11		3	35	ns	5, 6, 7	4, 9
Logic High Common Mode Transient Immunity		$\|CM_H\|$	V_{CM} = 50 V_{P-P}, I_F = 0 mA	9, 10, 11	500	3000		V/µs	11	5, 9, 11
Logic Low Common Mode Transient Immunity		$\|CM_L\|$	V_{CM} = 50 V_{P-P}, I_F = 6 mA	9, 10, 11	500	3000		V/µs	11	5, 9, 11

Single Channel Product Only

Parameter	Sym.	Test Conditions	Group A[10] Subgroups	Limits			Units	Fig.	Notes
				Min.	Typ.*	Max.			
Logic High Enable Voltage	V_{EH}		1, 2, 3	2.0			V		
Logic Low Enable Voltage	V_{EL}		1, 2, 3			0.8	V		
Logic High Enable Current	I_{EH}	V_E = 2.4 V	1, 2, 3			20	µA		
		V_E = 5.25 V	1, 2, 3			100			
Logic Low Enable Current	I_{EL}	V_E = 0.4 V	1, 2, 3		-0.28	-0.4	mA		
High Impedance State Supply Current	I_{CCZ}	V_{CC} = 5.25 V, V_E = 5.25 V	1, 2, 3		22	28	mA		
High Impedance State Output Current	I_{OZL}	V_O = 0.4 V, V_E = 2 V	1, 2, 3			-20	µA		
	I_{OZH}	V_O = 2.4 V, V_E = 2 V				20			
		V_O = 5.25 V, V_E = 2 V				100			

*All typical values are at V_{CC} = 5 V, T_A = 25°C, I_F = 8 mA except where noted.

Typical Characteristics

All typical values are at T_A = 25°C, V_{CC} = 5 V, I_F = 8 mA, unless otherwise specified.

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Input Current Hysteresis	I_{HYS}	0.25	mA	V_{CC} = 5 V	3	
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$	-1.11	mV/°C	I_F = 10 mA	4	
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V		2
Capacitance (Input-Output)	C_{I-O}	0.6	pF	f = 1 MHz, V_{I-O} = 0 V		2
Logic Low Short Circuit Output Current	I_{OSL}	65	mA	V_O = V_{CC} = 5.25 V, I_F = 10 mA		6, 9
Logic High Short Circuit Output Current	I_{OSH}	-50	mA	V_{CC} = 5.25 V, I_F = 0 mA, V_O = GND		6, 9
Output Rise Time (10-90%)	t_r	15	ns		5	
Output Fall Time (90-10%)	t_f	10	ns		5	
Propagation Delay Skew	t_{PSK}	30	ns		10	12
Power Supply Noise Immunity	PSNI	0.5	V_{P-P}	48 Hz ≤ f_{ac} ≤ 50 MHz		7

Single Channel Product Only

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Notes
Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_F = 0 V, Pins 2 and 3		
Output Enable Time to Logic High	t_{PZH}	15	ns		8, 9	
Output Enable Time to Logic Low	t_{PZL}	30	ns		8, 9	
Output Disable Time from Logic High	t_{PHZ}	20	ns		8, 9	
Output Disable Time from Logic Low	t_{PLZ}	15	ns		8, 9	

Dual and Quad Channel Product Only

Input Capacitance	C_{IN}	15	pF	f = 1 MHz, V_O = 0 V		
Input-Input Leakage Current	I_{I-I}	0.5	nA	RH = 45%, V_{I-I} = 500 Vdc		8
Input-Input Resistance	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 V		8
Input-Input Capacitance	C_{I-I}	1.3	pF	f = 1 MHz, V_F = 0 V		8

Notes:

1. Not to exceed 5% duty factor, not to exceed 50 µsec pulse width.
2. All devices are considered two-terminal devices: measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
3. This is a momentary withstand test, not an operating condition.
4. t_{PHL} propagation delay is measured from the 50% point on the rising edge of the input current pulse to the 1.5 V point on the falling edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the falling edge of the input current pulse to the 1.5 V point on the rising edge of the output pulse. Pulse Width Distortion, PWD = $|t_{PHL} - t_{PLH}|$.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_{O(MAX)}$ < 0.8 V). CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_{O(MIN)}$ > 2.0 V).
6. Duration of output short circuit time not to exceed 10 ms.
7. Power Supply Noise Immunity is the peak to peak amplitude of the ac ripple voltage on the V_{CC} line that the device will withstand and still remain in the desired logic state. For desired logic high state, $V_{OH(MIN)}$ > 2.0 V, and for desired logic low state, $V_{OL(MAX)}$ < 0.8 V.
8. Measured between adjacent input pairs shorted together for each multichannel device.
9. Each channel.
10. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and hi-rel parts receive 100% testing at 25, 125, and –55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
11. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.
12. Propagation delay skew is defined as the difference between the minimum and maximum propagation delays for any given group of optocouplers with the same part number that are all switching at the same time under the same operating conditions.
13. The HCPL-6430 and HCPL-6431 dual channel parts function as two independent single channel units. Use the single channel parameter limits.

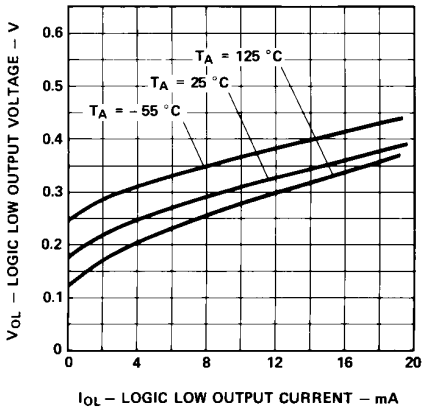


Figure 1. Typical Logic Low Output Voltage vs. Logic Low Output Current.

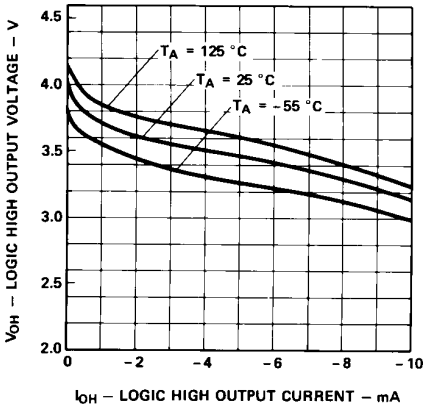


Figure 2. Typical Logic High Output Voltage vs. Logic High Output Current.

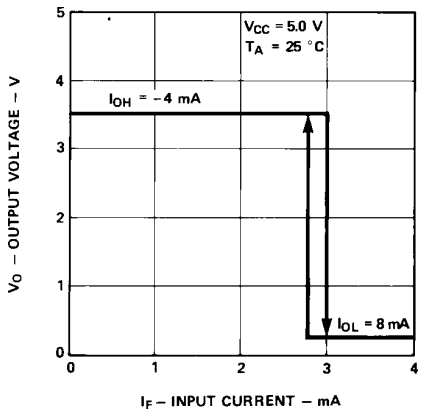


Figure 3. Typical Output Voltage vs. Input Forward Current.

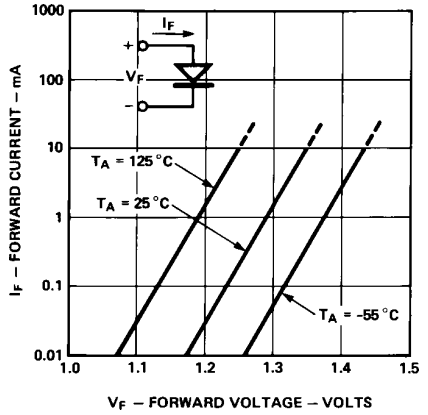
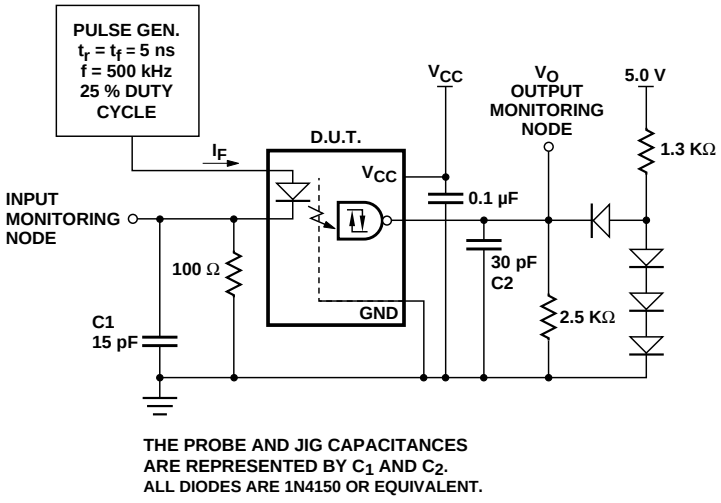


Figure 4. Typical Diode Input Forward Current Characteristic.



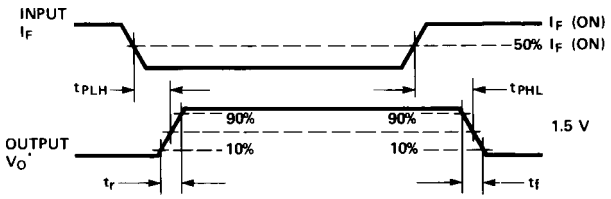


Figure 5. Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f.

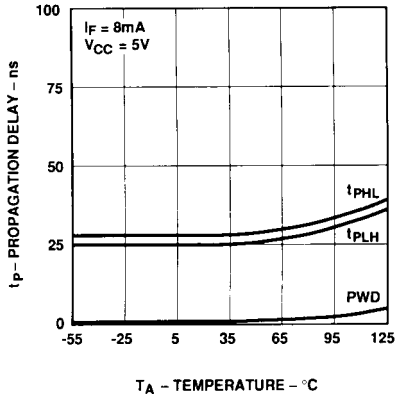


Figure 6. Typical Propagation Delay vs. Ambient Temperature.

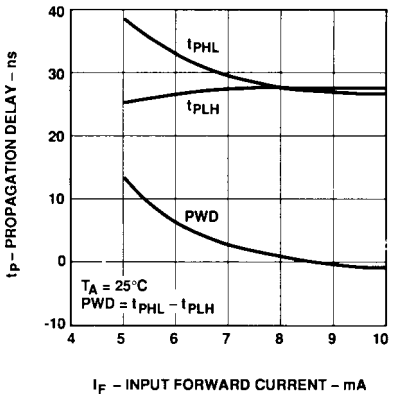
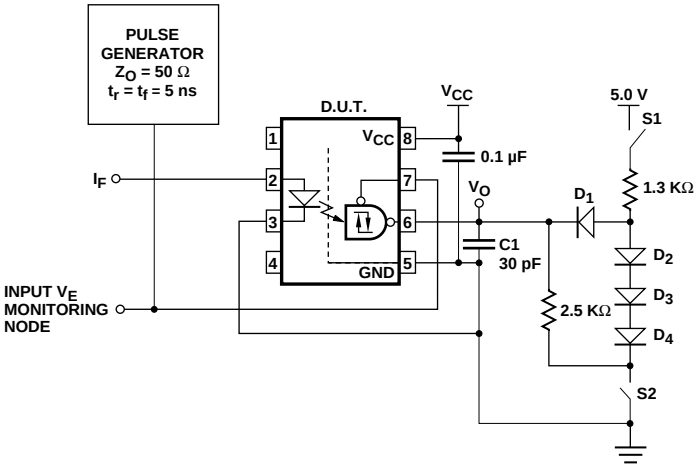
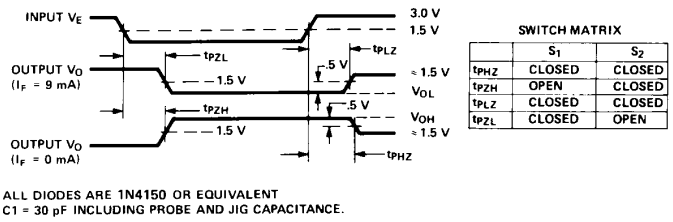


Figure 7. Typical Propagation Delay vs. Input Forward Current.





SWITCH MATRIX

	S_1	S_2
t_{PHZ}	CLOSED	CLOSED
t_{PZH}	OPEN	CLOSED
t_{PLZ}	CLOSED	CLOSED
t_{PZL}	CLOSED	OPEN

ALL DIODES ARE 1N4150 OR EQUIVALENT
C1 = 30 pF INCLUDING PROBE AND JIG CAPACITANCE.

Figure 8. Test Circuit for t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL}. (Single Channel Product Only).

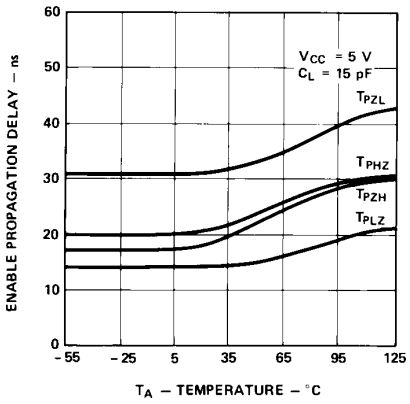


Figure 9. Typical Enable Propagation Delay vs. Ambient Temperature. (Single Channel Product Only).

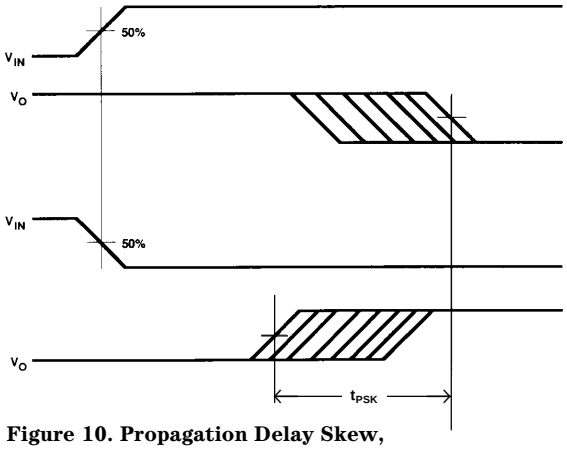
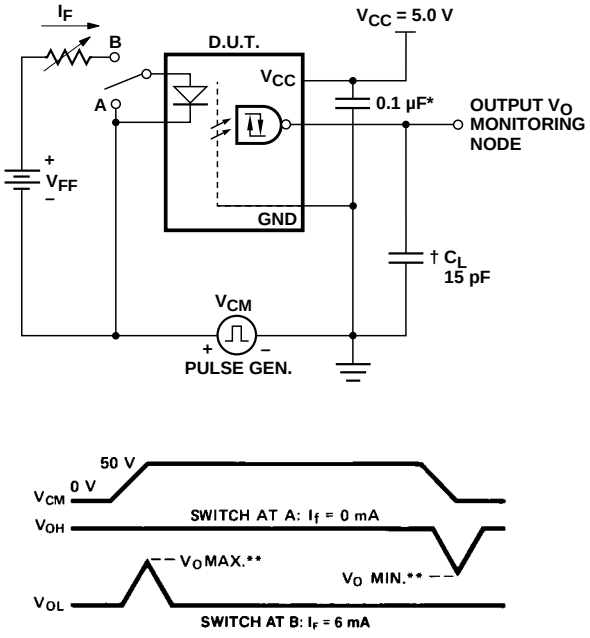
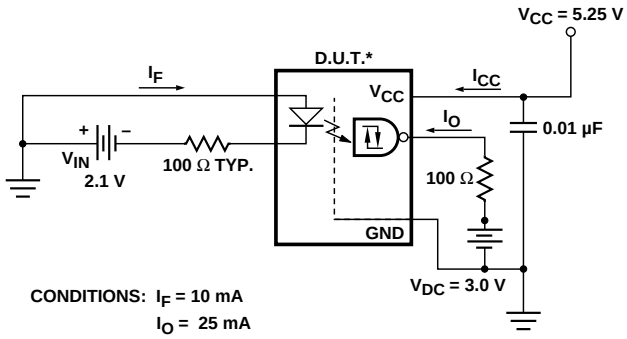


Figure 10. Propagation Delay Skew, t_{PSK}, Waveform.



*TOTAL LEAD LENGTH < 10 mm FROM DEVICE UNDER TEST.
**SEE NOTE 5.
†C_L IS APPROXIMATELY 15 pF, WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

Figure 11. Test Diagram for Common Mode Transient Immunity and Typical Waveforms.



CONDITIONS: I_F = 10 mA
I_O = 25 mA

T_A = +125 °C

* FOR SINGLE CHANNEL UNITS, GROUND ENABLE PIN.

Figure 12. Operating Circuit for Burn-In and Steady State Life Tests.

MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H devices are also in compliance with DESC drawings 5962-89570, and 5962-89571.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

Data Rate and Pulse-Width Distortion Definitions

Propagation delay is a figure of merit which describes the finite amount of time required for a system to translate information from input to output when shifting logic levels. Propagation delay from low to high (t_{PLH}) specifies the amount of time required for a system's output to change from a Logic 0 to a Logic 1, when given a stimulus at the input. Propagation delay from high to low (t_{PHL}) specifies the amount of time required for a system's output to change from a Logic 1 to a Logic 0, when given a stimulus at the input (see Figure 5).

When t_{PLH} and t_{PHL} differ in value, pulse width distortion results. Pulse width distortion is defined as $|t_{PHL} - t_{PLH}|$ and determines the maximum data rate capability of a distortion-limited system. Maximum pulse width distortion on the order of 25-35% is typically used when specifying the maximum data rate capabilities of systems. The exact figure depends on the particular application (RS-232, PCM, T-1, etc.).

These high performance optocouplers offer the advantages of specified propagation delay (t_{PLH}, t_{PHL}), and pulse width distortion ($|t_{PLH} - t_{PHL}|$) over temperature and power supply voltage ranges.

Applications

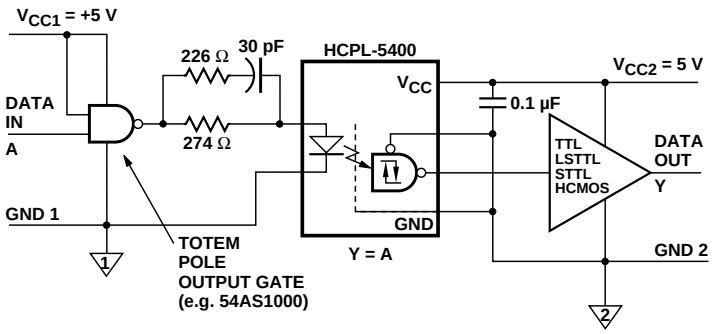


Figure 13. Recommended HCPL-5400 Interface Circuit.

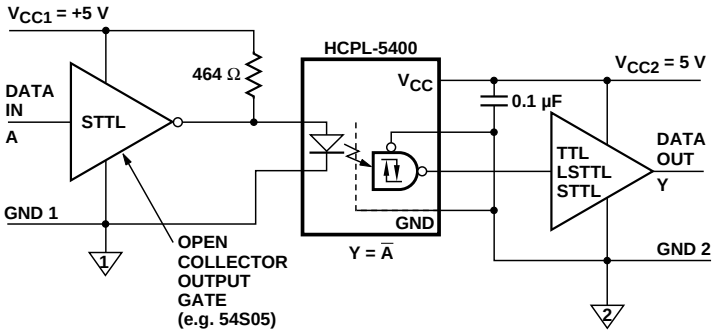


Figure 14. Alternative HCPL-5400 Interface Circuit.

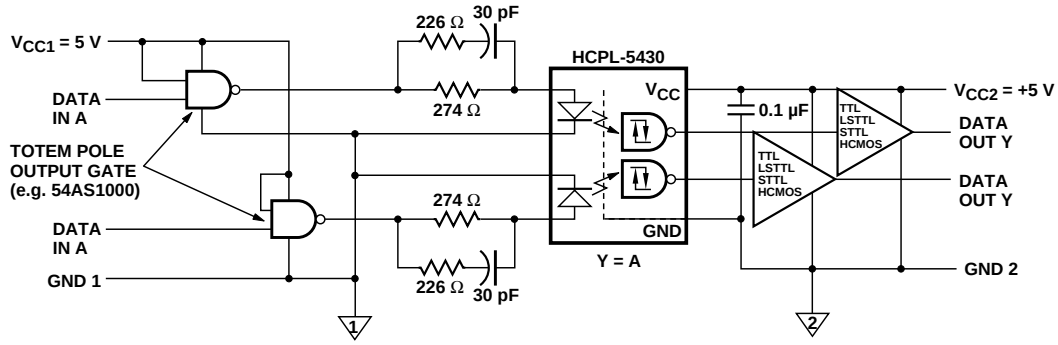


Figure 15. Recommended HCPL-5430 and HCPL-6430 Interface Circuit.

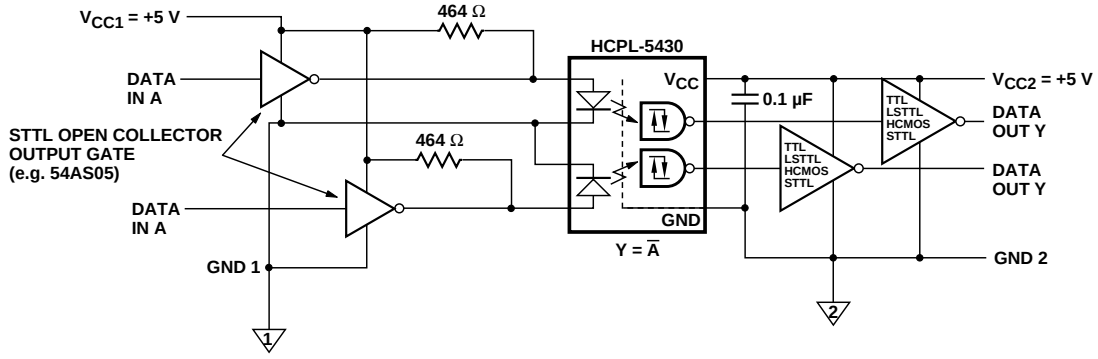


Figure 16. Alternative HCPL-5430 and HCPL-6430 Interface Circuit.