R8822
Datasheet
16-BIT RISC MICRO-CONTROLLER

RDC ***RISC DSP Communication***

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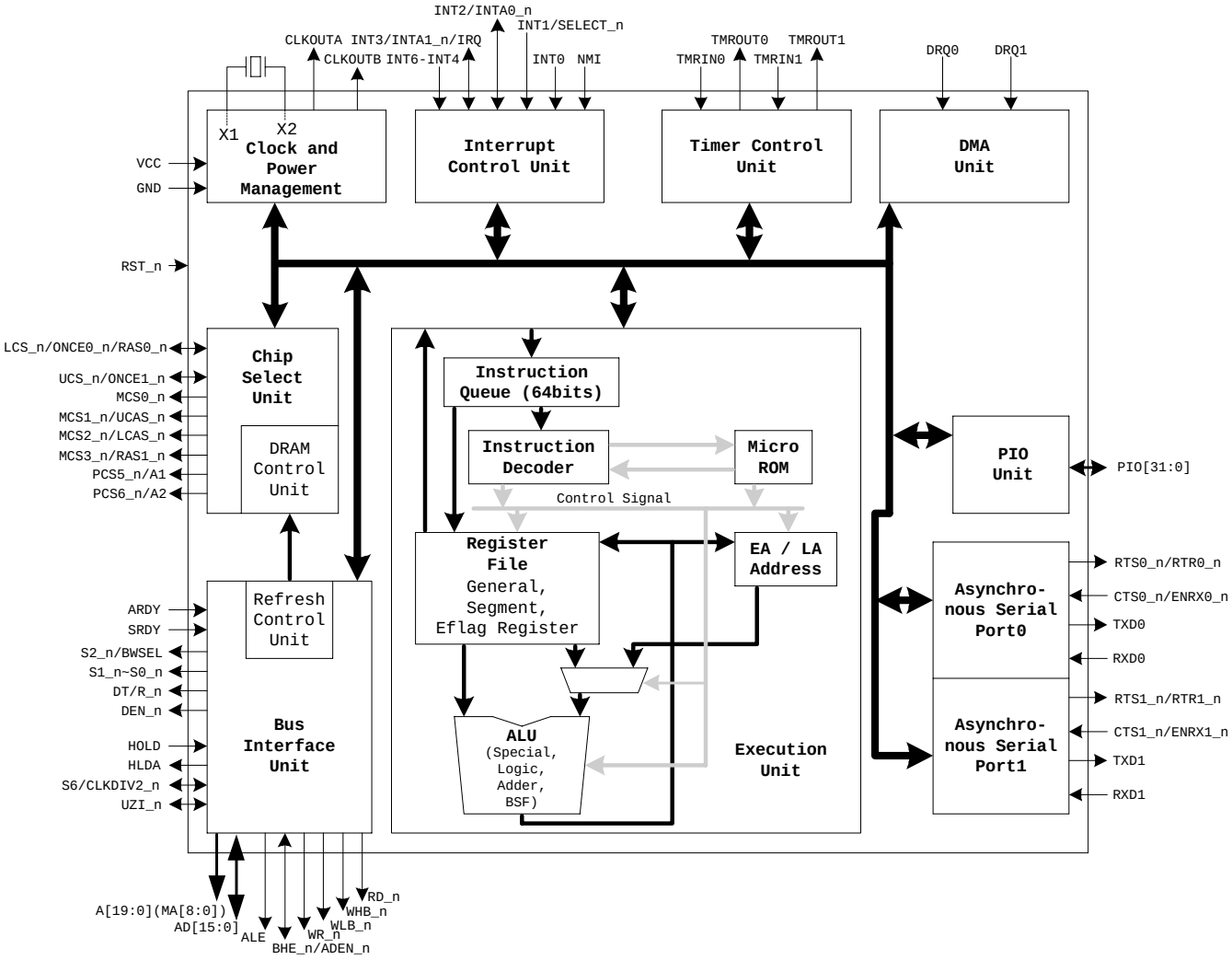
CONTENTS

~~1.~~16-Bit Micro-controller with 8-Bit or 16-Bit External Data Bus

1. Features

- Five-stage pipeline
- RISC architecture
- Static & synthesizable design
- Bus interface
  - Multiplexed address and data bus
  - Supports a non-multiplexed address bus A[19:0]
  - 8-bit or 16-bit external bus dynamic access
  - 1M-byte memory address space
  - 64K-byte I/O space
- Software is compatible with the 80C186 microprocessor
- Supports two asynchronous serial channels with hardware handshaking signals.
- Supports CPU ID
- Supports 32 PIO pins
- Supports 64Kx16, 128Kx16, 256Kx16 EDO or FP DRAM with auto-refresh control
- Three independent 16-bit timers and one independent programmable watchdog timer
- The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt
- Two independent DMA channels
- Programmable chip-select logic for memory or I/O bus cycle decoder
- Programmable wait-state generators
- With 8-bit or 16-bit boot ROM bus size

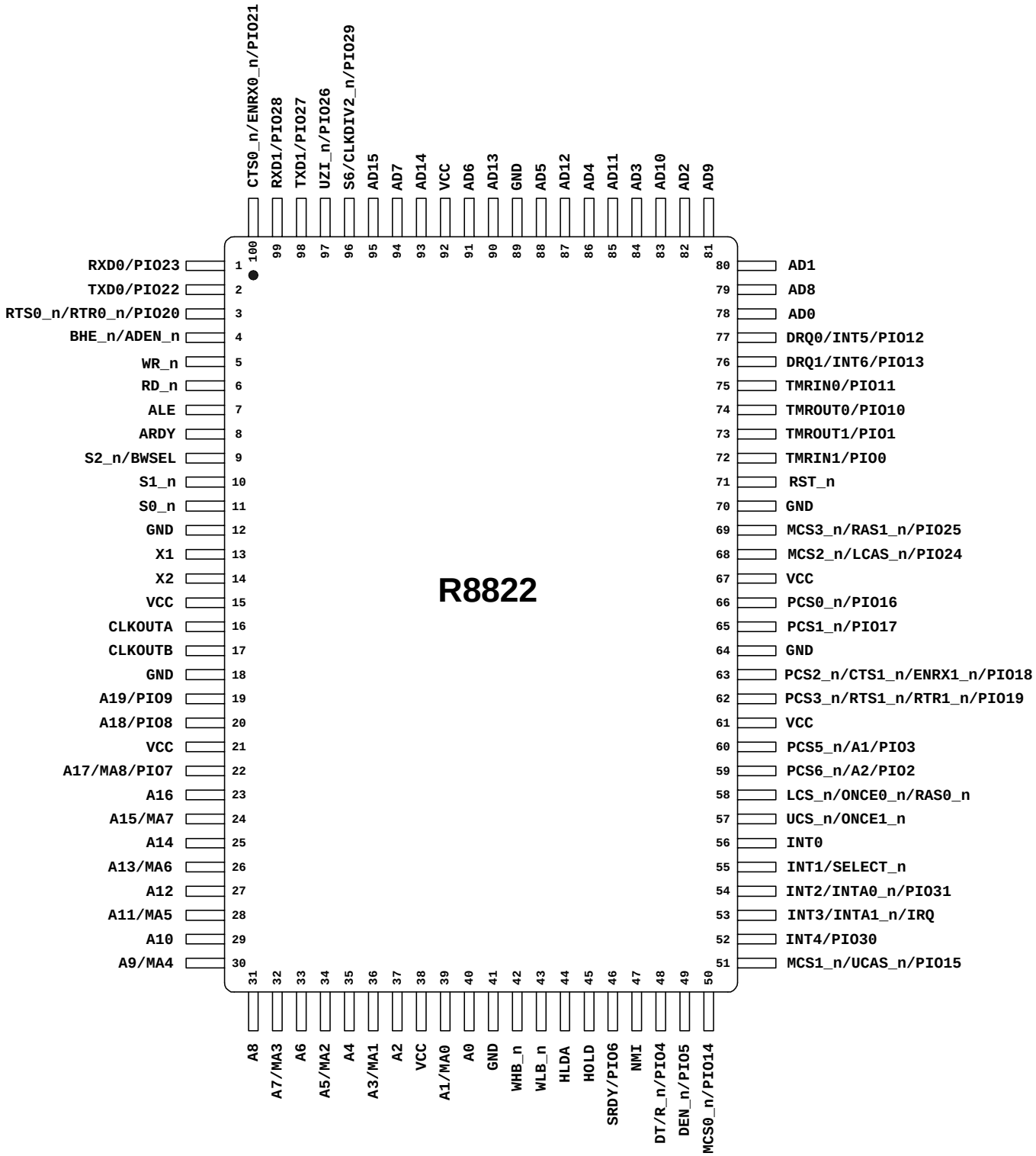
2. Block Diagram



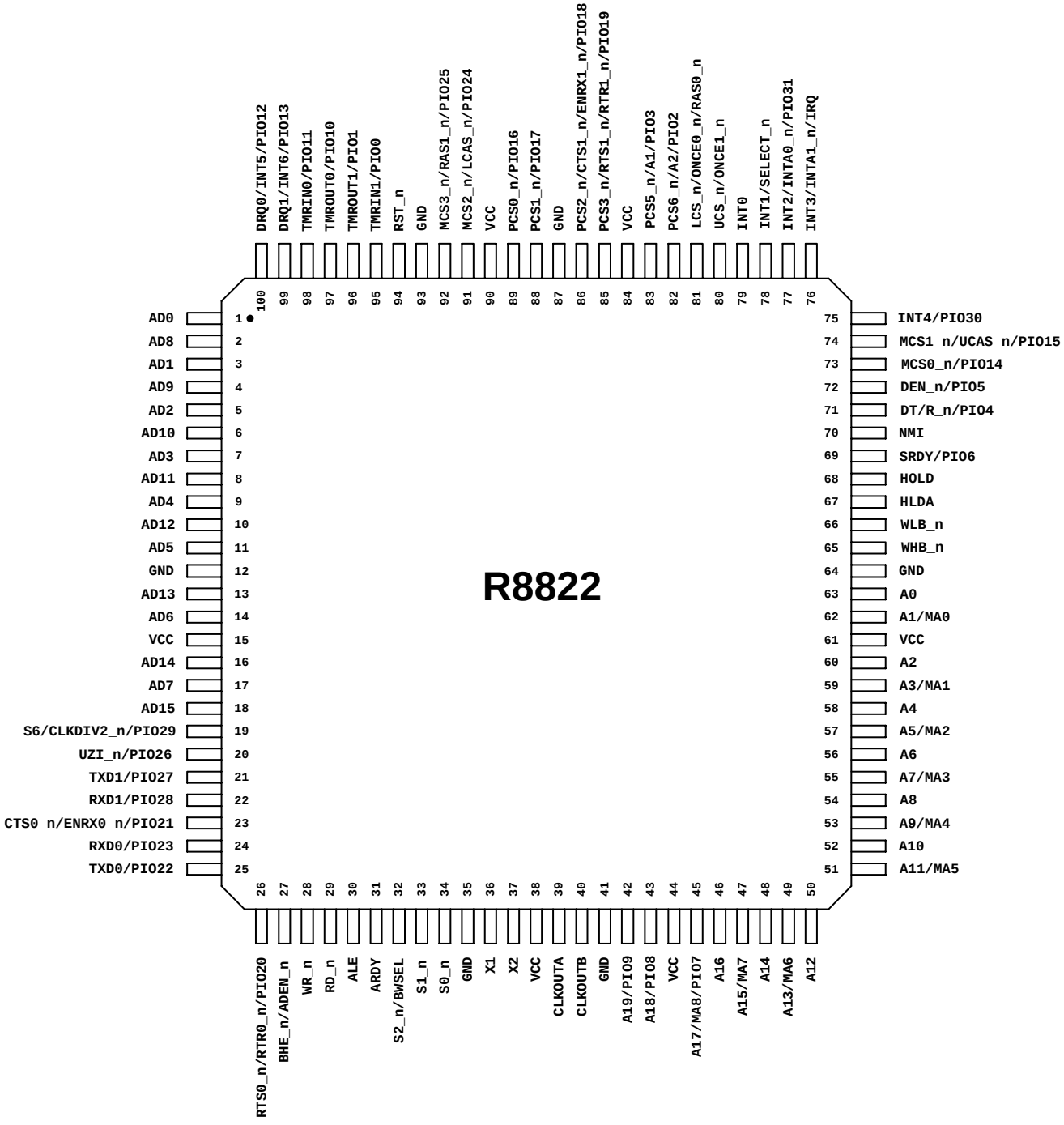
3. Pin Description

3.1 Pin Placement

3.1.1 PQFP



3.1.2 LQFP


R8822
1 AD0
2 AD8
3 AD1
4 AD9
5 AD2
6 AD10
7 AD3
8 AD11
9 AD4
10 AD12
11 AD5
12 GND
13 AD13
14 AD6
15 VCC
16 AD14
17 AD7
18 AD15
19 S6/CLKDIV2_n/PIO29
20 UZI_n/PIO26
21 TXD1/PIO27
22 RXD1/PIO28
23 CTS0_n/ENRX0_n/PIO21
24 RXD0/PIO23
25 TXD0/PIO22
26 RTS0_n/RTR0_n/PIO20
27 BHE_n/ADEN_n
28 WR_n
29 RD_n
30 ALE
31 ARDY
32 S2_n/BWSEL
33 S1_n
34 S0_n
35 GND
36 X1
37 X2
38 VCC
39 CLKOUTA
40 CLKOUTB
41 GND
42 A19/PIO9
43 A18/PIO8
44 VCC
45 A17/MA8/PIO7
46 A16
47 A15/MA7
48 A14
49 A13/MA6
50 A12
51 A11/MA5
52 A10
53 A9/MA4
54 A8
55 A7/MA3
56 A6
57 A5/MA2
58 A4
59 A3/MA1
60 A2
61 VCC
62 A1/MA0
63 A0
64 GND
65 WHB_n
66 WLB_n
67 HLDA
68 HOLD
69 SRDY/PIO6
70 NMI
71 DT/R_n/PIO4
72 DEN_n/PIO5
73 MCS0_n/PIO14
74 MCS1_n/UCAS_n/PIO15
75 INT4/PIO30
76 INT3/INTA1_n/IRQ
77 INT2/INTA0_n/PIO31
78 INT1/SELECT_n
79 INT0
80 UCS_n/ONCE1_n
81 LCS_n/ONCE0_n/RAS0_n
82 PCS6_n/A2/PIO2
83 PCS5_n/A1/PIO3
84 VCC
85 PCS3_n/RTS1_n/RTR1_n/PIO19
86 PCS2_n/CTS1_n/ENRX1_n/PIO18
87 GND
88 PCS1_n/PIO17
89 PCS0_n/PIO16
90 VCC
91 MCS2_n/LCAS_n/PIO24
92 MCS3_n/RAS1_n/PIO25
93 GND
94 RST_n
95 TMRIN1/PIO0
96 TMROUT1/PIO1
97 TMROUT0/PIO10
98 TMRIN0/PIO11
99 DRQ1/INT6/PIO13
100 DRQ0/INT5/PIO12

3.2 R8822 PQFP & LQFP Pin-Out Table

Pin Name	LQFP Pin No.	PQFP Pin No.	Pin Name	LQFP Pin No.	PQFP Pin No.
AD0	1	78	A11/MA5	51	28
AD8	2	79	A10	52	29
AD1	3	80	A9/MA4	53	30
AD9	4	81	A8	54	31
AD2	5	82	A7/MA3	55	32
AD10	6	83	A6	56	33
AD3	7	84	A5/MA2	57	34
AD11	8	85	A4	58	35
AD4	9	86	A3/MA1	59	36
AD12	10	87	A2	60	37
AD5	11	88	VCC	61	38
GND	12	89	A1/MA0	62	39
AD13	13	90	A0	63	40
AD6	14	91	GND	64	41
VCC	15	92	WHB_n	65	42
AD14	16	93	WLB_n	66	43
AD7	17	94	HLDA	67	44
AD15	18	95	HOLD	68	45
S6/CLKDIV2_n/PIO29	19	96	SRDY/PI O6	69	46
UZI_n/PIO26	20	97	NMI	70	47
TXD1/PIO27	21	98	DT/R_n/PIO4	71	48
RXD1/PIO28	22	99	DEN_n/PIO5	72	49
CTS0_n/ENRX0_n/PIO21	23	100	MCS0_n/PIO14	73	50
RXD0/PIO23	24	1	MCS1_n/UCAS_n/PIO15	74	51
TXD0/PIO22	25	2	INT4/PIO30	75	52
RTS0_n/RTR0_n/PIO20	26	3	INT3/INTA1_n/IRQ	76	53
BHE_n/ADEN_n	27	4	INT2/INTA0_n/PIO31	77	54
WR_n	28	5	INT1/SELECT_n	78	55
RD_n	29	6	INT0	79	56
ALE	30	7	UCS_n/ONCE1_n	80	57
ARDY	31	8	LCS_n/ONCE0_n/RAS0_n	81	58
S2_n/BWSEL	32	9	PCS6_n/A2/PIO2	82	59
S1_n	33	10	PCS5_n/A1/PIO3	83	60
S0_n	34	11	VCC	84	31
GND	35	12	PCS3_n/RTS1_n/RTR1_n/PIO19	85	62
X1	36	13	PCS2_n/CTS1_n/ENRX1_n/PIO18	86	63
X2	37	14	GND	87	64
VCC	38	15	PCS1_n/PIO17	88	65
CLKOUTA	39	16	PCS0_n/PIO16	89	66
CLKOUTB	40	17	VCC	90	67
GND	41	18	MCS2_n/LCAS_n/PIO24	91	68
A19/PIO9	42	19	MCS3_n/RAS1_n/PIO25	92	69
A18/PIO8	43	20	GND	93	70
VCC	44	21	RST_n	94	71
A17/MA8/PIO7	45	22	TMRIN1/PIO0	95	72
A16	46	23	TMROUT1/PIO1	96	73
A15/MA7	47	24	TMROUT0/PIO10	97	74
A14	48	25	TMRIN0/PIO11	98	75
A13/MA6	49	26	DRQ1/INT6/PIO13	99	76
A12	50	27	DRQ0/INT5/PIO12	100	77

3.3 Functional Description

I = Input;

O = Output;

● CPU Core

PIN No. (PQFP)	Symbol	Type	Description
15, 21, 38, 61, 67, 92	VCC	I	System power: +5 volt power supply.
12, 18, 41, 64, 70, 89	GND	I	System ground.
71	RST_n	I	~~Reset input~~Reset Input. When RST_n is asserted, the CPU immediately terminates all operations, clears the internal registers & logic, and transfers the address to the reset address FFFF0h.
13	X1	I	Input to the oscillator amplifier.
14	X2	O	Output from the inverting oscillator amplifier.
16	CLKOUTA	O	Clock Output A. CLKOUTA operates at the crystal input frequency (X1). CLKOUTA remains active during reset and bus hold conditions.
17	CLKOUTB	O	Clock Output B. CLKOUTB operates at the crystal input frequency (X1). CLKOUTB remains active during reset and bus hold conditions.

● Asynchronous Serial Port Interface

PIN No. (PQFP)	Symbol	Type	Description
1	RXD0/PIO23	I/O	Receive Data for Asynchronous Serial Port 0. This pin receives asynchronous serial data.
2	TXD0/PIO22	O/I	Transmit Data for Asynchronous Serial Port 0. This pin transmits asynchronous serial data from the UART of the micro-controllers.
3	RTS0_n/RTR0_n/PIO20	O/I	Ready to Send/Ready to Receive Signals for Asynchronous Serial Port 0. When the RTS0 bit in the AUXCON register is set and the FC bit in the Serial Port 0 Control register is set, the RTS0_n signal is enabled. Otherwise, when the RTS0 bit is cleared and the FC bit is set, the RTR0_n signal is enabled.
100	CTS0_n/ENRX0_n/PIO21	I/O	Clear to Send/Enable Receiver Request Signals for Asynchronous Serial Port 0. When the ENRX0 bit in the AUXCON register is cleared and the FC bit in the Serial Port 0 Control register is set, the CTS0_n signal is enabled. Otherwise, when the ENRX0 bit is set and the FC bit is set, the ENRX0_n signal is enabled.
98	TXD1/PIO27	O/I	Transmit Data for Asynchronous Serial Port 1. This pin transmits asynchronous serial data from the UART of the micro-controllers.
99	RXD1/PIO28	I/O	Receive Data for Asynchronous Serial Port 1. This pin receives asynchronous serial data.

62	PCS3_n/RTS1_n/RTR1_n /PIO19	O/I	Ready to Send/Ready to Receive Signals for Asynchronous Serial Port 1. When the RTS1 bit in the AUXCON register is set and FC bit in the Serial Port 1 Control register is set, the RTS1_n signal is enabled. Otherwise, when the RTS1 bit is cleared and the FC bit is set, the RTR1_n signal is enabled.
63	PCS2_n/CTS1_n /ENRX1_n/PIO18	I/O	Clear to Send/Enable Receiver Request Signals for Asynchronous Serial Port 1. When the ENRX1 bit in the AUXCON register is cleared and the FC bit in the Serial Port 1 Control register is set, the CTS1_n signal is enabled. Otherwise, when the ENRX1 bit is set and the FC bit is set, the ENRX1_n signal is enabled.

● Bus Interface

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td rowspan="5">4</td><td rowspan="5">BHE_n/ADEN_n</td><td rowspan="5">O/I</td><td>Bus High Enable/Address Enable. During a memory access, the BHE_n and (AD0 or A0) encodings indicate types of the bus cycle. BHE_n is asserted during T1 and keeps the asserted to T3 and Tw. This pin is floating during bus holds and resets.</td></tr>
<tr><td>BHE_n and (AD0 or A0) Encodings</td></tr>
<tr><td>
<table>
<tr><th>BHE_n</th><th>AD0 or A0</th><th>Types of Bus Cycle</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>Word transfer
High byte transfer (D[15:8])
Low byte transfer (D[7:0])
Refresh</td></tr>
</table>
</td></tr>
<tr><td>The address portion of the AD bus can be enabled or disabled by the DA bit in the LMCS and UMCS register during LCS or UCS bus cycle accesses if BHE_n/ADEN_n is held high during power-on resets. No external pull-up resistor is required because BHE_n/ADEN_n is with a weak internal pull-up resistor. The AD bus always drives both addresses and data during LCS or UCS bus cycle accesses if the BHE_n/ADEN_n pin is with an external pull-low resistor during resets.</td></tr>
<tr><td></td></tr>
<tr><td>5</td><td>WR_n</td><td>O</td><td>Write Strobe. This pin indicates that the data on the bus is to be written into a memory or an I/O device. WR_n is active during T2, T3 and Tw of any write cycle, floating during a bus hold or reset.</td></tr>
<tr><td>6</td><td>RD_n</td><td>O</td><td>Read Strobe. It’s an active low signal indicates that the micro-controller is performing a memory or I/O read cycle. RD_n is floating during a bus hold or reset.</td></tr>
<tr><td>7</td><td>ALE</td><td>O</td><td>Address Latch Enable. Active high. This pin indicates that an address output on the AD bus. The address is guaranteed to be valid on the trailing edge of ALE. This pin is tri-stated during ONCE mode and never floating during a bus hold or reset.</td></tr>
<tr><td>8</td><td>ARDY</td><td>I</td><td>Asynchronous Ready. This pin indicates to the micro-controller that the address memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUTA and is active high. The falling edge of ARDY must be synchronized to CLKOUTA. Tie ARDY high, so the micro-controller is always asserted in ready condition. If ARDY is not used, tie this pin low to yield control to SRDY.
Both SRDY and ARDY should be tied to high if the system need not assert wait-states by externality.</td></tr>
</table>

<table>
<tr>
<td>9
10
11</td>
<td>S2_n/BWSEL
S1_n
S0_n</td>
<td>O/I
O
O</td>
<td>Bus Cycle Status. These pins are encoded to indicate the bus status. S2_n can be used as memory or I/O indicator. S1_n can be used as DT/R_n indicator. These pins are floating during bus holds and resets.
S2_n/BWSEL is to decide the boot ROM bus width when the RST_n pin goes from low to high. If S2_n/BWSEL is with a pull-low resistor (330 ohm), the boot ROM bus width is 8 bits. Otherwise, the boot ROM bus width is 16 bits.
<table>
<tr><td colspan="4">Bus Cycle Encoding Description</td></tr>
<tr><td>S2_n</td><td>S1_n</td><td>S0_n</td><td>Bus Cycle</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read data from I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write data to I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read data from memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write data to memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
</td>
</tr>
<tr>
<td>19
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35
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39
40</td>
<td>A19/PIO9
A18/PIO8
A17/MA8/PIO7
A16
A15/MA7
A14
A13/MA6
A12
A11/M15
A10
A9/MA4
A8
A7/MA3
A6
A5/MA2
A4
A3/MA1
A2
A1/MA0
A0</td>
<td>O/I</td>
<td>Address Bus. Non-multiplexed memory or I/O addresses. The A bus is one half of a CLKOUTA period earlier than the AD bus. These pins are high-impedance during bus holds or resets.

MA[8:0]: DRAM Address Interface. The MA bus is multiplexed with A bus. When the DRAM is accessed, the bus performs row or column address, otherwise the bus performs address bus.</td>
</tr>
<tr>
<td>94, 91, 88, 86, 84, 82, 80, 78
95, 93, 90, 87, 85, 83, 81, 79</td>
<td>AD[7:0]

AD[15:8]</td>
<td>I/O</td>
<td>The Multiplexed Address and Data Bus for Memory or I/O Accesses. The address is present during the t1 clock phase and the data bus phase is in t2-t4 cycle.
The address phase of the AD bus cannot be disabled when the BHE_n/ADEN_n pin is with an external pull-low resistor during resets.
The AD bus is in high-impedance state during bus hold or reset conditions. This bus can also be used to load system configuration information (with pull-up or pull-low resistors) into the RESCON register when the reset input goes from low to high.</td>
</tr>
<tr>
<td>42</td>
<td>WHB_n</td>
<td>O</td>
<td>Write High Byte. This pin indicates that the high byte data (AD[15:8]) on the bus is to be written to a memory or I/O device. WHB_n is the logic OR of BHE_n and WR_n.
This pin is floating during resets or bus holds.</td>
</tr>
</table>

43	WLB_n	O	Write Low Byte. This pin indicates that the low byte data (AD[7:0]) on the bus is to be written to a memory or I/O device. WLB_n is the logic OR of WR_n and A0. This pin is floating during resets or bus holds.
44	HLDA	O	Bus Hold Acknowledge. Active high. The micro-controller will issue an HLDA in response to a HOLD request by the external bus master at the end of T4 or Ti. When the micro-controller is in hold status (HLDA is high), AD[15:0], A[19:0], WR_n, RD_n, DEN_n, S0_n–S2_n, S6, BHE_n, DT/R_n, WHB_n and WLB_n are floating, and UCS_n, LCS_n, PCS6_n–PCS5_n, MCS3_n–MCS0_n and PCS3_n–PCS0_n will be driven high. After HOLD is detected as being low, the micro-controller will lower HLDA.
45	HOLD	I	Bus Hold Request. Active high. This pin indicates that another bus master is requesting the local bus.
46	SRDY/PIO6	I/O	Synchronous Ready. This pin indicates to the micro-controller that the address memory space or I/O device will complete a data transfer. The SRDY pin accepts a falling edge that is asynchronous to CLKOUTA and is active high. SRDY is accomplished by elimination of the one-half clock period required to internally synchronize ARDY. Tie SRDY high, so the micro-controller is always asserted in ready condition. If SRDY is not used, tie this pin low to yield control to ARDY. Both SRDY and ARDY should be tied to high if the system need not assert wait-states by externality.
48	DT/R_n/PIO4	O/I	Data Transmit or Receive. This pin indicates the direction of data flow through an external data-bus transceiver. When DT/R_n is asserted low, the micro-controller receives data. When DT/R_n is asserted high, the micro-controller writes data to the data bus.
49	DEN_n/PIO5	O/I	Data Enable. This pin is provided as a data bus transceiver output enable. DEN_n is asserted during memory and I/O accesses. DEN_n is driven high when DT/R_n changes states. It is floating during bus hold or reset conditions.
96	S6/CLKDIV2_n/PIO29	O/I	Bus Cycle Status bit6/Clock Divided by 2. For S6 feature, this pin is set to low to indicate a micro-controller-initiated bus cycle or high to indicate a DMA-initiated bus cycle during T2, T3, Tw and T4. For CLKDIV2_n feature, the internal clock of the micro-controller is the external clock divided by 2 (CLKOUTA, CLKOUTB=X1/2) if this pin is held low during power-on resets. The pin is sampled on the rising edge of RST_n.
97	UZI_n/PIO26	O/I	Upper Zero Indicate. This pin is the logical OR of the inverted A[19:16]. It is asserted in the T1 and held throughout the cycle.

● Chip Select Unit Interface

PIN No.	Symbol	Type	Description
50 51 68 69	MCS0_n/PIO14 MCS1_n/UCAS_n/PIO15 MCS2_n/LCAS_n/PIO24 MCS3_n/RAS1_n/PIO25	O/I	Midrange Memory Chip Selects. For MCS_n feature, these pins are active low when the MMCS register is enabled to access a memory. The address ranges are programmable. MCS3_n–MCS0_n are held high during bus holds. When bit 6 of the UMCS (A0h) register is set to 1, UCS_n will be disabled and MCS3_n–MCS1_n will be activated as bank1 control signals RAS1_n, LCAS_n and UCAS_n of the DRAM controller. The DRAM memory is located from 80000h to FFFFFh.
57	UCS_n/ONCE1_n	O/I	Upper Memory Chip Select/ONCE Mode Request 1. For UCS_n feature, this pin is active low when the system accesses the defined upper 512K-byte (80000h-FFFFFh) memory block. UCS_n defaults to active from F0000h to FFFFFh after power-on resets. UCS_n address range is programmed by software. For ONCE1_n feature, if ONCE0_n and ONCE1_n are sampled low on the rising edge of RST_n, the micro-controller enters ONCE mode. In ONCE mode, all pins are high-impedance. This pin incorporates a weak pull-up resistor.
58	LCS_n/ONCE0_n/RAS0_n	O/I	Lower Memory Chip Select/ONCE Mode Request 0. For LCS_n feature, this pin is active low when the micro-controller accesses the defined lower 512K-byte (00000h-7FFFFh) memory block. LCS_n address range is programmed by software. For ONCE0_n feature, please see UCS_n/ONCE1_n description. This pin incorporates a weak pull-up resistor. When bit 6 of the LMCS (A2h) register is set to 1, this pin will be activated as RAS0_n which is the row address of DRAM bank 0.
59 60	PCS6_n/A2/PIO2 PCS5_n/A1/PIO3	O/I	Peripheral Chip Selects/Latched Address bits. For PCS_n feature, these pins are active low when the micro-controller accesses the fifth or sixth region of the peripheral memory (I/O or memory space). The base address of PCS_n is programmable. These pins are asserted with the AD address bus and not floating during bus holds. For latched address bit feature, these pins output the latched addresses A2 and A1 when the EX bit in the PCS_n and MCS_n auxiliary register is cleared. A2 and A1 retain previous latched data during bus holds.
62 63 65 66	PCS3_n/RTS1_n/RTR1_n/PIO19 PCS2_n/CTS1_n/ENRX1_n/PIO18 PCS1_n/PIO17 PCS0_n/PIO16	O/I	Peripheral Chip Selects. These pins are active low when the micro-controller accesses the defined memory area of the peripheral memory block (I/O or memory addresses). For I/O accesses, the base address can be programmed in the region from 00000h to 0FFFFh. For memory address accesses, the base address can be located in the 1M-byte memory address region. These pins are asserted with the multiplexed AD address bus and not floating during bus holds.

● Interrupt Control Unit Interface

PIN No.	Symbol	Type	Description
47	NMI	I	Non-maskable Interrupt. NMI is the highest priority hardware interrupt and is non-maskable. When this pin is asserted (the NMI transition from low to high), the micro-controller always transfers the address bus to the location specified by the non-maskable interrupt vector in the micro-controller interrupt vector table. The NMI pin must be asserted for at least one CLKOUTA period to guarantee that the interrupt is recognized.
52	INT4/PIO30	I/O	Maskable Interrupt Request 4. Active high. This pin indicates that an interrupt request has occurred. The micro-controller will jump to the INT4 address vector to execute the service routine if INT4 is enabled. The interrupt input can be configured to be either edge- or level-triggered. The requesting device must hold INT4 until the request is acknowledged to guarantee interrupt recognition.
53	INT3/INTA1_n/IRQ	I/O	Maskable Interrupt Request 3/Interrupt Acknowledge 1/Slave Interrupt Request. For INT3 feature, except the differences in interrupt line and interrupt address vector, the function of INT3 is the same as that of INT4. For INTA1_n feature, in cascade mode or special fully-nested mode, this pin corresponds to INT1. For IRQ feature, when the micro-controller is as a slave device, this pin issues an interrupt request to the master interrupt controller.
54	INT2/INTA0_n/PIO31	I/O	Maskable Interrupt Request 2/Interrupt Acknowledge 0. For INT2 feature, except the differences in interrupt line and interrupt address vector, the function of INT2 is the same as that of INT4. For INTA0_n feature, in cascade mode or special fully-nested mode, this pin corresponds to INT0.
55	INT1/SELECT_n	I/O	Maskable Interrupt Request 1/Slave Select. For INT1 feature, except the differences in interrupt line and interrupt address vector, the function of INT1 is the same as that of INT4. For SELECT_n feature, when the micro-controller is as a slave device, this pin is driven from the master interrupt controller decoding. This pin is activated to indicate that an interrupt appears on the address and data bus. INT0 must be active before SELECT_n is activated when the interrupt type appears on the bus.
56	INT0	I/O	Maskable Interrupt Request 0. Except the differences in interrupt line and interrupt address vector, the function of INT0 is the same as that of INT4.

● Timer Control Unit Interface

PIN No.	Symbol	Type	Description
72 75	TMRIN1/PIO0 TMRIN0/PIO11	I/O	Timer Inputs. These pins can be used as clock or control signal inputs, depending upon the programmed timer mode. After internally synchronizing low to high transitions on TMRIN, the timer controller increments. These pins must be pulled up if not used.
73 74	TMROUT1/PIO1 TMROUT0/PIO10	O/I	Timer outputs. Depending upon timer mode selects, these pins provide single pulses or continuous waveforms. The duty cycles of the waveforms can be programmable. These pins are floating during a bus hold or reset.

● **DMA Unit Interface**

PIN No.	Symbol	Type	Description
76 77	DRQ1/INT6/PIO13 DRQ0/INT5/PIO12	I/O	DMA Request. These pins are asserted high by an external device when the device is ready for DMA channel 1 or channel 0 to perform a transfer. These pins are level-triggered and internally synchronized. The DRQ signals are not latched and must remain active until finish is serviced. For INT6/INT5: When the DMA function is not used, INT6 and INT5 can be used as additional external interrupt requests. They share the corresponding interrupt types and register control bits. INT6/5 are level-triggered only and not necessary to be held until the interrupt is acknowledged. (Interrupt requests are kept on such high levels.)

Notes:

1. *When the PIO mode and direction registers are configured as PIO modes, the 32 MUX definition pins can be set as PIO pins. For example, DRQ1/INT6/PIO13 (pin76) can be set as PIO13.*
2. *The PIO status during power-on resets: PIO1, PIO10, PIO22 and PIO23 are inputs with pull-downs, PIO4 to PIO9 are in normal operations, and the others are inputs with pull-ups.*

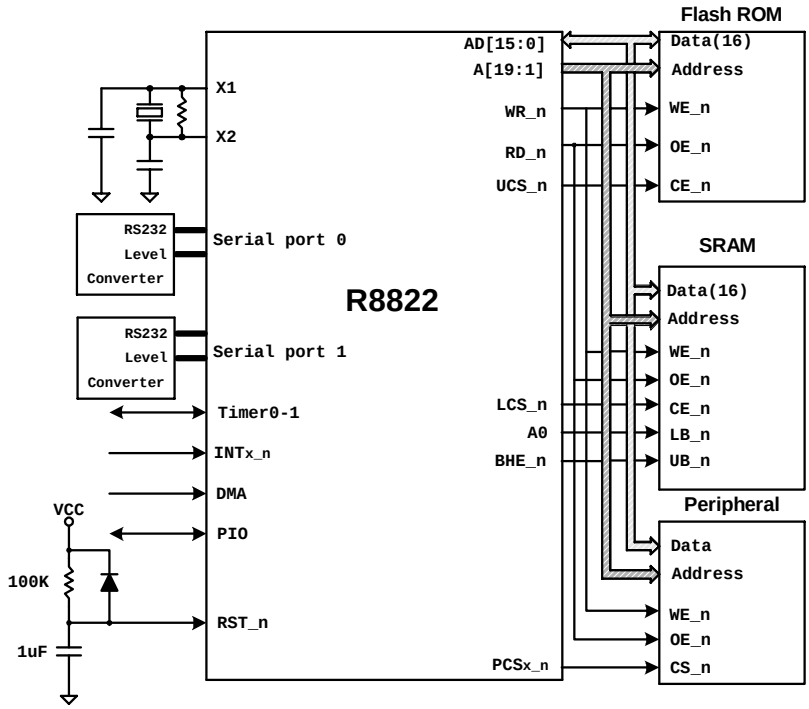
3.4 R8822 I/O Characteristics of Each Pin

PQFP Pin No.	Pin Name	Characteristics
71	RST_n	Schmitt trigger input, with a 50K internal pull-up resistor
8	ARDY	Schmitt trigger input, with a 50K internal pull-down resistor
45 47	HOLD NMI	CMOS input, with a 50K internal pull-down resistor
56 55	INT0 INT1/SELECT_n	Schmitt trigger TTL input, with a 10K internal pull-down resistor
16 17	CLKOUTA CLKOUTB	8mA 3-state CMOS output
9	S2_n/BWSEL	Bi-directional I/O, with a 50K internal pull-up resistor and 4mA TTL output
10 11	S1_n S0_n	4mA 3-state CMOS output
43 6 5	WLB_n RD_n WR_n	12mA 3-state CMOS output
19 20 22	A19/PIO9 A18/PIO8 A17/MA8/PIO7	Bi-directional I/O, with a 10K enabled/disabled internal pull-up resistor when functioning as PIO and the 10K pull-up resistor disabled for normal function; 16mA TTL output
23 24	A16 A15/MA7	16mA 3-state CMOS output

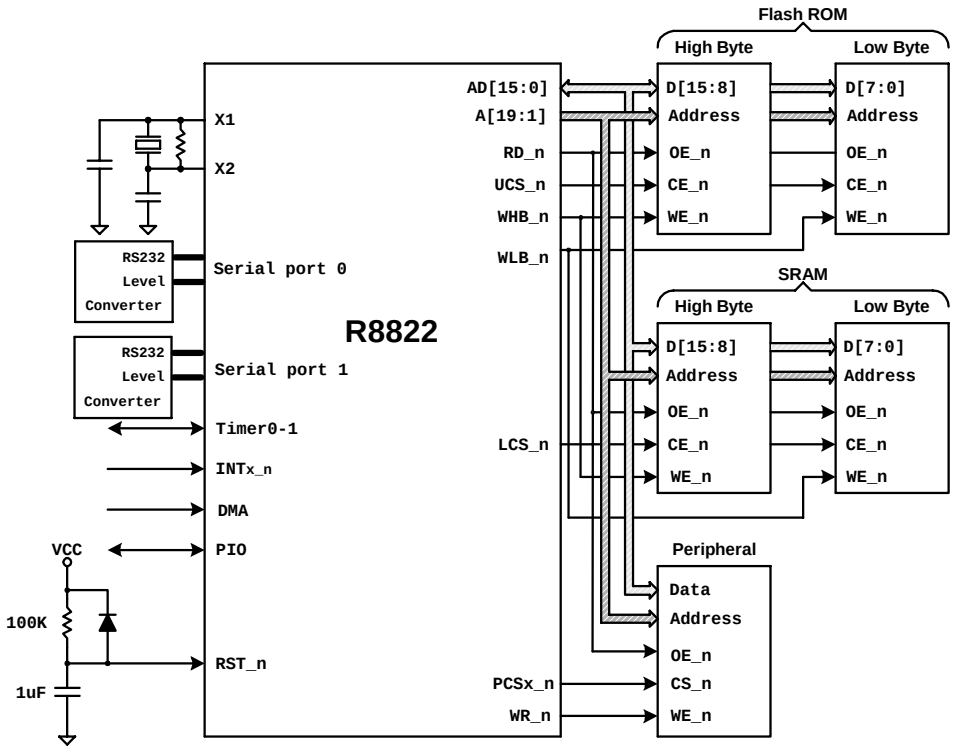
PQFP Pin No.	Pin Name	Characteristics
25 26 27 28 29 30 31 32 33 34 35 36 37 39 40	A14 A13/MA6 A12 A11/MA5 A10 A9/MA4 A8 A7/MA3 A6 A5/MA2 A4 A3/MA1 A2 A1/MA0 A0	
78 80 82 84 86 88 91 94 79 81 83 85 87 90 93 95	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15	Bi-directional I/O; 16mA TTL output
7	ALE	Bi-directional I/O, with a 50K internal pull-down resistor; 4mA TTL output
46 74 73 2 1	SRDY/PIO6 TMROUT0/PIO10 TMROUT1/PIO1 TXD0/PIO22 RXD0/PIO23	Bi-directional I/O, with a 10K enabled/disabled internal pull-down resistor when functioning as PIO and the 10k pull-down resistor disabled for normal function; 8mA TTL output.
4	BHE_n/ADEN_n	Bi-directional I/O, with a 50K internal pull-up resistor; 4mA TTL output
42	WHB_n	Bi-directional I/O, with a 50K internal pull-up resistor; 12mA TTL output
44	HLDA	4mA CMOS output
54 52	INT2/INTA0_n/PIO31 INT4/PIO30	Bi-directional I/O, with a 10K enabled/disabled internal pull-up resistor when functioning as PIO and the 10k pull-up resistor disabled for normal function; 8mA TTL output; TTL schmitt trigger input
53	INT3/INTA1_n/IRQ	Bi-directional I/O, with a 10K internal pull-up resistor; 8mA TTL output,; TTL schmitt trigger input

PQFP Pin No.	Pin Name	Characteristics
57 58	UCS_n/ONCE1_n LCS_n/ONCE0_n/RAS0_n	Bi-directional I/O, with a 10K internal pull-up resistor; 8mA TTL output; TTL schmitt trigger input
49 48 66 65 63 62 60 59 50 51 68 69 97 96 75 72 77 76 98 99 100 3	DEN_n/PIO5 DT/R_n/PIO4 PCS0_n/PIO16 PCS1_n/PIO17 PCS2_n/CTS1_n/ENRX1_n/PIO18 PCS3_n/RTS1_n/RTR1_n/PIO19 PCS5_n/A1/PIO3 PCS6_n/A2/PIO2 MCS0_n/PIO14 MCS1_n/UCAS_n/PIO15 MCS2_n/LCAS_n/PIO24 MCS3_n/RAS1_n/PIO25 UZI_n/PIO26 S6/CLKDIV2_n/PIO29 TMRIN0/PIO11 TMRIN1/PIO0 DRQ0/INT5/PIO12 DRQ1/INT6/PIO13 TXD1/PIO27 RXD1/PIO28 CTS0_n/ENRX0_n/PIO21 RTS0_n/RTR0_n/PIO20	Bi-directional I/O, with a 10K enabled/disabled internal pull-up resistor when functioning as PIO and the 10k pull-up resistor disabled for normal function; 8mA TTL output

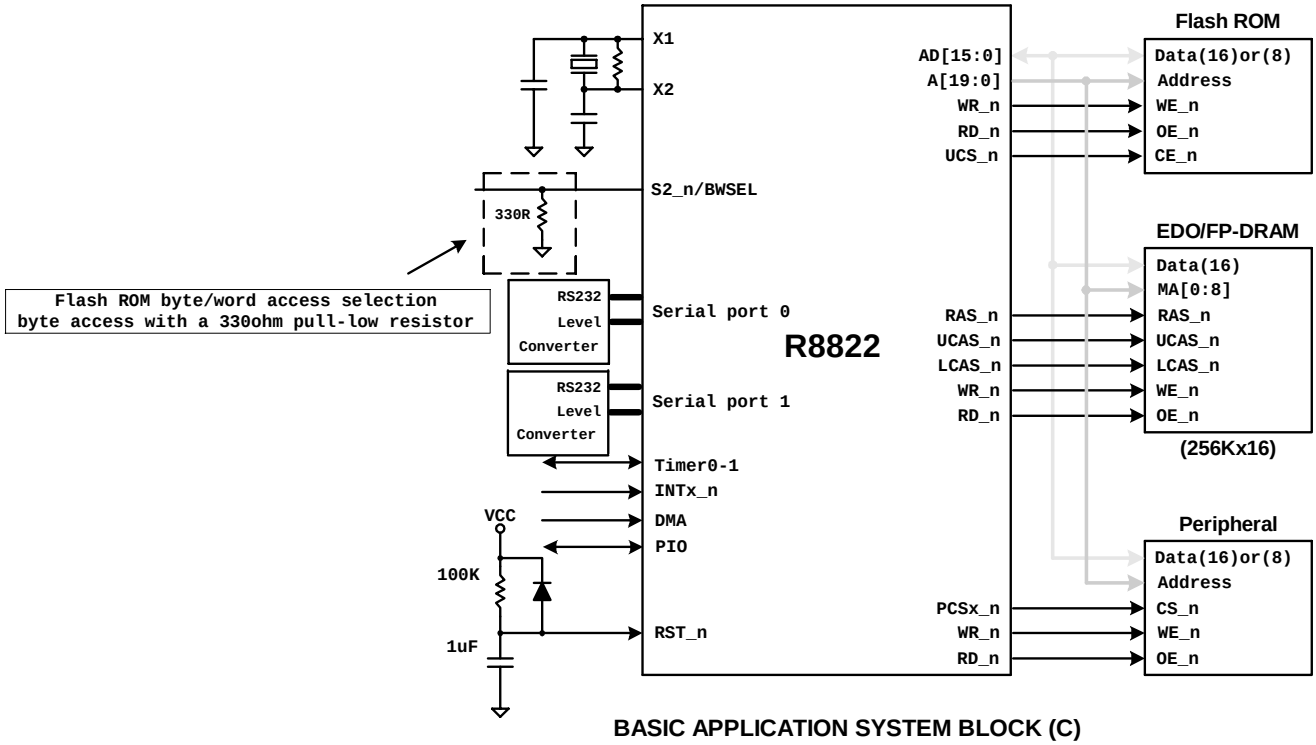
4. Basic Application System Block



BASIC APPLICATION SYSTEM BLOCK (A)

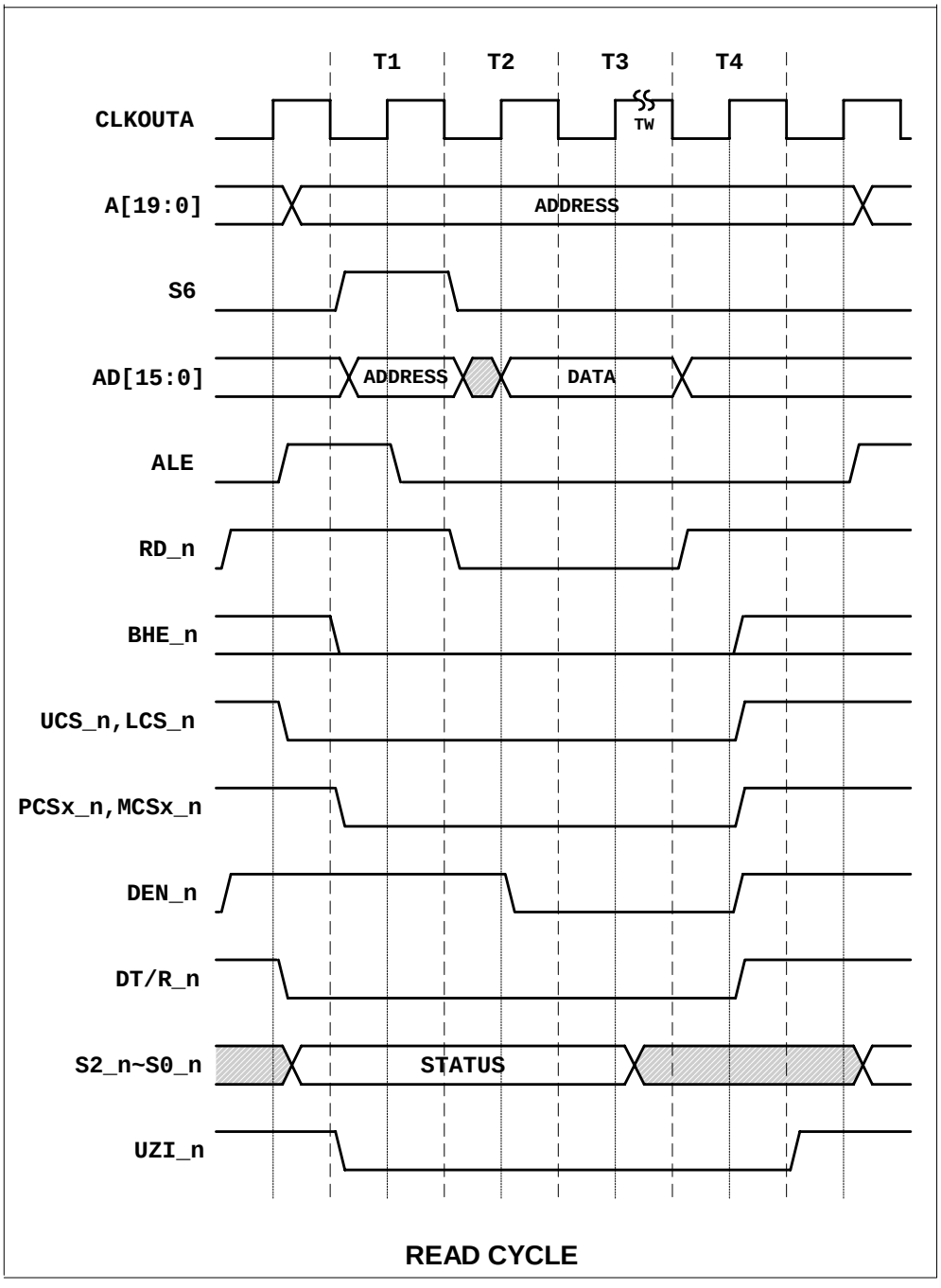


BASIC APPLICATION SYSTEM BLOCK (B)

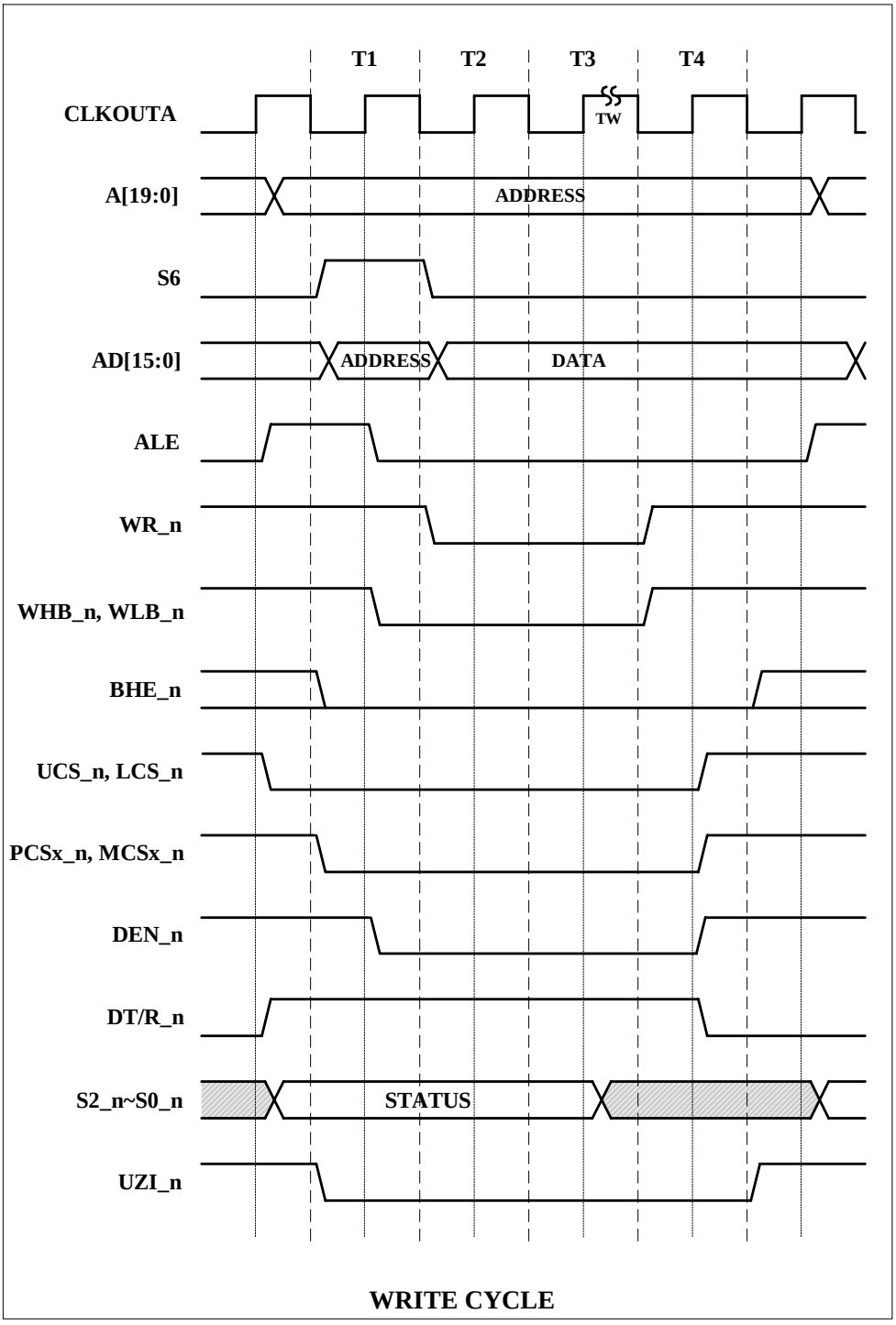


BASIC APPLICATION SYSTEM BLOCK (C)

~~4.~~5. Read/Write Timing Diagram



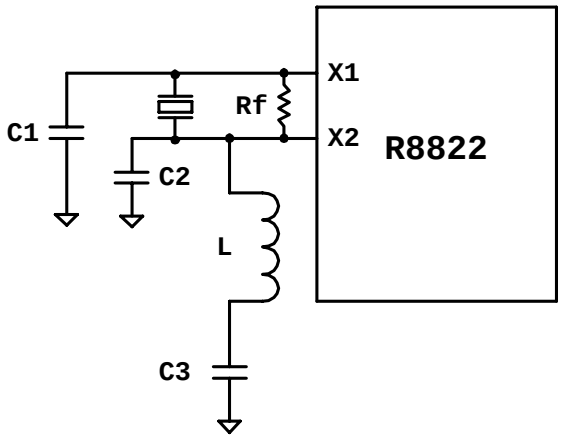
READ CYCLE


T1
T2
T3
T4
TW
CLKOUTA
A[19:0]
ADDRESS
S6
AD[15:0]
ADDRESS
DATA
ALE
WR_n
WHB_n, WLB_n
BHE_n
UCS_n, LCS_n
PCSx_n, MCSx_n
DEN_n
DT/R_n
S2_n~S0_n
STATUS
UZI_n

WRITE CYCLE

6. Crystal Characteristics

~~4.1~~6.1 Fundamental Mode



For fundamental-mode crystal:

Reference values

Frequency	10.8288MHz	19.66MHz	30MHz	33MHz	40MHz
Rf	None	None	None	None	None
C1	10Pf	10Pf	None	None	None
C2	10Pf	10Pf	10Pf	10Pf	10Pf
C3	None	None	None	None	None
L	None	None	None	None	None

For third-overtone mode crystal:

Reference values

Frequency	22.1184MHz	28.322MHz	33.177MHz	40MHz
Rf	1M	1.5M	1.5M	1.5M
C1	15Pf	15Pf	15Pf	15Pf
C2	30Pf	30Pf	30Pf	30Pf
C3	None	220Pf	220Pf	220Pf
L	None	10uL	4.7uL	2.7uL

7. Execution Unit

~~6.1~~7.1 General Registers

The R8822 has eight 16-bit general registers. The AX, BX, CX and DX can be subdivided into two 8-bit registers (AH, AL, BH, BL, CH, CL, DH and DL). The functions of these registers are described as follows:

AX: word divide, word multiply, word I/O operation

AH: byte divide, byte multiply, byte I/O, decimal arithmetic, translate operation

AL: byte divide, byte multiply operation

BX: translate operation

CX: loops, string operation

CL: variable shift and rotate operation

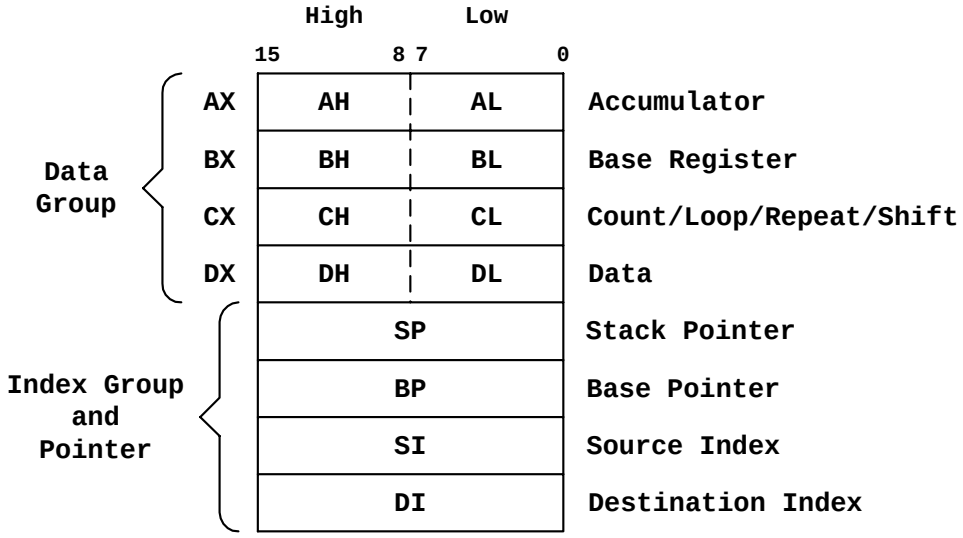
DX: word divide, word multiply, indirect I/O operation

SP: stack operations (POP, POPA, POPF, PUSH, PUSHA and PUSHF)

BP: general-purpose registers which can be used to determine offset address of operands in memory

SI: string operations

DI: string operations



GENERAL REGISTERS

~~6.2~~7.2 Segment Registers

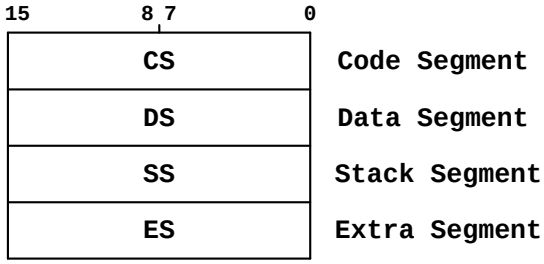
The R8822 has four 16-bit segment registers: CS, DS, SS and ES. The segment registers contain the base addresses (starting location) of these memory segments. They are immediately addressable for code (CS), data (DS & ES) and stack (SS) memory.

CS (Code Segment): The CS register points to the current code segment, which contains instructions to be fetched. The default memory space for all instructions is 64K. The initial value of CS register is 0FFFFh.

DS (Data Segment): The DS register points to the current data segment, which generally contains program variables. The DS register is initialized to 0000h.

SS (Stack Segment): The SS register points to the current stack segment, which is for all stack operations, such as pushes and pops. The stack segment is used for temporary space. The SS register is initialized to 0000h.

ES (Extra Segment): The ES register points to the current extra segment, which is typically for data storage, such as large string operations and large data structures. The ~~DS~~ ES register is initialized to 0000h.



SEGMENT REGISTERS

~~6.3~~7.3 Instruction Pointer and Status Flags Registers

IP (Instruction Pointer): The IP is a 16-bit register containing the offset of the next instruction to be fetched. This register cannot be directly accessed by software. It is updated by the bus interface unit and can be changed, saved or restored as a result of program execution. The IP register is initialized to 0000h and the starting execution address for CS:IP is at 0FFFF0h.

Register Name: Processor Status Flags Register

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				OF	DF	IF	TF	SF	ZF	Rsvd	AF	Rsvd	PF	Rsvd	CF

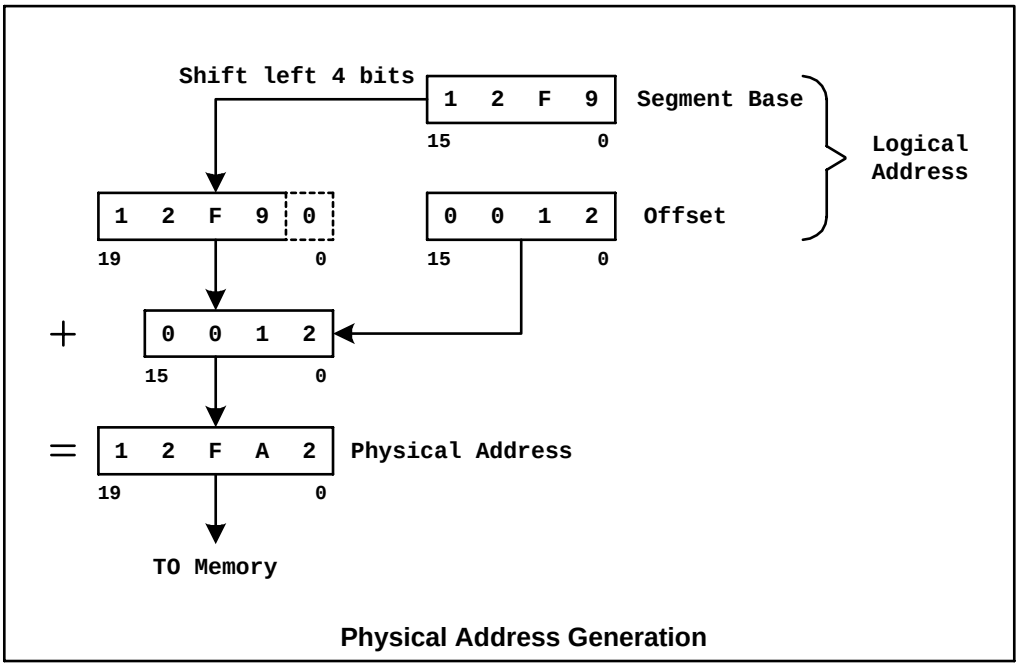
These flags reflect the status after the Execution Unit is executed.

Bit	Name	Description
15-12	Rsvd	Reserved.
11	OF	Overflow Flag. If an arithmetic overflow occurs, this flag will be set.
10	DF	Direction Flag. If this flag is set, the string instructions are in the process of incrementing addresses. If DF is cleared, the string instructions are in the process of decrementing addresses. Refer to the STD and CLD instructions for setting and clearing the DF flag.
9	IF	Interrupt-Enable Flag. Refer to the STI and CLI instructions for setting and clearing the IF flag. Set 1: The CPU enables the maskable interrupt requests. Set 0: The CPU disables the maskable interrupt requests.
8	TF	Trace Flag. Set to enable single-step mode for debugging; cleared to disable the single-step mode. If an application program sets the TF flag with a POPF or IRET instruction, a debug exception is generated after the instruction (The CPU automatically generates an interrupt after each instruction) that follows the POPF or IRET instruction.
7	SF	Sign Flag. If this flag is set, the high-order bit of the result of an operation will be 1, indicating the state of being negative.
6	ZF	Zero Flag. If this flag is set, the result of the operation will be zero.
5	Rsvd	Reserved
4	AF	Auxiliary Flag. If this flag is set, there will be a carry from the low nibble to the high one or a borrow from the high nibble to the low one of the AL general-purpose register. It is used in BCD operation.
3	Rsvd	Reserved
2	PF	Parity Flag. If this flag is set, the result of the low-order 8-bit operation will have even parities.
1	Rsvd	Reserved
0	CF	Carry Flag. If CF is set, there will be a carry out or a borrow into the high-order bit of the instruction result.

~~6.4~~7.4 Address Generation

~~6.5~~

The Execution Unit generates a 20-bit physical address to the Bus Interface Unit by Address Generation. Memory is organized in sets of segments. Each segment contains a 16-bit value. Memory is addressed with a two-component address that consists of a 16-bit segment and 16-bit offset. The Physical Address Generation figure describes how the logical address is transferred to the physical address.



Physical Address Generation

~~7.~~8. Peripheral Register List

The peripheral control block can be mapped into either memory or I/O space by programming the FEh register. It starts at FF00h in I/O space when the microprocessor is reset. The definitions of all the peripheral control block registers are listed in the following table and the complete descriptions arranged in the related block units.

Offset (HEX)	Register Name	Page	Offset (HEX)	Register Name	Page
FE	Peripheral Control Block Relocation Register	29	66	Timer 2 Mode/Control Register	81
FA	Disable Peripheral Clock Register	32	62	Timer 2 Maxcount Compare A Register	82
F6	Reset Configuration Register	34	60	Timer 2 Count Register	82
F4	Processor Release Level Register	29	5E	Timer 1 Mode/Control Register	80
F2	Auxiliary Configuration Register	39	5C	Timer 1 Maxcount Compare B Register	81
F0	Power-Save Control Register	31	5A	Timer 1 Maxcount Compare A Register	80
E6	Watchdog Timer Control Register	83	58	Timer 1 Count Register	80
E4	Refresh Counter Register	99	56	Timer 0 Mode/Control Register	77
E2	Refresh Reload Value Counter Register	98	54	Timer 0 Maxcount Compare B Register	79
DA	DMA 1 Control Register	72	52	Timer 0 Maxcount Compare A Register	79
D8	DMA 1 Transfer Count Register	73	50	Timer 0 Count Register	79
D6	DMA 1 Destination Address High Register	73	46	Power-Down Configuration Register	32
D4	DMA 1 Destination Address Low Register	73	44	Serial Port 0 Interrupt Control Register	51
D2	DMA 1 Source Address High Register	74	42	Serial Port 1 Interrupt Control Register	51
D0	DMA 1 Source Address Low Register	74	40	INT4 Control Register	52
CA	DMA 0 Control Register	69	3E	INT3 Control Register	53
C8	DMA 0 Transfer Count Register	71	3C	INT2 Control Register	53
C6	DMA 0 Destination Address High Register	71	3A	INT1 Control Register	54
C4	DMA 0 Destination Address Low Register	71	38	INT0 Control Register	55
C2	DMA 0 Source Address High Register	72	36	DMA1/INT6 Interrupt Control Register	56
C0	DMA 0 Source Address Low Register	72	34	DMA0/INT5 Interrupt Control Register	57
A8	PCS_n and MCS_n Auxiliary Register	44	32	Timer Interrupt Control Register	58
A6	Midrange Memory Chip Select Register	43	30	Interrupt Status Register	59
A4	Peripheral Chip Select Register	45	2E	Interrupt Request Register	60
A2	Low Memory Chip Select Register	41	2C	Interrupt In-Service Register	61
A0	Upper Memory Chip Select Register	40	2A	Interrupt Priority Mask Register	63
88	Serial Port 0 Baud Rate Divisor Register	90	28	Interrupt Mask Register	64
86	Serial Port 0 Receive Register	90	26	Interrupt Poll Status Register	65
84	Serial Port 0 Transmit Register	90	24	Interrupt Poll Register	65
82	Serial Port 0 Status Register	89	22	End-of-Interrupt Register	66
80	Serial Port 0 Control Register	88	20	Interrupt Vector Register	67
7A	PIO Data 1 Register	94	18	Serial Port 1 Baud Rate Divisor Register	92
78	PIO Direction 1 Register	94	16	Serial Port 1 Receive Register	91
76	PIO Mode 1 Register	95	14	Serial Port 1 Transmit Register	91
74	PIO Data 0 Register	95	12	Serial Port 1 Status Register	91
72	PIO Direction 0 Register	95	10	Serial Port 1 Control Register	91
70	PIO Mode 0 Register	96			

Register Offset: FEh

Register Name: Peripheral Control Block Relocation Register

Reset Value : ~~0000~~20FFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	S/M_n	Rsvd	M/IO_n	R [19:8]											

The Peripheral Control Block (PCB) is mapped into either memory or I/O space by programming this register. When the other chip selects (PCSx_n or MCSx_n) are programmed to zero wait state and the external ready is ignored, PCSx_n or MCSx_n can overlap the control block.

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14	S/M_n	R/W	Slave/Master – configures the interrupt controller. Set 0: Master mode. Set 1: Slave mode.
13	Rsvd	RO	Reserved.
12	M/IO_n	R/W	Memory/IO space. At reset, this bit is set to 0 and the PCB map starts at FF00h in I/O space. Set 1: The peripheral control block (PCB) is located in memory space. Set 0: The PCB is located in I/O space (default).
11-0	R[19:8]	R/W	Relocation Address bits. The upper address bits of the PCB base address. The lower eight bits default to 00h. When the PCB is mapped into I/O space, R[19:16] must be programmed to 0000b.

Register Offset: F4h

Register Name: Processor Release Level Register

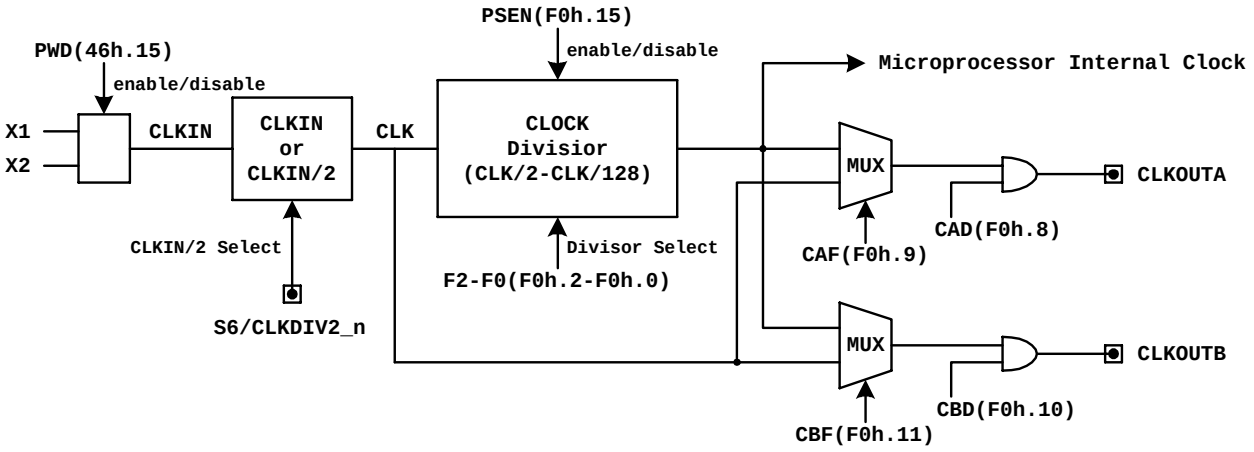
Reset Value : --~~00~~D9~~0~~h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRL								1	~~0~~1	0	1	1	0	0	1

This read-only register specifies the processor release version and RDC identification number.

Bit	Name	Attribute	Description
15-13	PRL	RO	Read only:011
12-8			Processor Version. 01h: Version A. 02h: Version B 03h: Version C 04h: Version D
7-0	ID	RO	RDC identification number is --D9.

9. Power-Save & Power-Down



System Clock

The CPU provides power-save & power-down functions.

* **Power-Save:**

In power-save mode, users can program the Power-Save Control Register to divide the internal operating clock. Users can also disable each non-used peripheral clock by programming the Disable Peripheral Clock Register.

* **Power-Down:**

The CPU can enter power-down mode (stop clock) when the Power-Down Configuration Register is programmed and the CPU runs in full-speed or power-save mode. The CPU will be waked up when each one of the external INT0, INT1, INT2, INT3 and INT4 pins is active high, and the CPU operating clock will go back to full-speed mode if the INT function is serviced (the interrupt flag is enabled). If the interrupt flag is disabled, the CPU will be waked up by INT, the operating clock will go back to the previous operating clock state, and the CPU will execute the next program counter instruction. It will wait 19-bit counter time for the crystal clock to be stable when the CPU wakes up from the stop clock mode.

Register Offset: F0h
Register Name: Power-Save Control Register
Reset Value : 0000~~000~~h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSEN	MCSBIT	0	0	CBF	CBD	CAF	CAD	0	0	0	0	0	F2	F1	F0

Bit	Name	Attribute	Description
15	PSEN	R/W	Enable Power-Save Mode. This bit is cleared by hardware when an external interrupt occurs. This bit will not change when software interrupts (INT instructions) and exceptions occur. Set 1: Enable power-save mode and divide the internal operating clock by values in F[2:0].
14	MCSBIT	R/W	MCS0_n Control bit. Set 0: MCS0_n operates normally. Set 1: MCS0_n is active over the entire MCSx_n range
13-12	Rsvd	RO	Reserved.
11	CBF	R/W	CLKOUTB Output Frequency selection. Set 1: The CLKOUTB output frequency is the same as the crystal input frequency. Set 0: The CLKOUTB output frequency, which is the same as the internal clock frequency of the microprocessor, is generated from the clock divisor.
10	CBD	R/W	CLKOUTB Drive Disable Set 1: Disable CLKOUTB. This pin will be three-stated. Set 0: Enable CLKOUTB.
9	CAF	R/W	CLKOUTA Output Frequency selection. Set 1: The CLKOUTA output frequency is the same as the crystal input frequency. Set 0: The CLKOUTA output frequency, which is the same as the internal clock frequency of the microprocessor, is generated from the clock divisor.
8	CAD	R/W	CLKOUTA Drive Disable. Set 1: Disable CLKOUTA. This pin will be three-stated. Set 0: Enable CLKOUTA.
7-3	Rsvd	RO	Reserved.
2-0	F[2:0]	R/W	Clock Divisor Select. **F2, F1, F0 ----- Divider Factor** 0, 0, 0 ---- Divide by 1 0, 0, 1 ---- Divide by 2 0, 1, 0 ---- Divide by 4 0, 1, 1 ---- Divide by 8 1, 0, 0 ---- Divide by 16 1, 0, 1 ---- Divide by 32 1, 1, 0 ---- Divide by 64 1, 1, 1 ---- Divide by 128

Register Offset: FAh
Register Name: Disable Peripheral Clock Register
Reset Value : 0000~~000~~h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntClk	UART Clk	DMA Clk	Timer Clk	Reserved											

Bit	Name	Attribute	Description
15	IntClk	R/W	Set 1 to stop the Interrupt controller clock.
14	UARTClk	R/W	Set 1 to stop the asynchronous serial port controller clock.
13	DMAClk	R/W	Set 1 to stop the DMA controller clock.
12	TimerClk	R/W	Set 1 to stop the timer controller clock.
11-0	Rsvd	RO	Reserved.

Register Offset: 46h
Register Name: Power-Down Configuration Register
Reset Value : 00~~000~~h

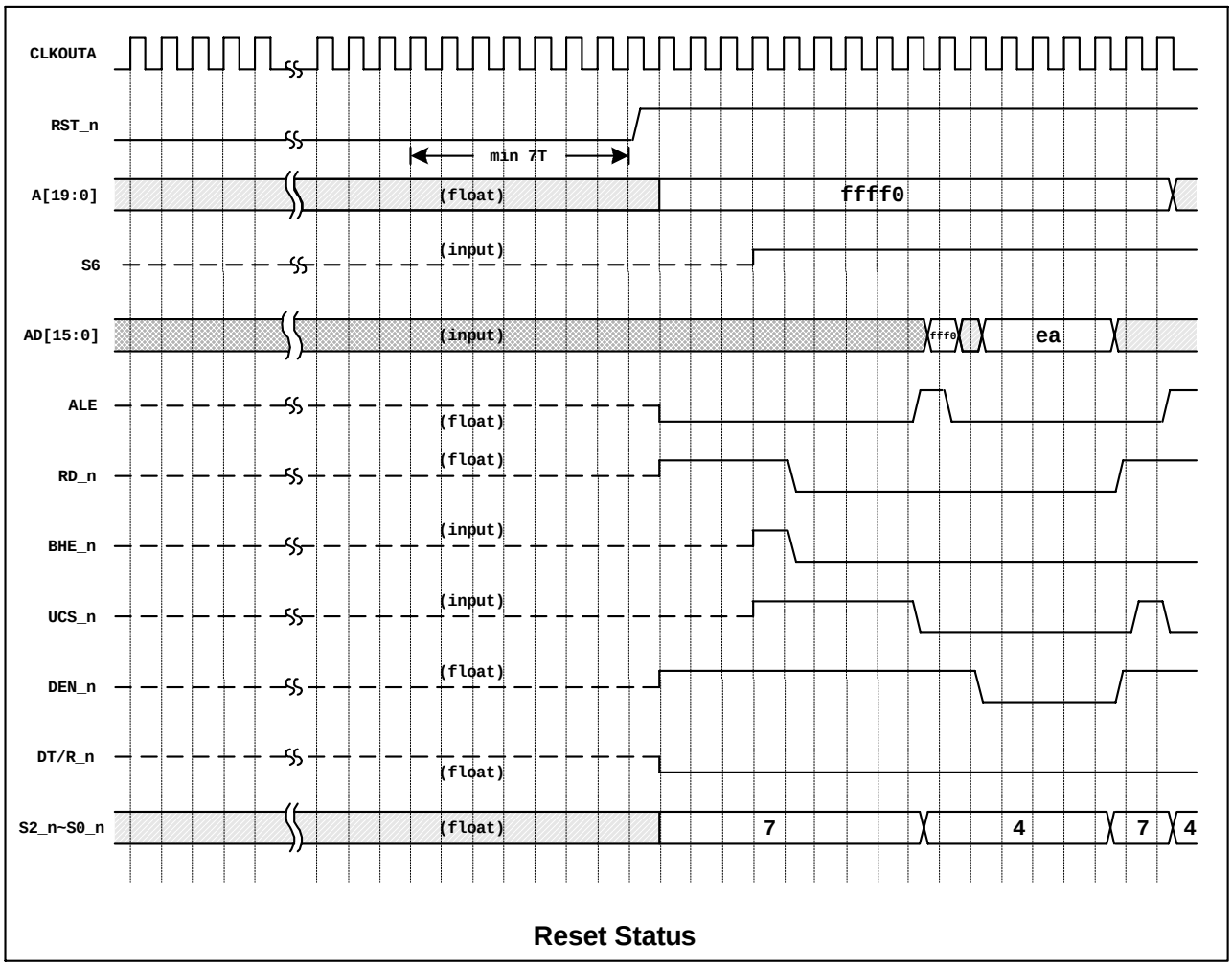
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWD	0	0	0	0	0	0	WIF	0	0	0	I4	I3	I2	I1	I0

Bit	Name	Attribute	Description
15	PWD	R/W	Power-Down Enable. When this bit is set to 1, the CPU will enter power-down mode, then the crystal clock will stop. The CPU will be waked up when an external INT (INT4 – INT0]) is active high. It will wait 19-bit counter time for the crystal clock to be stable before the CPU is waked up.
14-9	Rsvd	RO	Reserved.
8	WIF	R/W	Wake-up Interrupt Flag. Read-only bit. When the CPU is waked up by interrupts from power-down mode, this bit will be set to 1 by hardware. Otherwise this bit is 0.
7-5	Rsvd	RO	Reserved.
4-0	I[4:0]	R/W	Enable the external interrupt (INT4 – INT0) wake-up function. Set these bits to 1 to make the INT pins function as power-down wake-up pins.

10. Reset

Processor initialization is accomplished with activation of the RST_n pin. To reset the processor, this pin should be held low for at least seven oscillator periods. The Reset Status Figure shows the status of the RST_n pin and the other related pins.

When RST_n goes from low to high, the state of input pins (with weak pull-up or pull-down resistors) will be latched, and each pin will perform its individual function. AD [15:0] will be latched into Register F6h. UCS_n/ONCE1_n and LCS_n/ONCE0_n/RAS0_n will enter ONCE mode (all of the pins will be floating except X1 and X2) when they are with pull-low resistors. The input clock will be divided by 2 when S6/CLKDIV2_n is with a pull-low resistor. The AD[15:0] bus will drive both of the address and data regardless of the DA bit setting during UCS_n and LCS_n cycles if BHE_n/ADEN_n is with a pull-low resistor



Reset Status

Register Offset: F6h

Register Name: Reset Configuration Register

Reset Value : AD [15:0]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RC															

Bit	Name	Attribute	Description
15-0	RC	RO	Reset Configuration AD[15:0]. AD [15:0] must be with weak pull-up or pull-down resistors to correspond to the contents when they are latched into this register as the RST_n signal goes from low to high. The value of the Reset Configuration Register provides system information when this register is read by software. This register is read only and the contents remain valid until next processor is reset.

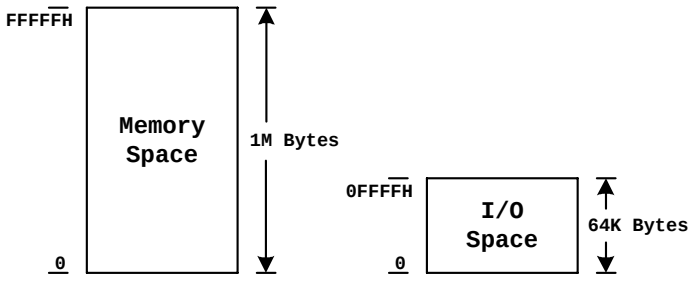
~~10.~~11. Bus Interface Unit

The bus interface unit drives address, data, status and control information to define a bus cycle. A[19:0] form a non-multiplexed memory or I/O address bus and AD[15:0] form a multiplexed address and data bus for memory or I/O accesses. S2_n – S0_n are encoded to indicate the bus status, which is described in Chapter 3.3 (Functional Description). The Basic Application System Block (Chapter 4) and Read/Write Timing Diagram (Chapter 5) describe the basic bus operations.

When the DRAM controller is enabled and the microcontroller accesses the DRAM, AD[15:0] will perform the DRAM data bus. MA[8:0] form a bus which is multiplexed with Address bus.

~~10.2~~11.1 Memory and I/O Interface

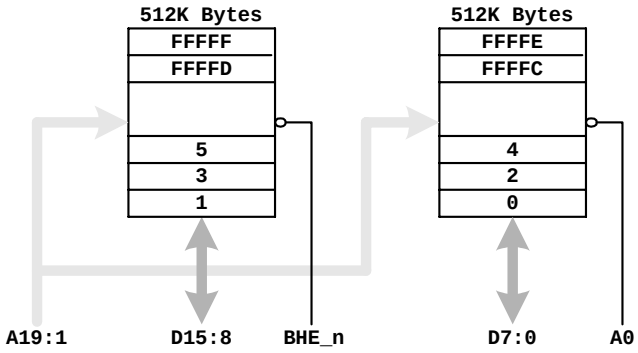
The memory space consists of 1M bytes (512K 16-bit port) and the I/O space consists of 64K bytes (32K 16-bit port). Memory devices exchange information with the CPU during memory read, memory write and instruction fetch bus cycles. I/O read and I/O write bus cycles use a separate I/O address space. Only IN/OUT instructions can access I/O address space, and information must be transferred between the peripheral devices and the AX register. The first 256 bytes of I/O space can be accessed directly by the I/O instructions. The entire 64K-byte I/O address space can be accessed indirectly through the DX register. The I/O instructions always force address A[19:16] to low level.



Memory and I/O Space

~~10.3~~11.2 Data Bus

The data bus for memory address space is physically implemented by dividing the address space into two banks of up to 512K bytes. One bank connects to the lower half of the data bus and contains the even-addressed bytes (A0=0); the other bank connects to the upper half of the data bus and contains odd-addressed bytes (A0=1). A0 and BHE_n determine either one bank or both banks participate in data transfers.

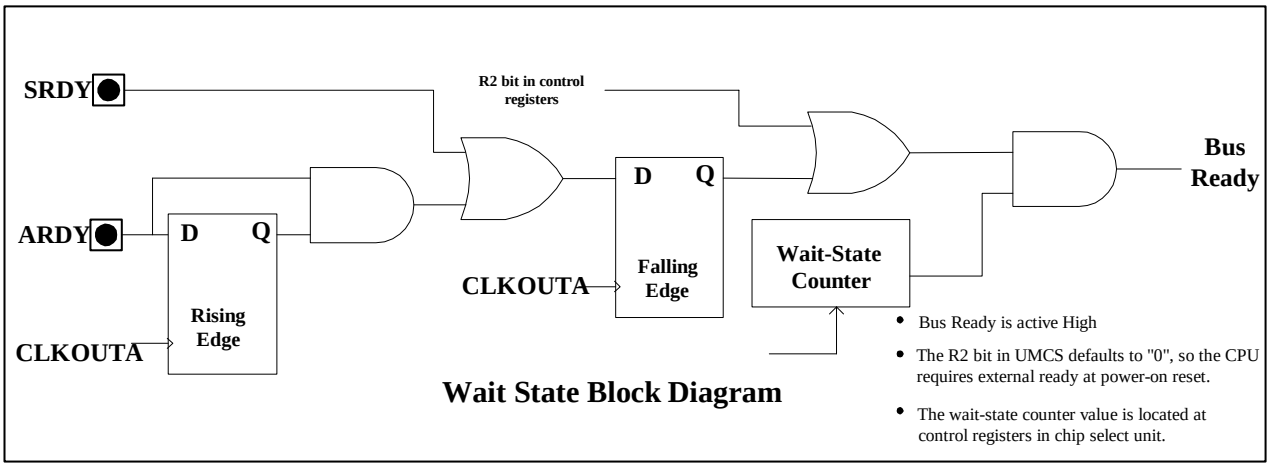


Physical Data Bus Models

~~10.4~~11.3 Wait States

Wait states extend the data phase of the bus cycle. As long as the ARDY or SRDY input remains with low level, wait states will be inserted in. If R2 bit=0, wait states can also be inserted in by programming the internal chip select registers. The R2 bit of UMCS (offset A0h) defaults to be low, so either ARDY or SRDY should be in ready state (with a pull-high resistor) when at power-on resets or external resets.

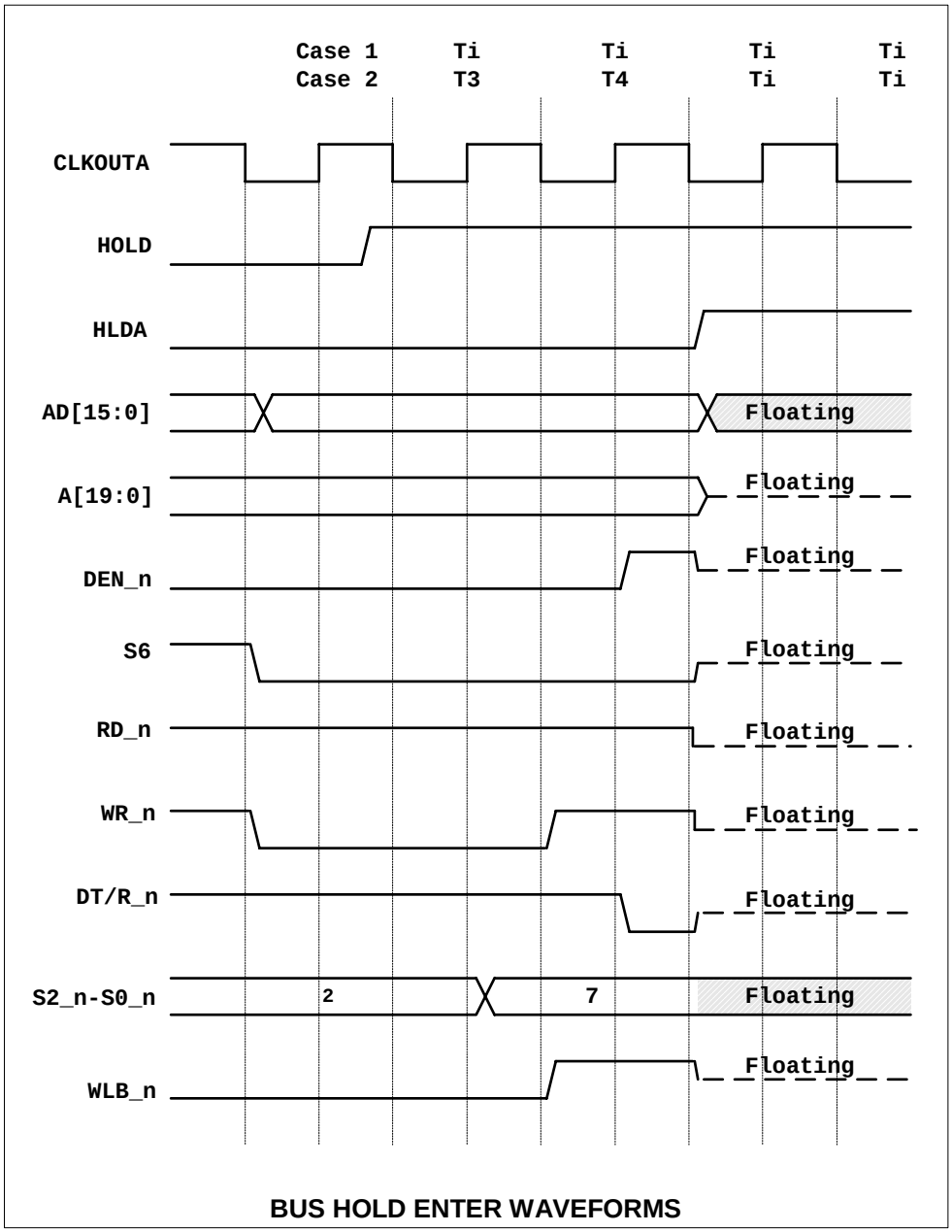
The wait-state counter value is decided by the R3, R1 and R0 bits in each chip select register. There are five groups of the R3, R1 and R0 bits in Register offset A0h, A2h, A4h, A6h and A8h, and each group is independent.



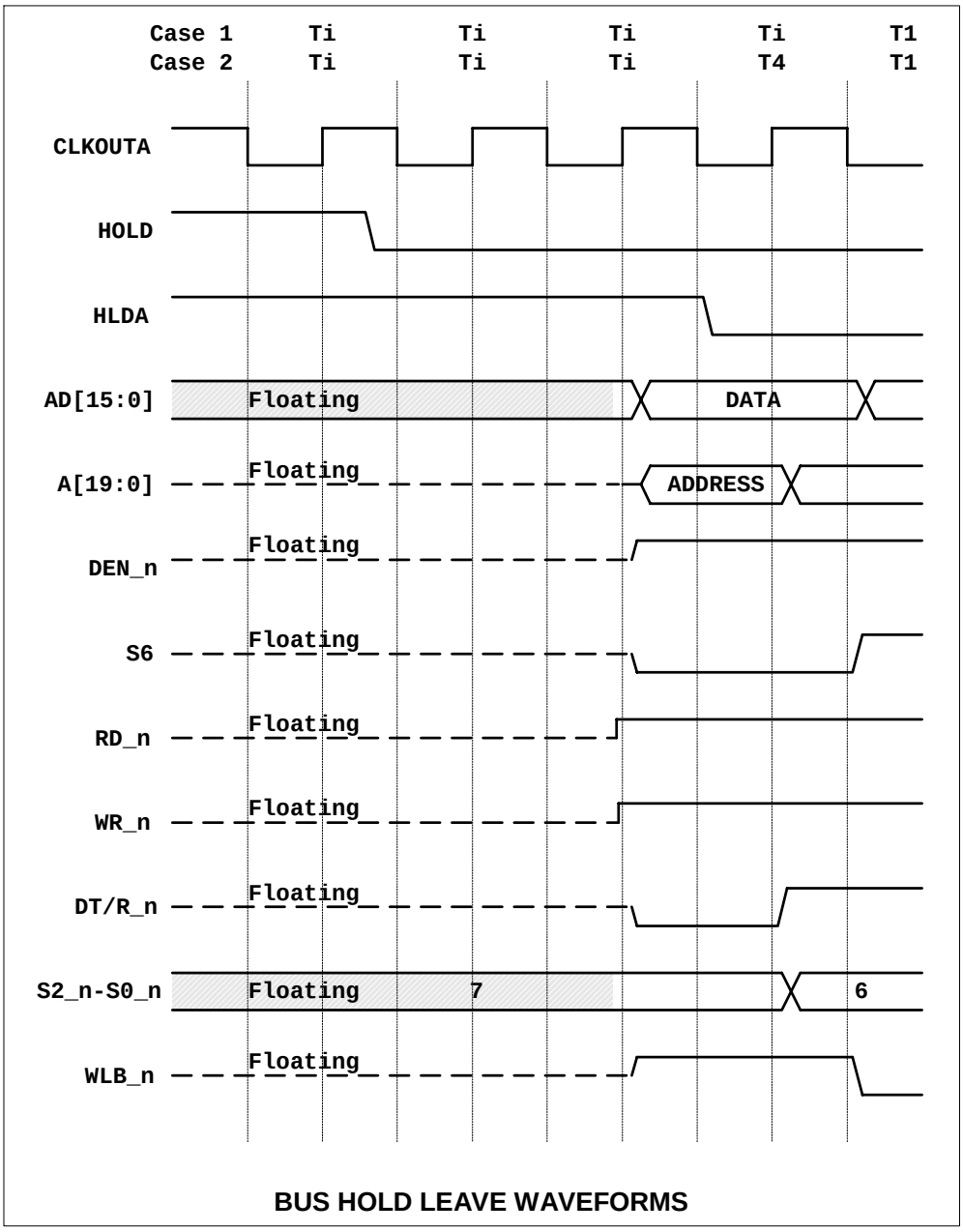
Wait State Block Diagram

~~10.6~~11.4 Bus Hold

When another bus master requests a bus hold condition (HOLD is active high), the microprocessor will issue an HLDA in response to a HOLD request at the end of T4 or Ti. When the microprocessor is in hold status (HLDA is high), AD[15:0], A[19:0], WR_n, RD_n, DEN_n, S2_n–S0_n, S6, BHE_n, DT/R_n, WHB_n and WLB_n are floating, and UCS_n, LCS_n, PCS6_n–PCS5_n, MCS3_n–MCS0_n and PCS3_n–PCS0_n will be driven high. After HOLD is detected as being low, the microprocessor will lower HLDA.



BUS HOLD ENTER WAVEFORMS



BUS HOLD LEAVE WAVEFORMS

11.5 Bus Width

The R8822 defaults to 16-bit bus access and the bus can be programmed as 8-bit or 16-bit access when memory or I/O access is located in the LCS_n, MCSx_n or PCSx_n address space. The UCS_n code fetch selection can be 8-bit or 16-bit bus width, which is decided by the S2_n/BWSEL pin input status as the RST_n pin goes from low to high. When the S2_n/BWSEL pin is with a pull-low resistor, the code fetch selection is 8-bit bus width. The DRAM bus width is 16 bits, which cannot be changed.

Register Offset: F2h
Register Name: Auxiliary Configuration Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								USIZ	ENRX1	RTS1	ENRX0	RTS0	LSIZ	MSIZ	IOSIZ

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	USIZ	R/W	Boot Code Bus Width. This bit reflects the S2_n/BWSEL pin input status when the RST_n pin goes from low to high. Set 0: 16-bit bus width booting when the S2_n/BWSEL pin is without a pull-low resistor. Set 1: 8-bit bus width booting when the S2_n/BWSEL pin is with a 330 ohm pull-low resistor.
6	ENRX1	R/W	Enable the Receiver Request of Serial Port 1. Set 1: The CTS1_n/ENRX1_n pin is configured as ENRX1_n. Set 0: The CTS1_n/ENRX1_n pin is configured as CTS1_n.
5	RTS1	R/W	Enable Request to Send of Serial Port 1. Set 1: The RTR1_n/RTS1_n pin is configured as RTS1_n. Set 0: The RTR1_n/RTS1_n pin is configured as RTR1_n.
4	ENRX0	R/W	Enable the Receiver Request of Serial Port 0. Set 1: The CTS0_n/ENRX0_n pin is configured as ENRX0_n. Set 0: The CTS0_n/ENRX0_n pin is configured as CTS0_n.
3	RTS0	R/W	Enable Request to Send of Serial port 0. Set 1: The RTR0_n/RTS0_n pin is configured as RTS0_n. Set 0: The RTR0_n/RTS0_n pin is configured as RTR0_n.
2	LSIZ	R/W	LCS_n Data Bus Size selection. This bit cannot be changed while executing from the LCS_n space or while the Peripheral Control Block is overlaid with the PCS_n space. Set 1: 8-bit data bus access when the memory access is located in the LCS_n memory space. Set 0: 16-bit data bus access when the memory access is located in the LCS_n memory space.
1	MSIZ	R/W	MCSx_n and PCSx_n Memory Space Data Bus Size selection. This bit cannot be changed while executing from the associated address space or while the Peripheral Control Block is overlaid on this address space. Set 1: 8-bit data bus access when the memory access is located in the selected memory space. Set 0: 16-bit data bus access when the memory access is located in the selected memory space.
0	IOSIZ	R/W	I/O Space Data Bus Size selection. This bit determines the width of the data bus for all I/O space accesses. Set 1: 8-bit data bus access. Set 0: 16-bit data bus access.

~~11.~~12. Chip Select Unit

The Chip Select Unit provides 12 programmable chip select pins to access a specific memory or peripheral device. The chip selects are programmed through five peripheral control registers (A0h, A2h, A4h, A6h and A8h) and all the chip selects can be inserted wait states in by programming the peripheral control registers.

~~11.1~~12.1 UCS_n

UCS_n defaults to active on reset for code accesses with a default memory range of 64K bytes (F0000h – FFFFFh) and three wait states automatically inserted. However, the base address and size of the upper memory block are programmable up to 512K bytes (80000h – FFFFFh). If no wait states are inserted, UCS_n will be driven low within four CLKOUTA oscillators~~CLKOUTA~~ when active.~~three~~

Register Offset: A0h
Register Name: Upper Memory Chip Select Register
Reset Value : F03Bh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	LB [2:0]			0	0	0	0	DA	UDEN	1	1	1	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-12	LB[2:0]	R/W	**LB[2:0]**, Memory block size selection for the UCS_n chip select pin. The region in which the UCS_n chip select pin is active can be configured by LB[2:0]. The default memory block size is from F0000h to FFFFFh. **LB2, LB1, LB0** ---- **Memory Block size** , **Start address**, **End Address** 1 , 1 , 1 ---- 64K , F0000h , FFFFFh 1 , 1 , 0 ---- 128K , E0000h , FFFFFh 1 , 0 , 0 ---- 256K , C0000h , FFFFFh 0 , 0 , 0 ---- 512K , 80000h , FFFFFh
11-8	Rsvd	RO	Reserved
7	DA	R/W	Disable Address. If the BHE_n/ADEN_n pin is held high on the rising edge of RST_n, the DA bit will be valid to enable/disable the address phase of the AD bus. If the BHE_n/ADEN_n pin is held low on the rising edge of RST_n, the AD bus will always drive both the address and data, regardless of the DA bit setting. Set 1: Disable the address phase of the AD[15:0] bus cycle when UCS_n is asserted. Set 0: Enable the address phase of the AD[15:0] bus cycle when UCS_n is asserted.
6	UDEN	R/W	Upper DRAM Enable. Set this bit to enable the bank2 (80000h – FFFFFh) DRAM controller. When the UDEN bit is set, the MCS3_n pin becomes RAS1_n, and the MCS1_n and MCS2_n pins become UCAS_n and LCAS_n respectively. The UCS_n

			pin is disabled when the UDEN bit is set to 1. Users can boot the code from flash memory with the UCS_n pin and switch space to DRAM bank 1 after system initialization.
5-3	Rsvd	RO	Reserved
2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for the UCS_n chip select. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**R1-R0**, Wait-State value. When R2 is set to 0, wait states can be inserted into an access to the UCS_n memory area. The reset value of (R1,R0) is (1,1). **R1, R0 -- Wait States** 0, 0 -- 0 0, 1 -- 1 1, 0 -- 2 1, 1 -- 3

~~11.2~~12.2 LCS_n

LCS_n means lower memory chip selects. The base address and size of the lower memory block (which have no default size on reset) are programmable up to 512K bytes (00000h-7FFFFh). Register A2h must be programmed first before the target memory range is accessed. The LCS_n pin is not active on reset, but any read or write access to the A2h register activates this pin.

Register Offset: A2h
Register Name: Low Memory Chip Select Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	UB [2:0]			1	1	1	1	DA	LDEN	1	1	1	R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-12	UB[2:0]	R/W	**UB[2:0]**, Memory block size selection for the LCS_n chip select pin. The region in which the LCS_n chip select pin is active can be configured by UB[2:0]. The LCS_n pin is not active on reset, but any read or write access to the A2h (LMCS) register activates this pin. **UB2, UB1, UB0 ---- Memory Block size , Start address, End Address** 0 , 0 , 0 ---- 64K , 00000h , 0FFFFh 0 , 0 , 1 ---- 128K , 00000h , 1FFFFh 0 , 1 , 1 ---- 256K , 00000h , 3FFFFh 1 , 1 , 1 ---- 512K , 00000h , 7FFFFh
11-8	Rsvd	RO	Reserved
7	DA	R/W	Disable Address. If the BHE_n/ADEN_n pin is held high on the rising edge of

			RST_n, the DA bit will be valid to enable/disable the address phase of the AD bus. If the BHE_n/ADEN_n pin is held low on the rising edge of RST_n, the AD bus will always drive the address and data. Set 1: Disable the address phase of the AD[15:0] bus cycle when LCS_n is asserted. Set 0: Enable the address phase of the AD[15:0] bus cycle when LCS_n is asserted.
6	LDEN	R/W	Lower DRAM Enable. This bit is used to enable the bank 0 (00000h-7FFFFh) DRAM controller. Set LDEN to 1, the LCS_n pin becomes RAS0_n and the MCS1_n and MCS2_n pins become UCAS_n and LCAS_n respectively.
5-3	Rsvd	RO	Reserved
2	R2	R/W	Ready Mode. This bit is used to configure the ready mode for the LCS_n chip select. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	Wait-state value. When R2 is set to 0, wait states can be inserted into an access to the LCS_n memory area. **R1, R0 -- Wait States** 0, 0 -- 0 0, 1 -- 1 1, 0 -- 2 1, 1 -- 3

12.3 MCSx_n

The memory block of MCS3_n – MCS0_n can be located anywhere within the 1M-byte memory space, exclusive of the areas associated with the UCS_n and LCS_n chip selects. The base address and size of the midrange memory block are programmable up to 512K bytes. The 512K MCSx_n block size can only be used when located at address 00000h, and the LCS_n chip selects must not be active in this case. Locating the 512K MCSx_n block size at 80000h is not allowed because it always in conflict with the range of UCS_n or RAS1_n. The MCS_n chip selects are programmed through two registers A6h and A8h, but these select pins are not active on resets. Both of the A6h and A8h registers must be accessed with a read or write to activate MCS3_n–MCS0_n. There is no default value in the A6h and A8h registers, so the A6h and A8h must be programmed first before MCS3_n–MCS0_n are activated. When the DRAM controller is enabled, MCS3_n–MCS1_n are performed as DRAM interface. (Refer to the DRAM Controller unit.)

Register Offset: A6h
Register Name: Midrange Memory Chip Select Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA[19:13]							1	1	1	1	1	1	R2	R1	R0

Bit	Name	Attribute	Description
15-9	BA[19:13]	R/W	Base Address. BA[19:13] correspond to bit[19:13] of the 1M-byte (20-bit) programmable base address of the MCS_n chip select block. Bits 12 to 0 of the base address are always 0. The base address can be set to any integer multiple of the size of the memory block size selected in these bits. For example, if the midrange block is 32K bytes, only bits BA[19:15] can be programmed. Therefore, the block address could be located at 20000h or 38000h but not 22000h. The base address of the MCS_n chip select can be set to 00000h only if the LCS_n chip select is not active. The MCS_n chip select address range is not allowed to overlap the LCS_n chip select address range. The MCS_n chip select address range is not allowed to overlap the UCS_n chip select address range, either.
8-3	Rsvd	RO	Reserved.
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the wait states inserted for the MCS_n chip selects. The R1 and R0 bits of this register determine the number of wait states to be inserted. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	Wait-State Value. R1 and R0 determine the number of wait states inserted into an access to the MCS_n memory area **R1, R0 -- Wait States** 0, 0 -- 0 0, 1 -- 1 1, 0 -- 2 1, 1 -- 3

Register Offset: A8h
Register Name: PCS_n and MCS_n Auxiliary Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rsvd	M[6:0]							EX	MS	Reserved			R2	R1	R0

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved.
14-8	M[6:0]	R/W	MCS_n Block Size. These bits determine the total block size for the MCS3_n – MCS0_n chip selects. Each individual chip select is active for one quarter of the total block size. For example, if the block size is 32K bytes and the base address located at 20000h, MCS3_n to MCS0_n are individually active from: MCS0_n – 20000h to 21FFFh; MCS1_n – 22000h to 23FFFh; MCS2_n – 24000h to 25FFFh; MCS3_n – 26000h to 27FFFh. MCSx_n total block size is defined by M[6:0], **M[6:0]** , **Total block size**, **MCSx_n address active range** 0000001b , 8K , 2K 0000010b , 16K , 4K 0000100b , 32K , 8K 0001000b , 64K , 16K 0010000b , 128K , 32K 0100000b , 256K , 64K 1000000b , 512K , 128K
7	EX	R/W	Pin Selector. Setting this bit configures the multiplexed outputs as chip selects (PCS6_n – PCS5_n) or A2-A1. Set 1: PCS6_n and PCS5_n are configured as peripheral chip select pins. Set 0: PCS6_n is configured as address bit A2 and PCS5_n configured as A1.
6	MS	R/W	Memory or I/O space selector. This bit determines whether the PCSx_n pins are active during memory or I/O bus cycle. Set 1: The PCSx_n pins are active for memory bus cycle. Set 0: The PCSx_n pins are active for I/O bus cycle.
5-3	Rsvd	RO	Reserved.
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the wait states inserted for the PCS5_n and PCS6_n chip selects. The R1 and R0 bits of this register determine the number of wait states to be inserted. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	Wait-State Value. R1 and R0 determine the number of wait states inserted into an access to the PCS5_n – PCS6_n memory area. **R1, R0 -- Wait States** 0, 0 -- 0 0, 1 -- 1 1, 0 -- 2 1, 1 -- 3

~~11.3~~12.4 PCSx_n

In order to define these pins, the peripheral or memory chip selects are programmed through the A4h and A8h registers. The base address memory block can be located anywhere within the 1M-byte memory space, exclusive of the areas associated with the UCS_n, LCS_n and MCS_n chip selects. If the chip selects are mapped to I/O space, the access range will be 64k bytes. PCS6_n–PCS5_n can be configured from 0 to 3 wait states. PCS3_n–PCS0_n can be configured from 0 to 15 wait states

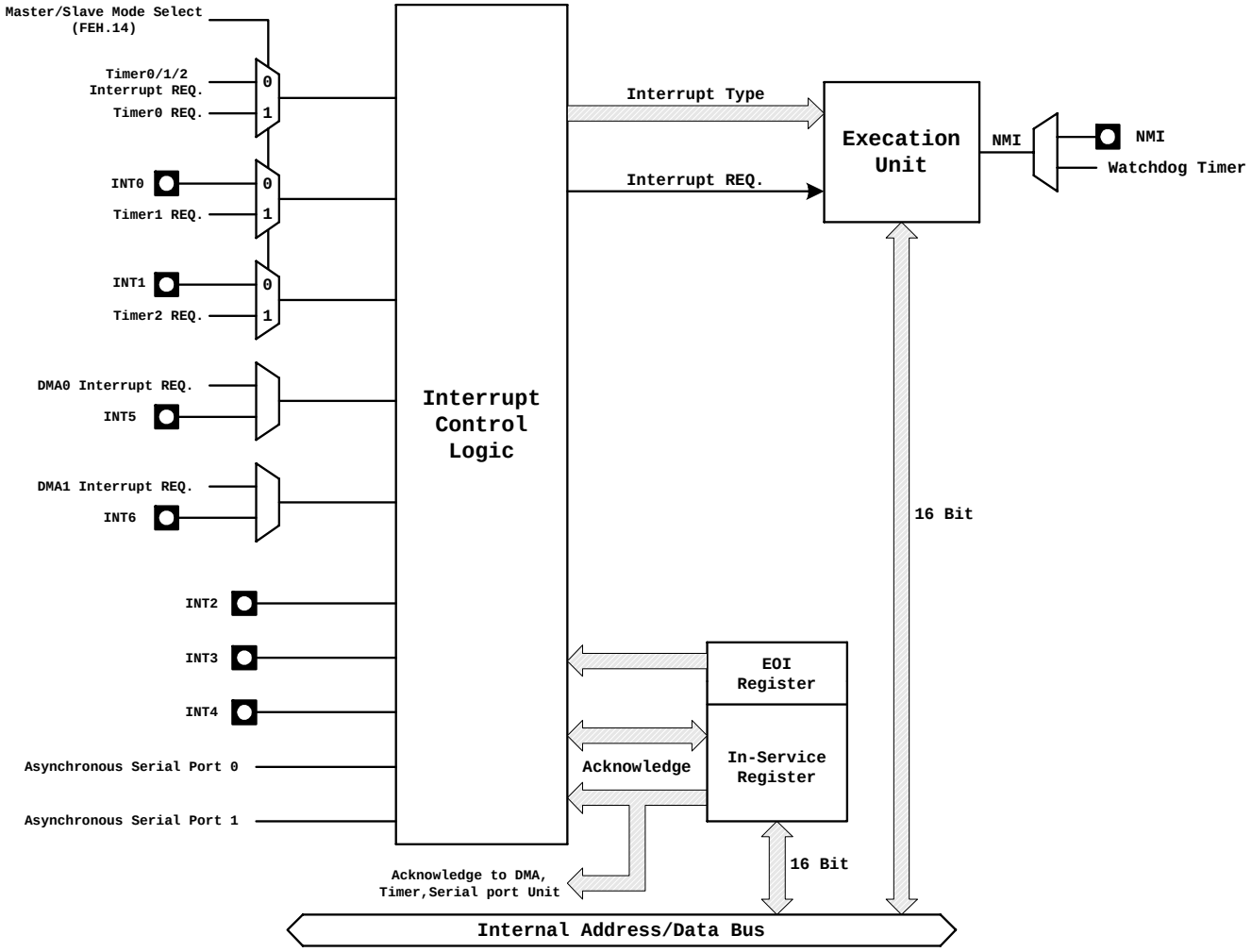
Register Offset: A4h
Register Name: Peripheral Chip Select Register
Reset Value : ~~0000h~~----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA [19:11]									1	1	1	R3	R2	R1	R0

Bit	Name	Attribute	Description
15-7	BA[19:12]	R/W	Base Address. BA[19:11] correspond to bit [19:11] of the 1M-byte (20-bit) programmable base address of the PCS_n chip select block. When the PCS_n chip selects are mapped to I/O space, BA[19:16] must be written to 0000b because the I/O address bus is only 64K bytes (16 bits) wide. **PCSx_n address range:** PCS0_n : Base Address - Base Address+255 PCS1_n : Base Address+256 - Base Address+511 PCS2_n : Base Address+512 - Base Address+767 PCS3_n : Base Address+768 - Base Address+1023 PCS5_n : Base Address+1280 - Base Address+1535 PCS6_n : Base Address+1536 - Base Address+1791
6-4	Rsvd	RO	Reserved.
3	R3	R/W	See bit[1:0].
2	R2	R/W	Ready Mode. This bit is configured to enable/disable the wait states inserted for the PCS3_n–PCS0_n chip selects. The R3, R1 and R0 bits determine the number of wait states to be inserted. Set 1: external ready is ignored. Set 0: external ready is required.
1-0	R[1:0]	R/W	**Bit 3, Bit 1-0: R3, R1, R0**, Wait-State Value. R3, R1 and R0 determine the number of wait states inserted into an access to the PCS3_n–PCS0_n memory area. **R3, R1, R0 -- Wait States** 0, 0, 0 -- 0 0, 0, 1 -- 1 0, 1, 0 -- 2 0, 1, 1 -- 3 1, 0, 0 -- 5 1, 0, 1 -- 7 1, 1, 0 -- 9 1, 1, 1 -- 15

13. Interrupt Controller Unit

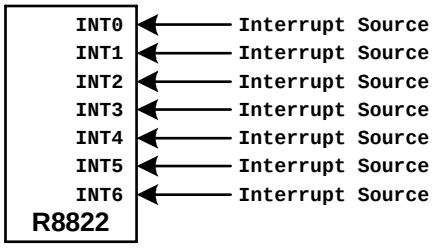
There are 16 interrupt request sources connected to the controller: 7 maskable interrupt pins (INT0 – INT6); 2 non-maskable interrupts (NMI and WDT); 7 internal unit request sources (Timer 0, 1 and 2; DMA 0 and 1; Asynchronous serial port 0 and 1).



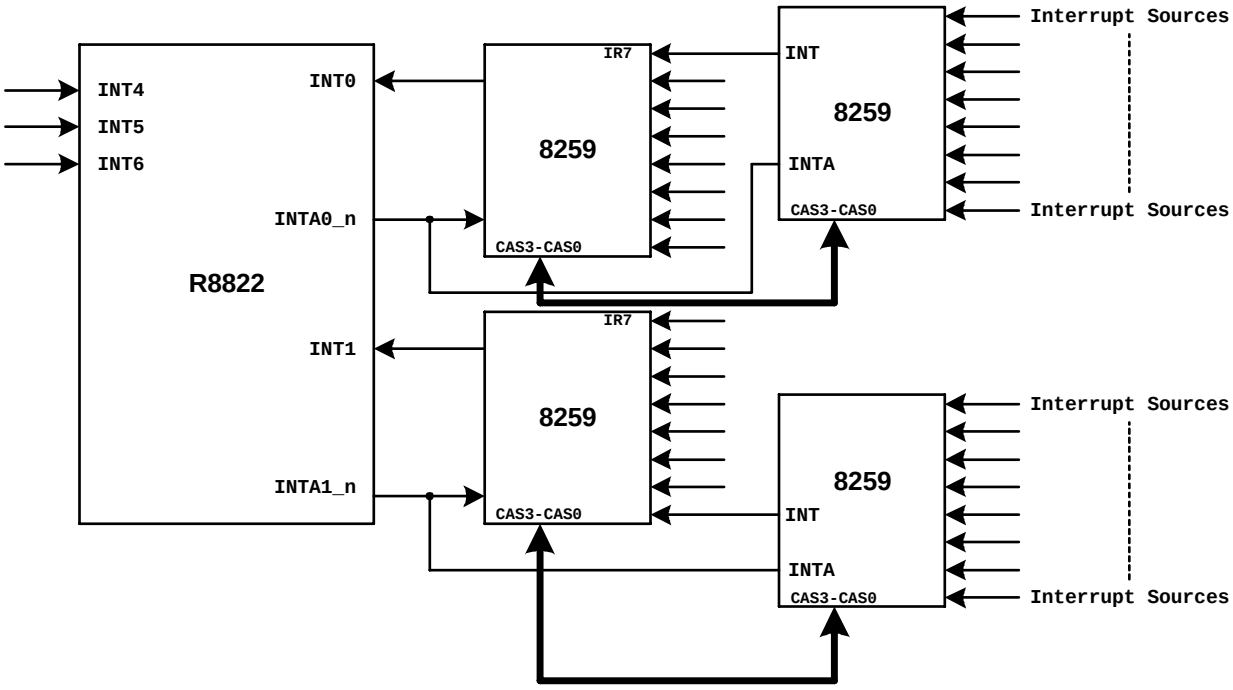
Interrupt Control Unit Block Diagram

13.1 Master Mode and Slave Mode

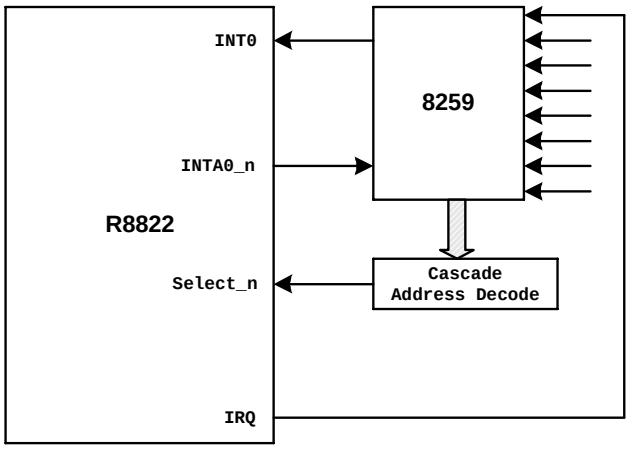
The interrupt controller can be programmed as master or slave mode (by programming FEh [14]). The master mode has two connections: fully nested mode or cascade mode.



Fully Nested Mode Connections



Cascade Mode Connection



Slave Mode Connection

13.2 Interrupt Vectors, Types and Priorities

The following table shows the interrupt vector addresses, types and priorities. Programming the priority registers may change the maskable interrupt priorities. The vector address for each interrupt is fixed.

Interrupt Source	Interrupt Type	Vector Address	EOI Type	Priority	Note
Divide Error Exception	00h	00h		1	
Trace interrupt	01h	04h		1-1	*
NMI	02h	08h		1-2	*
Breakpoint Interrupt	03h	0Ch		1	
INTO Detected Over Flow Exception	04h	10h		1	
Array Bounds Exception	05h	14h		1	
Undefined Opcode Exception	06h	18h		1	
ESC Opcode Exception	07h	1Ch		1	
Timer 0	08h	20h	08h	2-1	*/**
Reserved	09h				
DMA 0/INT5	0Ah	28h	0Ah	3	**
DMA 1/INT6	0Bh	2Ch	0Bh	4	**
INT0	0Ch	30h	0Ch	5	
INT1	0Dh	34h	0Dh	6	
INT2	0Eh	38h	0Eh	7	
INT3	0Fh	3Ch	0Fh	8	
INT4	10h	40h	10h	9	
Asynchronous Serial port 1	11h	44h	11h	9	
Timer 1	12h	48h	08h	2-2	*/**
Timer 2	13h	4Ch	08h	2-3	*/**
Asynchronous Serial port 0	14h	50h	14h	9	
Reserved	15h-1Fh				

***Note** *: When interrupts occur at the same time, the priority is (1-1 > 1-2); (2-1> 2-2 > 2-3).*

***Note **:** The interrupt types of these sources are programmable in slave mode.*

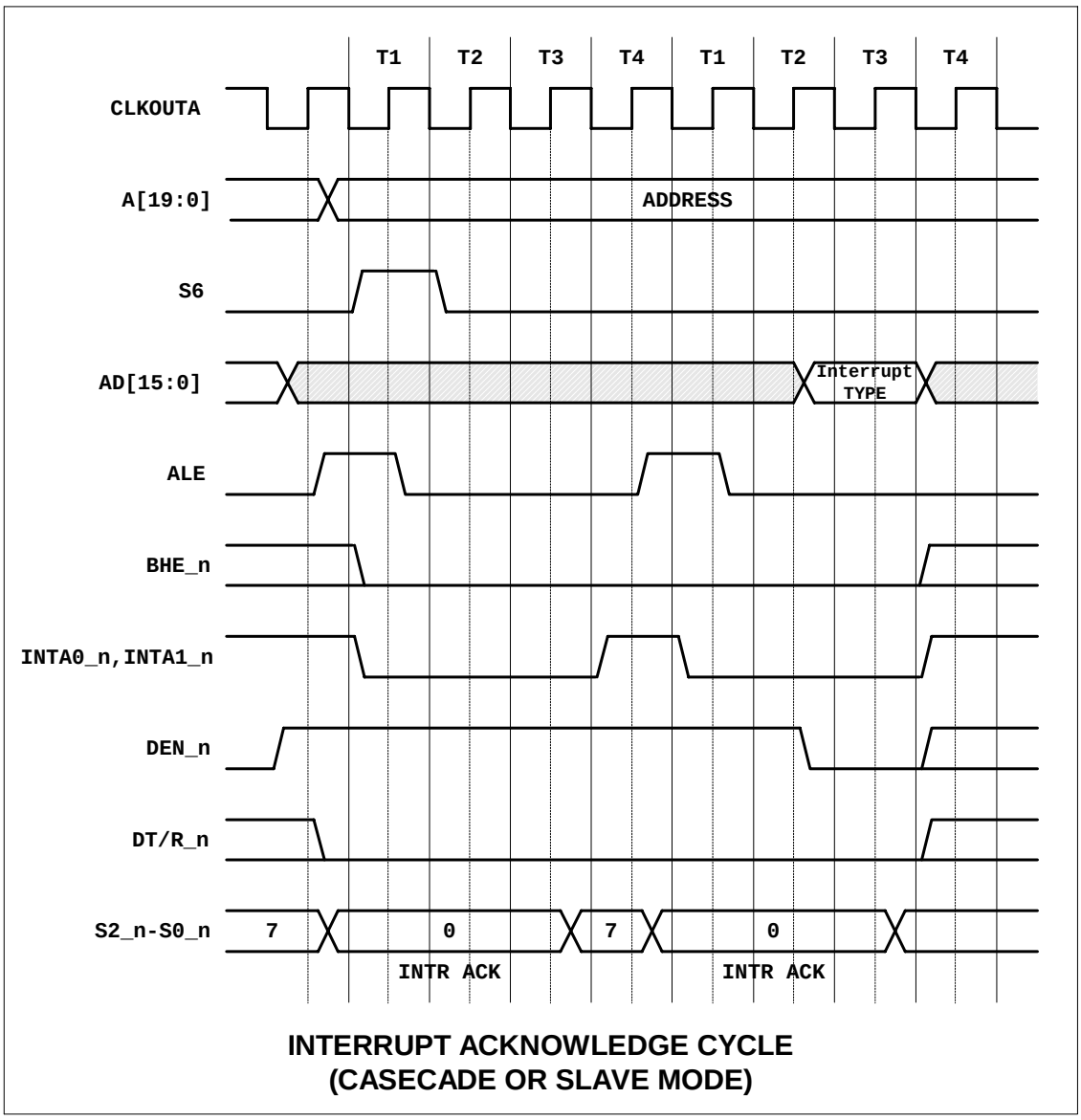
13.3 Interrupt Requests

When an interrupt is requested, the internal interrupt controller verifies that the interrupt is enabled (the IF flag is enabled, but no MSK bit is set) and that there is no higher priority interrupt request being serviced or pending. If the interrupt is granted, the interrupt controller uses the interrupt type to access a vector from the interrupt vector table.

If the external INT is active (level-triggered) to request the interrupt controller service, the INT pins must be held till the micro-controller enters the interrupt service routine. There is no interrupt-acknowledge output when the micro-controller runs in fully nested mode, so the PIO pin should be used to simulate the interrupt-acknowledge pin if necessary.

13.4 Interrupt Acknowledge

The processor requires the interrupt type as an index into the interrupt table. An internal interrupt controller can provide the interrupt type or an external interrupt controller can provide the interrupt type. When the internal interrupt controller provides the interrupt type to the processor, no external bus cycle is generated. When the external interrupt controller provides the interrupt type, the processor will generate two acknowledge bus cycles and the interrupt type will be written to the AD[15:0] lines by the external interrupt controller.



INTERRUPT ACKNOWLEDGE CYCLE (CASECADE OR SLAVE MODE)

13.5 Programming Registers

Registers (**Master mode:** 44h, 42h, 40h, 3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 26h, 24h and 22h; **Slave Mode:** 3Ah, 38h, 36h, 34h, 32h, 30h, 2Eh, 2Ch, 2Ah, 28h, 22h and 20h) are programmed by software to define the interrupt controller operation.

Register Offset: 44h
Register Name: Serial Port 0 Interrupt Control Register
Reset Value : 00~~0~~1Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											1	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for asynchronous serial port 0. Set 0: Enable serial port 0 interrupts.
2-0	PR[2:0]	R/W	Priority. These bits determine the priority of the serial port relative to the other interrupt signals. **The priority selection:** **PR[2:0] — Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 42h
Register Name: Serial Port 1 Interrupt Control Register
Reset Value : 000~~0~~Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for asynchronous serial port 1. Set 0: Enable serial port 1 interrupts.
2-0	PR[2:0]	R/W	Priority. These bits determine the priority of the serial port relative to the other

			interrupt signals. **The priority selection:** **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 40h
Register Name: INT4 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set to 1 and bit 4 ~~set~~ cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved.
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for INT4. Set 0: Enable INT4 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 3Eh
Register Name: INT3 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set to 1 and bit 4 ~~set~~ cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: An interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for INT3. Set 0: Enable INT3 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 3Ch
Register Name: INT2 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	Reserved		LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set and bit 4 ~~set~~ cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6-5	Rsvd	RO	Reserved
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for INT2. Set 0: Enable INT2 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 3Ah
Register Name: INT1 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set and bit 4 ~~set~~ cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode for INT1
5	C	R/W	Cascade Mode. Set 1: Enable the cascade mode for INT1 ~~or INT0~~.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for INT1. Set 0: Enable INT1 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 3Ah
Register Name: Timer 2 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MSK	PR2	PR1	PR0

(Slave Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for Timer 2. Set 0: Enable Timer 2 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 38h
Register Name: INT0 Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ETM	SFNM	C	LTM	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7	ETM	R/W	Edge-Triggered Mode enabled. When this bit is set and bit 4 ~~set~~ cleared to 0, an interrupt is triggered by a low to high edge. The low to high edge will be latched (one level) till this interrupt is serviced.
6	SFNM	R/W	Special Fully Nested Mode. Set 1: Enable the special fully nested mode for INT0
5	C	R/W	Cascade Mode. Set 1: Enable the cascade mode for ~~INT1 or~~ INT0.
4	LTM	R/W	Level-Triggered Mode. Set 1: An Interrupt is triggered by the active-high level. Set 0: An interrupt is triggered by the low to high edge.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for INT0. Set 0: Enable INT0 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 38h
Register Name: Timer 1 Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												MSK	PR2	PR1	PR0

(Slave Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for Timer 1. Set 0: Enable Timer 1 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 36h
Register Name: DMA1/INT6 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for the DMA1 controller. Set 0: Enable DMA1 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 36h
Register Name: DMA1/INT6 Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for the DMA 1 controller. Set 0: Enable DMA1 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 34h
Register Name: DMA0/INT5 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for the DMA 0 controller. Set 0: Enable DMA0 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 34h
Register Name: DMA0/INT5 Interrupt Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for the DMA 0 controller. Set 0: Enable DMA0 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 32h
Register Name: Timer Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Master Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3	MSK	R/W	Mask. Set 1: Mask the interrupt sources for timer controllers. Set 0: Enable interrupts for timer controllers.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 32h
Register Name: Timer 0 Interrupt Control Register
Reset Value : 000Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	MSK	PR2	PR1	PR0

(Slave Mode)

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved.
3	MSK	R/W	Mask. Set 1: Mask the interrupt source for the Timer 0 controller. Set 0: Enable Timer 0 interrupts.
2-0	PR[2:0]	R/W	Interrupt Priority. These bit settings for priority selections are the same as those of bit[2:0] in the 44h register.

Register Offset: 30h
Register Name: Interrupt Status Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved												TMR2	TMR1	TMR0

(Master Mode)

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-maskable interrupts occur. Set 0: When an IRET instruction is executed.
14-3	Rsvd	RO	Reserved.
2-0	TMR[2:0]	R/W	Set 1: Indicate that the corresponding timer has an interrupt request pending.

Register Offset: 30h
Register Name: Interrupt Status Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DHLT	Reserved												TMR2	TMR1	TMR0

(Slave Mode)

Bit	Name	Attribute	Description
15	DHLT	RO	DMA Halt. Set 1: Halt any DMA activity when non-maskable interrupts occur. Set 0: When an IRET instruction is executed.
14-3	Rsvd	RO	Reserved.
2-0	TMR[2:0]	R/W	Set 1: Indicate that the corresponding timer has an interrupt request pending.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	I4	I~~1~~3	~~1~~I2	~~1~~I1	~~1~~I0	D1/I6~~1~~	D0/I5	Rsvd	TMR

(Master Mode)

The Interrupt Request register is a read-only register. For internal interrupts (SP0, SP1, D1/I6, D0/I5 and TMR), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge. For INT4-INT0 external interrupts, the corresponding bits (I[4:0]) reflect the current values of the external signals.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved.
10	SP0	RO	Serial Port 0 Interrupt Request. Indicates the interrupt status of serial port 0.
9	SP1	RO	Serial Port 1 Interrupt Request. Indicates the interrupt status of serial port 1.
8-4	~~1~~I[4:~~1~~0]	~~R/W~~RO	Interrupt Requests. Set 1: The corresponding INT pin has an interrupt pending.
3-2	D1/~~1~~I6 D0/I5	~~R/W~~RO	DMA Channel or INT Interrupt Request. Set 1: The corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved.
0	TMR	~~R/W~~RO	Timer Interrupt Request. Set 1: The timer control unit has an interrupt pending.

Register Offset: 2Eh
Register Name: Interrupt Request Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										~~1~~TMR2	~~1~~TRM1	D1/I6~~1~~	D0/I5	Rsvd	TMR0

(Slave Mode)

The Interrupt Request register is a read-only register. For internal interrupts (D1/I6, D0/I5, TMR2, TMR1 and TMR0), the corresponding bit is set to 1 when the device requests an interrupt. The bit is reset during the internally generated interrupt acknowledge.

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved.
6-4	~~I~~TMR[2:1~~I~~]	~~R/W~~RO	Timer2/Timer1 Interrupt Request. Set 1: Indicates the state of any interrupt requests from the associated timer.
3-2	D1/I6 D0/I5	~~R/W~~RO	DMA Channel or INT Interrupt Request. Set 1: The corresponding DMA channel or INT has an interrupt pending.
1	Rsvd	RO	Reserved.
0	TMR0	~~R/W~~RO	Timer0 Interrupt Request. Set 1: Indicates the state of an interrupt request from Timer 0.

Register Offset: 2Ch
Register Name: Interrupt In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	I4	~~I~~I3	~~I~~I2	~~I~~I1	~~I~~I0	D1/~~I~~I6	D0/~~I~~I5	Rsvd	TMR

(Master Mode)

In this Register, bits are set by the interrupt controller when the interrupt is taken and cleared by writing the corresponding interrupt type to the EOI register.

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved.
10	SP0	RO	Serial Port 0 Interrupt In-Service. Set 1: The serial port 0 interrupt is currently being serviced.
9	SP1	RO	Serial Port 1 Interrupt In-Service. Set 1: The serial port 1 interrupt is currently being serviced.
8-4	~~I~~I[4:~~I~~0]	RO	Interrupt In-Service. Set 1: The corresponding INT interrupt is currently being serviced.
3-2	D1/~~I~~I6 – D0/~~I~~I5	RO	DMA Channel or INT Interrupt In-Service. Set 1:The corresponding DMA channel or INT interrupt is currently being serviced.
1	Rsvd	RO	Reserved.
0	TMR	RO	Timer Interrupt In-Service. Set 1: The timer interrupt is currently being serviced.

Register Offset: 2Ch
Register Name: Interrupt In-Service Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/16	D0/15	Rsvd	TMR0

(Slave Mode)

In this Register, bits are set by the interrupt controller when the interrupt is taken and cleared by writing the corresponding interrupt type to the EOI register.

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved.
5-4	TMR[2:1]	Ro	Timer2/Timer1 Interrupt In-Service. Set 1: The corresponding timer interrupt is currently being serviced.
3-2	D1/~~1~~I6 – D0/~~1~~I5	RO	DMA Channel or INT Interrupt In-Service. Set 1: The corresponding DMA Channel or INT Interrupt is currently being serviced.
1	Rsvd	RO	Reserved.
0	TMR0	RO	Timer 0 Interrupt In-Service. Set 1: The Timer 0 interrupt is currently being serviced.

Register Offset: 2Ah
Register Name: Interrupt Priority Mask Register
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Master Mode) It determines the minimum priority level at which maskable interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved.
2-0	PRM[2:0]	R/W	Priority Field Mask, It determines the minimum priority that is required in order for a maskable interrupt source to generate an interrupt. **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 2Ah
Register Name: Interrupt Priority Mask Register
Reset Value : 0007h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRM2	PRM1	PRM0

(Slave Mode) It determines the minimum priority level at which maskable interrupts can generate interrupts.

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved.
2-0	PRM[2:0]	R/W	Priority Field Mask, It determines the minimum priority that is required in order for a maskable interrupt source to generate an interrupt. **PR[2:0]** — **Priority** 000 — (High) 0 001 — 1 010 — 2 011 — 3 100 — 4 101 — 5 110 — 6 111 — (Low) 7

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : 07FD~~0~~h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					SP0	SP1	I4	~~I~~3	~~I~~2	~~I~~1	~~I~~0	D1/~~I~~6	D0/~~I~~5	Rsvd	TMR

(Master Mode)

Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved.
10	SP0	RO	Serial Port 0 Interrupt Mask. It indicates the state of the mask bit for the asynchronous serial port 0 interrupt.
9	SP1	RO	Serial Port 1 Interrupt Mask. It indicates the state of the mask bit for the asynchronous serial port 1 interrupt.
8-4	I[4:0]	RO	Interrupt Masks. They indicate the states of the mask bits for the corresponding interrupts.
3-2	D1/~~I~~6 – D0/~~I~~5	RO	DMA Channel or INT Interrupt Masks. They indicate the states of the mask bits for the corresponding DMA channel or INT interrupts.
1	Rsvd	RO	Reserved.
0	TMR	RO	Timer Interrupt Mask. It indicates the state of the mask bit for the timer control unit.

Register Offset: 28h
Register Name: Interrupt Mask Register
Reset Value : 003~~0~~Dh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										TMR2	TMR1	D1/~~I~~6	D0/~~I~~5	Rsvd	TMR0

(Slave Mode)

Bit	Name	Attribute	Description
15-6	Rsvd	RO	Reserved.
5-4	TMR[2:1]	RO	Timer2/Timer1 Interrupt Mask. They indicate the states of the mask bits in the Timer Interrupt Control Register. Set 1: Timer2 or Time1 has its interrupt requests masked
3-2	D1/~~I~~6 – D0/~~I~~5	RO	DMA Channel or INT Interrupt Masks. They indicate the states of the mask bits in the corresponding DMA or INT6/INT5 Control Registers.
1	Rsvd	RO	Reserved.
0	TMR0	RO	Timer0 Interrupt Mask. It indicates the state of the mask bit in the Timer Interrupt Control Register

Register Offset: 26h
Register Name: Interrupt Poll Status Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

(Master Mode)

The Interrupt Poll Status Register mirrors the current state of the Interrupt Poll Register. This register can be read without affecting the current interrupt requests.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved.
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

Register Offset: 24h
Register Name: Interrupt Poll Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IREQ	Reserved										S[4:0]				

(Master Mode)

When the Interrupt Poll Register is read, the current interrupt is acknowledged and the next interrupt takes its place in the Interrupt Poll Register.

Bit	Name	Attribute	Description
15	IREQ	R/W	Interrupt Request. Set 1: if an interrupt is pending. The S[4:0] field contains valid data.
14-5	Rsvd	RO	Reserved.
4-0	S[4:0]	R/W	Poll Status. It indicates the interrupt type of the highest priority pending interrupts.

Register Offset: 22h
Register Name: End-of-Interrupt Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NSPEC	Reserved										S[4:0]				

(Master Mode)

Bit	Name	Attribute	Description
15	NSPEC	R/W	Non-Specific EOI. Set 1: indicates the non-specific EOI. Set 0: indicates the specific EOI interrupt type in S[4:0].
14-5	Rsvd	RO	Reserved.
4-0	S[4:0]	~~R/W~~WO	Source EOI Type. It specifies the EOI type of the interrupt that is currently being processed.

Note: *We suggest that the specific EOI is the most secure method to use for resetting the In-Service bit.*

Register Offset: 22h
Register Name: Specific End-of-Interrupt Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	L2	L1	L0

(Slave Mode)

Bit	Name	Attribute	Description
15-3	Rsvd	RO	Reserved.
2-0	L[2:0]	~~R~~WO	Interrupt Type. The encoded value indicates the priority of the IS (interrupt service) bit to be reset. Writes to these bits cause an EOI issued for the interrupt type in slave mode.

Register Offset: 20h
Register Name: Interrupt Vector Register
Reset Value : 0000h

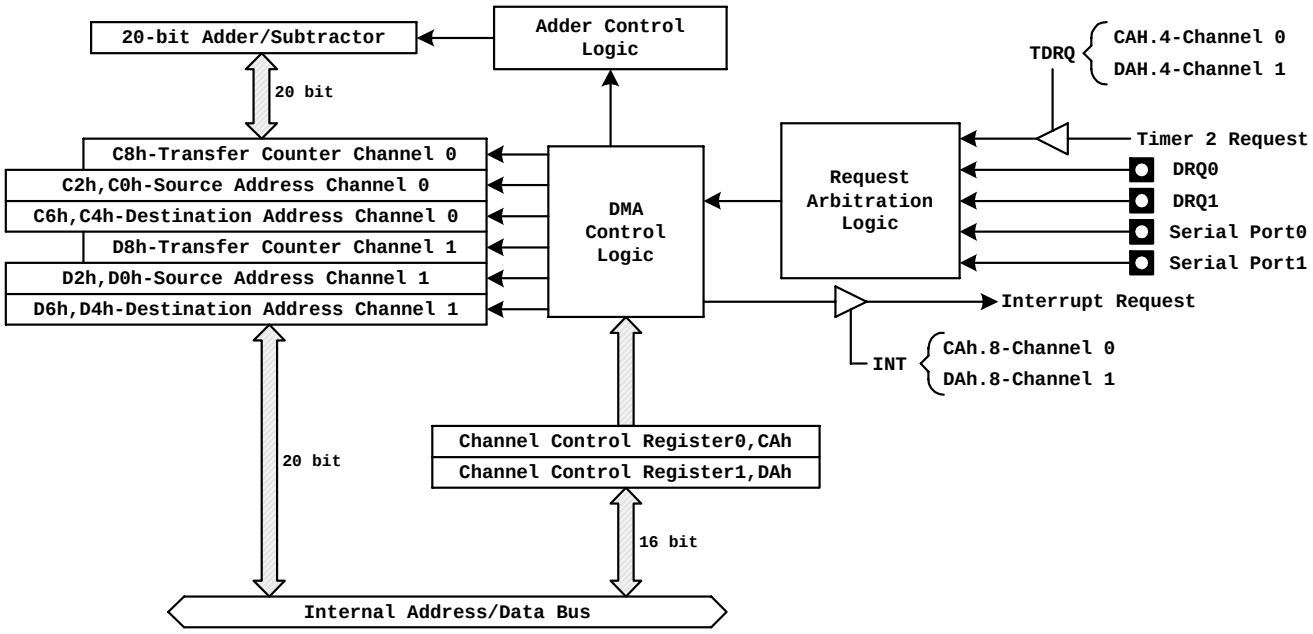
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	T[4:0]					0	0	0

(Slave Mode)

Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-3	T[4:0]	R/W	Interrupt Types. The following interrupt types in slave mode can be programmed. Timer 2 interrupt controller: (T4, T3, T2, T1, T0, 1, 0, 1) b. Timer 1 interrupt controller: (T4, T3, T2, T1, T0, 1, 0, 0) b. DMA 1 interrupt controller: (T4, T3, T2, T1, T0, 0, 1, 1) b. DMA 0 interrupt controller: (T4, T3, T2, T1, T0, 0, 1, 0) b. Timer 0 interrupt controller: (T4, T3, T2, T1, T0, 0, 0, 0) b.
2-0	Rsvd	RO	Reserved.

14. DMA Unit

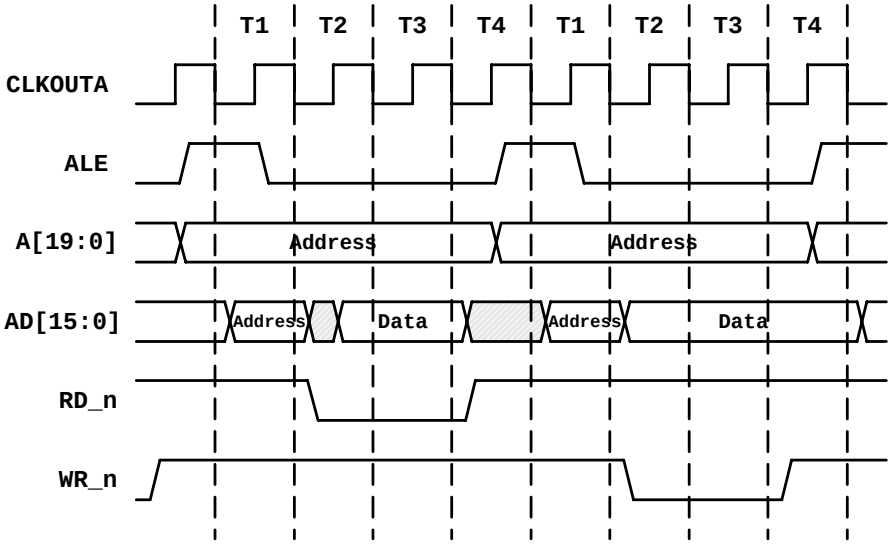
The DMA controller provides the data transfers between the memory and peripherals without the intervention of the CPU. There are two DMA channels in the DMA unit. Each channel can accept DMA requests from one of three sources: external pins (DRQ0 for channel 0 or DRQ1 for channel 1), serial ports (port 0 or port 1), or Timer 2 overflow. The data transfers from sources to destinations can be memory to memory, memory to I/O, I/O to I/O, or I/O to memory. Either bytes or words can be transferred to or from even or odd addresses and two bus cycles are necessary (reads from sources and writes to destinations) for each data transfer.



DMA Unit Block

14.1 DMA Operation

Every DMA transfer consists of two bus cycles (see figure of Typical DMA Transfers). These two bus cycles cannot be separated by a bus hold request, a refresh request or another DMA request. Registers CAh, C8h, C6h, C4h, C2h, C0h, DAh, D8h, D6h, D4h, D2h and D0h are used to configure and operate the two DMA channels.



Typical DMA Trarsfers

Register Offset: CAh (DMA0)
Register Name: DMA0 Control Register
Reset Value : ~~FFF9h~~0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

Bit	Name	Attribute	Description
15	DM/IO_n	R/W	Destination Address Space Select. Set 1: The destination address is in memory space. Set 0: The destination address is in I/O space.
14	DDEC	R/W	Destination Decrement. Set 1: The destination address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decremented value is by 1 or 2. When both the DDEC and DINC bits are set to the same value (1 or 0), the address remains constant. Set 0: Disable the decrement function.
13	DINC	R/W	Destination Increment. Set 1: The destination address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the increment function.
12	SM/IO_n	R/W	Source Address Space Select.

			Set 1: The Source address is in memory space. Set 0: The Source address is in I/O space.
11	SDEC	R/W	Source Decrement. Set 1: The Source address is automatically decremented after each transfer. The B_n/W (bit 0) bit determines the decremented value is by 1 or 2. When both the SDEC and SINC bits are set to the same value (1 or 0), the address remains constant. Set 0: Disable the decrement function.
10	SINC	R/W	Source Increment. Set 1: The Source address is automatically incremented after each transfer. The B_n/W (bit 0) bit determines the incremented value is by 1 or 2. Set 0: Disable the increment function.
9	TC	R/W	Terminal Count. Set 1: Synchronized DMA transfers terminate when the DMA Transfer Count Register reaches 0. Set 0: Synchronized DMA transfers do not terminate when the DMA Transfer Count Register reaches 0. Unsynchronized DMA transfers always terminate when the DMA transfer count register reaches 0, regardless of the setting of this bit.
8	INT	R/W	Interrupt. Set 1: The DMA unit generates an interrupt request on completion of the transfer count. The TC bit must be set to 1 to generate an interrupt.
7-6	SYN[1:0]	R/W	Synchronization Type Selection. **SYN1 , SYN0 -- Synchronization Type** 0 , 0 -- Unsynchronized 0 , 1 -- Source synchronized 1 , 0 -- Destination synchronized 1 , 1 -- Reserved
5	P	R/W	Priority. Set 1: It selects high priority for this channel when both DMA 0 and DMA 1 are transferred at the same time.
4	TDRQ	R/W	Timer Enable/Disable Request. Set 1: Enable the DMA requests from Timer 2. Set 0: Disable the DMA requests from Timer 2.
3	~~Rsvd~~EXT	R~~O~~/W	External I~~Reserved~~nterrupt Enable bit. Set 1: The external pin functions as an interrupt pin (The DMA 0 function is disabled.) Set 0: The external pin functions as a DRQ pin.
2	CHG	R/W	Changed Start bit. This bit must be set to 1 when the ST bit is modified.
1	ST	R/W	Start/Stop DMA channel. Set 1: Start the DMA channel Set 0: Stop the DMA channel
0	B_n/W	R/W	Byte/Word Select. Set 1: Word select. The address is incremented or decremented by 2 after each transfer. Set 0: Byte select. The address is incremented or decremented by 1 after each transfer.

Register Offset: C8h (DMA0)
Register Name: DMA0 Transfer Count Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA0 Transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: C6h (DMA0)
Register Name: DMA0 Destination Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DDA[19:16]	R/W	High DMA 0 Destination Address. These bits are mapped to A[19:16] during a DMA transfer when the destination address is in memory or I/O space. If the destination address is in I/O space (64K bytes), these bits must be programmed to 0000b.

Register Offset: C4h (DMA0)
Register Name: DMA0 Destination Address Low Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA0 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: C2h (DMA0)
Register Name: DMA0 Source Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DSA[19:16]			

Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DSA[19:16]	R/W	High DMA0 Source Address. These bits are mapped to A[19:16] during a DMA transfer when the source address is in memory or I/O space. If the source address is in I/O space (64K bytes), these bits must be programmed to 0000b

Register Offset: C0h (DMA0)
Register Name: DMA0 Source Address Low Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSA[15:0]															

Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA0 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: DAh (DMA1)
Register Name: DMA1 Control Register
Reset Value : ~~FFF9h~~0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM/IO_n	DDEC	DINC	SM/IO_n	SDEC	SINC	TC	INT	SYN1	SYN0	P	TDRQ	EXT	CHG	ST	B_n/W

The definitions of bit[15:0] for DMA 1 are the same as those of bit[15:0] in Register CAh for DMA0.

Register Offset: D8h (DMA1)
Register Name: DMA1 Transfer Count Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	DMA 1 transfer Count. The value of this register will be decremented by 1 after each transfer.

Register Offset: D6h (DMA1)
Register Name: DMA1 Destination Address High Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												DDA[19:16]			

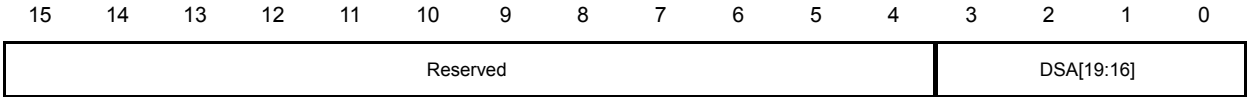
Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DDA[19:16]	R/W	High DMA1 Destination Address. These bits are mapped to A[19:16] during a DMA transfer when the destination address is in memory or I/O space. If the destination address is in I/O space (64K bytes), these bits must be programmed to 0000b.

Register Offset: D4h (DMA1)
Register Name: DMA1 Destination Address Low Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDA[15:0]															

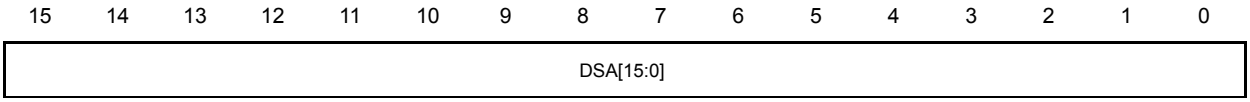
Bit	Name	Attribute	Description
15-0	DDA[15:0]	R/W	Low DMA 1 Destination Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DDA [19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

Register Offset: D2h (DMA1)
Register Name: DMA1 Source Address High Register
Reset Value : -----



Bit	Name	Attribute	Description
15-4	Rsvd	RO	Reserved
3-0	DSA[19:16]	R/W	High DMA 1 Source Address. These bits are mapped to A[19:16] during a DMA transfer when the source address is in memory or I/O space. If the source address is in I/O space (64K bytes), these bits must be programmed to 0000b.

Register Offset: D0h (DMA1)
Register Name: DMA1 Source Address Low Register
Reset Value : -----

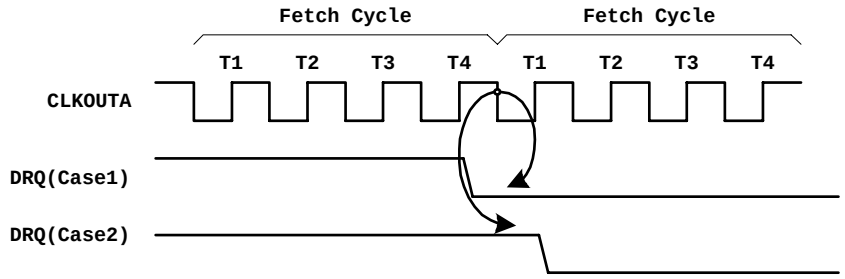


Bit	Name	Attribute	Description
15-0	DSA[15:0]	R/W	Low DMA1 Source Address. These bits are mapped to A[15:0] during a DMA transfer. The value of DSA[19:0] will be incremented or decremented by 2 or 1 after each DMA transfer.

14.2 External Requests

External DMA requests are asserted on the DRQ pins. The DRQ pins are sampled on the falling edge of ~~CLKOUTA~~CLKOUTA. It takes a minimum of four clocks before the DMA cycle is initiated by the Bus Interface. The DMA request is cleared four clocks before the end of the DMA cycle. No DMA acknowledge is provided, since the chip-selects (MCSx_n and ~~MCSx_n,~~PCSx_n) can be programmed to be active for a given block of memory or I/O space, and the DMA source and destination address registers can be programmed to point to the same given block.

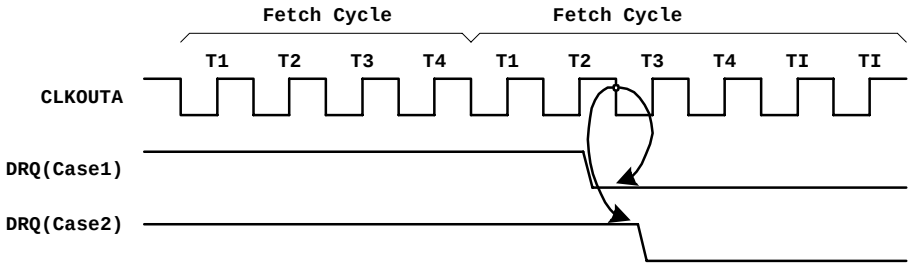
DMA transfers can be either source- or destination-synchronized, and they can also be unsynchronized. The Source-Synchronized Transfers figure shows the typical source-synchronized transfers which provide the source device at least three clock cycles from the time it is acknowledged to de-assert its DRQ line.



NOTES:
Case1 : The current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : The current source synchronized transfer will be immediately followed by antoher DMA transfer.

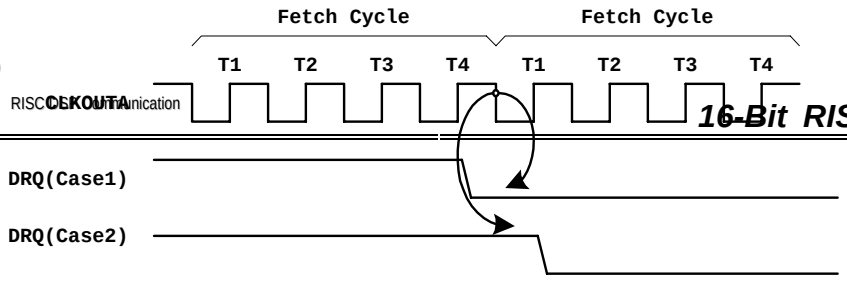
Source-Synchronized Transfers

The Destination-Synchronized Transfers figure shows the typical destination-synchronized transfer which differs from a source-synchronized transfer in which two idle states are added to the end of the deposit cycle. The two idle states extend the DMA cycle to allow the destination device to de-assert its DRQ pin four clocks before the end of the cycle. If the two idle states were not inserted, the destination device would not have time to de-assert its DRQ signal.



NOTES:
Case1 : The current destination synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : The current destination synchronized transfer will be immediately followed by another DMA transfer.

Destination-Synchronized Transfers



NOTES:
Case1 : Current source synchronized transfer will not be immediately followed by another DMA transfer.
Case2 : Current source synchronized transfer will be immediately followed by antoher DMA transfer.

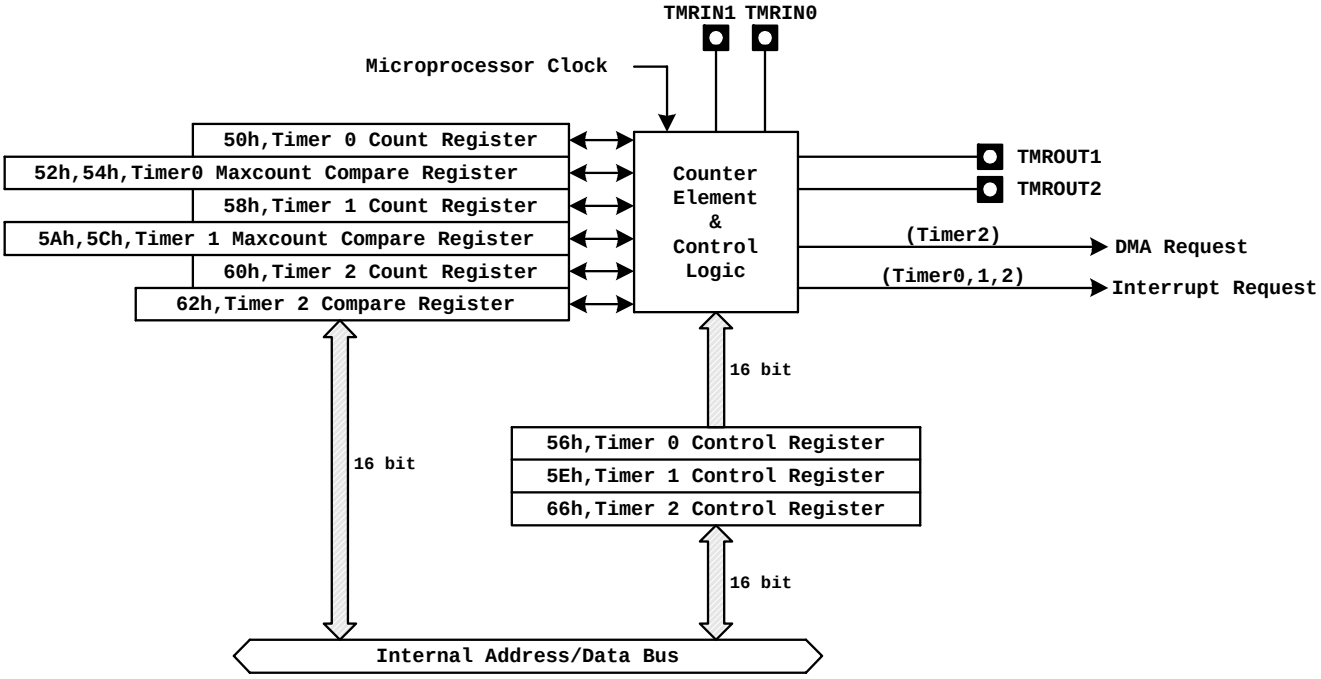
Source-Synchronized Transfers

14.3 Serial Port/DMA Transfers

Serial port data can be transferred to or from memory or I/O space via DMA. The B_n/W bit of the DMA Control Register must be set to 0 for byte transfers. The map address of the Transmit Data Register is written to the DMA Destination Address Register and the memory or I/O address to the DMA Source Address Register when the data are transmitted. The mapped address of the Receive Data Register is written to the DMA Source Address Register and the memory or I/O address to the DMA Destination Address Register when the data are received.

The Serial Port Control Register is programmed by software to perform the serial port/DMA transfers. When a DMA channel is in use by a serial port, the corresponding external DMA request signal is de-activated. For DMA transfers to the serial port, the DMA channel should be configured as being destination-synchronized. For DMA transfers from the serial port, the DMA channel should be configured as being source-synchronized.

15. Timer Control Unit



Timer / Counter Unit Block

There are three 16-bit programmable timers in the R8822. The timer operation is independent of the CPU. These three timers can be programmed as timer elements or as counter elements. Timer 0 and 1 are each connected to two external pins (TMRIN0, TMROUT0, TMRIN1 and TMROUT1), which can be used to count or time external events, or used to generate variable-duty-cycle waveforms. Timer 2 is not connected to any external pins. It can be used as a pre-scaler to Timer 0 and Timer 1 or as a DMA request source.

Register Offset: 56h
Register Name: Timer 0 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable bit. Set 1: Timer 0 is enabled. Set 0: Timer 0 is inhibited from counting. The INH_n bit must be set to 1 when the EN bit is written, and both the INH_n and EN bits must be in the same write.
14	INH_n	R/W	Inhibit bit.

			This bit allows selectively updating the EN bit. The INH_n bit must be set to 1 when the EN bit is written, and both the INH_n and EN bits must be in the same write. This bit is not stored and always read as 0.
13	INT	R/W	Interrupt bit. Set 1: An interrupt request is generated when the count register equals a maximum count. If the timer is configured in dual max-count mode, an interrupt is generated each time when the count reaches Max-Count A or Max-Count B. Set 0: Timer 0 will not issue interrupt requests.
12	RIU	R/W	Register in Use bit. Set 1: The Maxcount Compare B Register of Timer 0 is being used. Set 0: The Maxcount Compare A Register of Timer 0 is being used.
11-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. In dual maxcount mode, this bit is set each time when either the Maxcount Compare A or Maxcount Compare B register is reached. This bit is set regardless of the INT bit (offset 56h.13).
4	RTG	R/W	Re-trigger bit. This bit defines the control function by the input signal of the TMRIN0 pin. When EXT=1 (56h.2), this bit is ignored. Set 1: Timer 0 Count Register (50h) counts internal events; resets the counting on every TMRIN0 input signal from low to high (rising edge trigger). Set 0: Low input holds the Timer 0 Count Register (50h) value; high input enables the counting which counts internal events. **The definitions of setting the (EXT, RTG)** (0, 0) – Timer 0 counts the internal events if the TMRIN0 pin remains high. (0, 1) – Timer 0 counts the internal events; the count register is reset on every rising transition on the TMRIN0 pin. (1, x) – The TMRIN0 pin input functions as clock source and Timer 0 Count Register is incremented by one every external clock.
3	P	R/W	Pre-scaler bit. This bit and EXT (56h.2) define Timer 0 clock source. **The definitions of setting the (EXT, P)** (0, 0) – The Timer 0 Count Register is incremented by one every four internal processor clock. (0, 1) – The Timer 0 Count Register is incremented by one which is pre-scaled by Timer 2. (1, x) – The TMRIN0 pin input functions as clock source and the Timer 0 Count Register is incremented by one every external clock.
2	EXT	R/W	External Clock bit. Set 1: Timer 0 clock source from external events. Set 0: Timer 0 clock source from system clock.
1	ALT	R/W	Alternate Compare bit. This bit controls whether the timer runs in single or dual maximum count mode. Set 1: Specify dual maximum count mode. In this mode, the timer counts to Maxcount Compare A and resets the count register to 0. Then the timer counts to Maxcount Compare B, resets the count register to 0 again, and starts over with Maxcount Compare A. Set 0: Specify single maximum count mode. In this mode, the timer counts to the value contained in Maxcount Compare A and resets the count register to 0. Then the timer counts to Maxcount Compare A again. Maxcount Compare B is not used in this mode.
0	CONT	R/W	Continuous Mode bit. Set 1: The timer runs continuously. Set 0: The timer will halt after each counting to the maximum count and the EN bit will be cleared.

Register Offset: 50h
Register Name: Timer 0 Count Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Count Value. This register contains the current count of Timer 0. The count is incremented by one every four internal processor clocks, pre-scaled by Timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN0 signal.

Register Offset: 52h
Register Name: Timer 0 Maxcount Compare A Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare A Value.

Register Offset: 54h
Register Name: Timer 0 Maxcount Compare B Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 0 Compare B Value.

Register Offset: 5Eh
Register Name: Timer 1 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	RIU	0	0	0	0	0	0	MC	RTG	P	EXT	ALT	CONT

These bit definitions for timer 1 are the same as those in Register 56h for timer 0.

Register Offset: 58h
Register Name: Timer 1 Count Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Count Value. This register contains the current count of Timer 1. The count is incremented by one every four internal processor clocks, pre-scaled by Timer 2, or incremented by one every external clock which is through configuring the external clock select bit based on the TMRIN1 signal.

Register Offset: 5Ah
Register Name: Timer 1 Maxcount Compare A Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare A Value.

Register Offset: 5Ch
Register Name: Timer 1 Maxcount Compare B Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 1 Compare B Value.

Register Offset: 66h
Register Name: Timer 2 Mode/Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	INH_n	INT	0	0	0	0	0	0	0	MC	0	0	0	0	CONT

Bit	Name	Attribute	Description
15	EN	R/W	Enable bit. Set 1: Timer 2 is enabled. Set 0: Timer 2 is inhibited from counting. The INH_n bit must be set to 1 when the EN bit is written, and both the INH_n and EN bits must be in the same write.
14	INH_n	R/W	Inhibit bit. This bit allows selectively updating the EN bit. The INH_n bit must be set to 1 when the EN bit is written, and both the INH_n and EN bits must be in the same write. This bit is not stored and is always read as 0.
13	INT	R/W	Interrupt bit. Set 1: An interrupt request is generated when the count register equals a maximum count. Set 0: Timer 2 will not issue interrupt requests.
12-6	Rsvd	RO	Reserved
5	MC	R/W	Maximum Count bit. When the timer reaches its maximum count, the MC bit will be set to 1 by H/W. This bit is set regardless of the INT bit (66h.13).
4-1	Rsvd	RO	Reserved
0	CONT	R/W	Continuous Mode bit. Set 1: The timer is continuously running when it reaches the maximum count. Set 0: The EN bit (66h.15) is cleared and the timer is held after each timer count reaches the maximum count.

Register Offset: 60h
Register Name: Timer 2 Count Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Count Value. This register contains the current count of Timer 2. The count is incremented by one every four internal processor clocks.

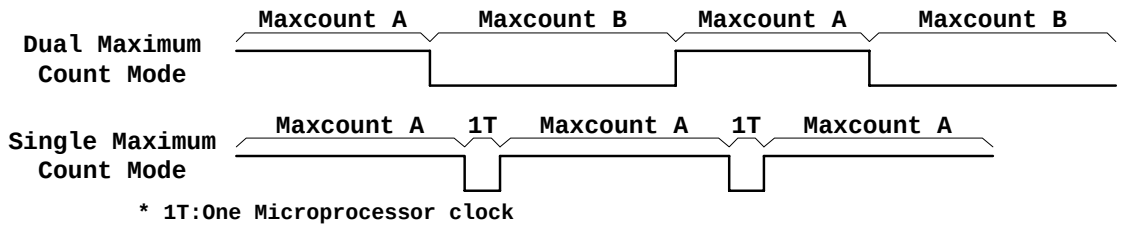
Register Offset: 62h
Register Name: Timer 2 Maxcount Compare A Register
Reset Value : ——

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC[15:0]															

Bit	Name	Attribute	Description
15-0	TC[15:0]	R/W	Timer 2 Compare A Value.

15.1 Timer/Counter Unit Output Mode

Timers 0 and 1 can use one maximum count value or two maximum count values. Timer 2 can use only one maximum count value. Timer 0 and Timer 1 can be configured to be single or dual maximum count mode. The TMROUT0 or TMROUT1 signals can be used to generate waveforms of various duty cycles.



Timer/Counter Unit Output Modes

~~15.2~~16. Watchdog Timer

The R8822 has one independent watchdog timer, which is programmable. The watchdog timer is active after reset and the timeout count is with a maximum count value. The keyed sequence (3333h, CCCCh) must be written to the register (E6h) first, then the new configuration to the Watchdog Timer Control Register. It is a single write, so every write to the Watchdog Timer Control Register must follow this rule.

When the watchdog timer is active, an internal counter is counting. If this internal count is over the watchdog timer duration, the watchdog timeout will happen. The keyed sequence (AAAAh, 5555h) must be written to the register (E6h) to reset the internal count and prevent the watchdog timeout. The internal count should be reset before the watchdog timer timeout period is modified to ensure that an immediate timeout will not occur.

Register Offset: ~~60h~~E6h
Register Name: ~~Timer 2 Count Register~~Watchdog Timer Control Register
Reset Value : ~~——~~C080h

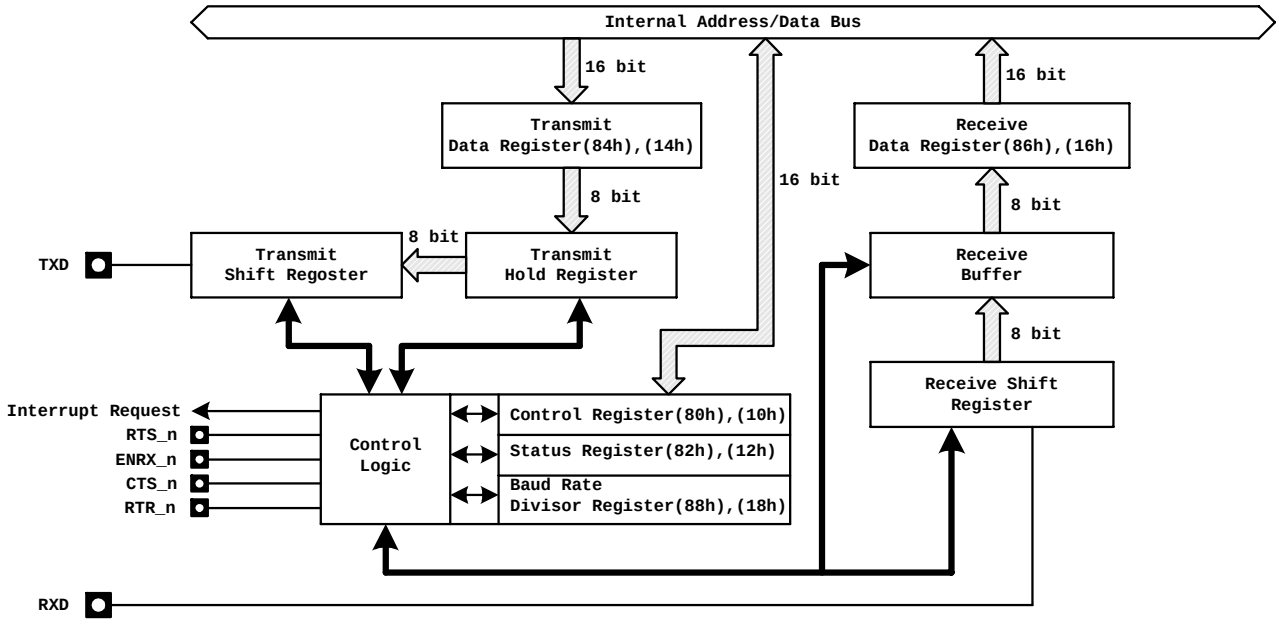
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA	WRST	RSTFLAG	NMIFLAG	Reserved				COUNT							

Bit	Name	Attribute	Description
15	ENA	R/W	Enable the Watchdog Timer. Set 1: Enable the watchdog timer. Set 0: Disable the watchdog timer.
14	WRST	R/W	Watchdog Reset. Set 1: The WDT generates a system reset when the WDT timeout count is reached. Set 0: The WDT will generate an NMI interrupt when the WDT timeout count is reached if the NMIFLAG bit is 0. If the NMIFLAG bit is 1, the WDT will generate a system reset when timeout.
13	RSTFLAG	R/W	Reset Flag. When a watchdog timer reset event occurs, this bit will be set to 1 by hardware. This bit will be cleared by any read from this register or through external reset. This bit is 0 after an external reset or 1 after a watchdog timer reset.
12	NMIFLAG	R/W	NMI Status Flag After the WDT generates an NMI interrupt, this bit will be set to 1 by H/W. This bit will be cleared by any keyed sequence written to this register.
11-8	Rsvd	RO	Reserved

<table>
<tr>
<td>7-0</td>
<td>COUNT</td>
<td>R/W</td>
<td>Timeout Count. The COUNT setting determines the duration of the watchdog timer timeout interval.
a. The duration equation: Duration =($2^{Exponent}$) / (Frequency/2)
b. The Exponent of the COUNT setting:
(bit 7, bit 6, bit 5, bit 4, bit 3, bit 2, bit 1, bit 0) = (Exponent)
(0 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (N/A)
(x , x , x , x, x , x , x , ~~x~~ 1) = (10)
(x , x , x , x, x , x , 1 , 0) = (20)
(x , x , x , x, x , 1 , 0 , 0) = (21)
(x , x , x , x, 1 , 0 , 0 , 0) = (22)
(x , x , x , 1, 0 , 0 , 0 , 0) = (23)
(x , x , 1 , 0, 0 , 0 , 0 , 0) = (24)
(x , 1 , 0 , 0, 0 , 0 , 0 , 0) = (25)
(1 , 0 , 0 , 0, 0 , 0 , 0 , 0) = (26)
c. Watchdog timer duration reference table:
<table>
<tr><th>Frequency\ Exponent</th><th>10</th><th>20</th><th>21</th><th>22</th><th>23</th><th>24</th><th>25</th><th>26</th></tr>
<tr><td>20 MHz</td><td>51 us</td><td>52 ms</td><td>104 ms</td><td>209 ms</td><td>419 ms</td><td>838 ms</td><td>1.67 s</td><td>3.35 s</td></tr>
<tr><td>25 MHz</td><td>40 us</td><td>41 ms</td><td>83 ms</td><td>167 ms</td><td>335 ms</td><td>671 ms</td><td>1.34 s</td><td>2.68 s</td></tr>
<tr><td>33 MHz</td><td>30 us</td><td>31 ms</td><td>62 ms</td><td>125 ms</td><td>251 ms</td><td>503 ms</td><td>1.00 s</td><td>2.01 s</td></tr>
<tr><td>40 MHz</td><td>25 us</td><td>26 ms</td><td>52 ms</td><td>104 ms</td><td>209 ms</td><td>419 ms</td><td>838 ms</td><td>1.67 s</td></tr>
</table>
</td>
</tr>
</table>

~~16.~~17. Asynchronous Serial Port

The R8822 has two asynchronous serial ports, which provide the TXD and RXD pins for the full duplex bi-directional data transfers with handshaking signals CTS_n, ENRX_n, RTS_n and RTR_n. The serial ports support: 9-bit, 8-bit or 7-bit data transfers; odd parities, even parities or no parity; 1 stop bit; error detection; DMA transfers through the serial ports; multi-drop protocol (9-bit) support; double buffers for transmit and receive. The receive/transmit clock is based on the microprocessor clock. The serial ports can be used in power-saved mode, but the transfer rate must be adjusted to correctly reflect the new internal operating frequency. Software can configure the asynchronous serial ports through programming the registers (80h, 82h, 84h, 86h and 88h – for port 0; 10h, 12h, 14h, 16h and18h – for port 1).



Serial Port Block Diagram

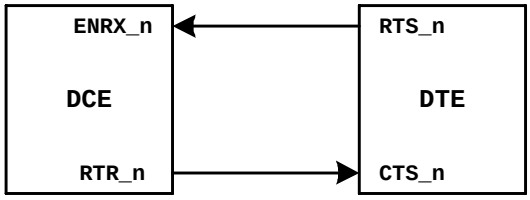
17.1 Serial Port Flow Control

The two serial ports provide two data pins (RXD and TXD) and two flow control signals (RTS_n and RTR_n). Hardware flow control is enabled when the FC bit in the Serial Port Control Register is set. The flow control signals are configured by software to support several different protocols.

17.1.1 DCE/DTE Protocol

The R8822 can function as a DCE (Data Communication Equipment) or a DTE (Data Terminal Equipment). This protocol provides flow control where one serial port is receiving data and the other serial port is sending data. To implement the DCE device, the ENRX bit should be set and the RTS bit should be cleared for the associated serial ports. To implement the DTE device, the ENRX bit should be cleared and the RTS bit should be set for the associated serial ports. The ENRX and RTS bits are found in Register F2h.

The DCE/DTE protocol is asymmetric interface since the DTE device cannot signal the DCE device that it is ready to receive data, and the DCE cannot send the requests to send signals.



RTS_n:Request to send
CTS_n:Clear to send
RTR_n:Ready to receive
ENRX_n:Enable receiver request

DCE/DTE Protocol Connection

The DCE/DTE protocol communication steps:

a. DTE sends data to DCE

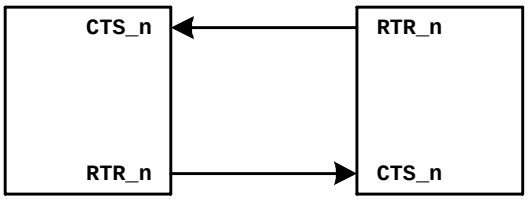
b. The RTS_n signal is asserted by the DTE when data is available.

c. The RTS_n signal interpreted by the DCE device functions as a request to enable its receiver.

d. The DCE asserts the RTR_n signal to response that the DCE is ready to receive data.

17.1.2 CTS/RTR Protocol

The serial ports can be programmed as CTS/RTS protocols by clearing both of the ENRX and RTS bits. This protocol is a symmetric interface, which provides flow control when both of the ports are sending and receiving data.



CTS_n:Clear to send
RTR_n:Ready to receive

CTS/RTR Protocol Connection

17.2 DMA Transfers to/from Serial Ports

DMA transfers to serial ports function as destination-synchronized DMA transfers. A new transfer is requested when the Transmit Holding Register is empty. When a port is configured for DMA transmits, the corresponding transmit interrupt is disabled regardless of the TXIE bit setting. DMA transfers from serial ports function as source-synchronized DMA transfers. A new transfer is requested when the Receive Buffer contains valid data. When a port is configured for DMA receives, the corresponding receive interrupt is disabled regardless of the RXIE bit setting. The DMA request is generated internally when a DMA channel is used for serial port transfers. DRQ0 or DRQ1 are not active when serial port DMA transfers occur. Hardware handshaking may be used in conjunction with serial port DMA transfers.

17.3 Asynchronous Modes

There are 4 mode operations in the asynchronous serial ports.

Mode1: Mode 1 is an 8-bit asynchronous communications mode. Each frame consists of a start bit, eight data bits and a stop bit. When parities are used, the eighth data bit becomes a parity bit.

Mode 2: Mode 2 is used together with Mode 3 for multiprocessor communications over a common serial link. In mode 2, the RX machine will not complete a reception unless the ninth data bit is a one. Any character received with the ninth bit equal to zero is ignored. No flags are set, no interrupts occur and no data are transferred to the Receive Data Register. In mode 3, characters are received regardless of the state of the ninth data bit.

Mode 3: Mode 3 is a 9-bit asynchronous communications mode. Mode 3 is the same as mode 1 except that a frame contains nine data bits. The ninth data bit becomes a parity bit when the parity feature is enabled.

Mode 4: Mode 4 is a 7-bit asynchronous communications mode. Each frame consists of a start bit, seven data bits and a stop bit. Parity bits are not available in mode 4.

Register Offset: 80h

Register Name: Serial Port 0 Control Register

Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA			RISE	BRK	TB8	FC	TXIE	RXIE	TMODE	RMODE	EVN	PE	MODE		

Bit	Name	Attribute	Description
15-13	DMA	R/W	DMA Control Field. With DMA transfers listed as follows, these bits can be configured for serial port use. **DMA control bits (bit 15, bit 14, bit 13) --- Receive --- Transmit** (0, 0, 0) --- No DMA --- No DMA (0, 0, 1) --- DMA 0 --- DMA 1 (0, 1, 0) --- DMA 1 --- DMA 0 (0, 1, 1) --- N/A --- N/A (1, 0, 0) --- DMA 0 --- No DMA (1, 0, 1) --- DMA 1 --- No DMA (1, 1, 0) --- No DMA --- DMA 0 (1, 1, 1) --- No DMA --- DMA 1
12	RSIE	R/W	Receive Status Interrupt Enable. It will generate an interrupt when an error is detected (frame error, parity error or overrun error) or a break interrupt bit is received in serial port 0. Set 1: Enable the serial port 0 to generate an interrupt request.
11	BRK	R/W	Send Break. Set 1: The TXD pin is always driven low. Long Break: The TXD pin is driven low for greater than (2M+3) bit times; Short break: The TXD pin is driven low for greater than M bit times; * M= start bit + data bit number + parity bit + stop bit
10	TB8	R/W	Transmit Bit 8. This bit is transmitted as the ninth data bit in mode 2 and mode 3. This bit is cleared after every transmission.
9	FC	R/W	Flow Control Enable. Set 1: Enable the hardware flow control for serial port 0. Set 0: Disable the hardware flow control for serial port 0.
8	TXIE	R/W	Transmitter Ready Interrupt Enable. When the Transmit Holding Register is empty (the THRE bit in the Status Register is set), an interrupt will occur. Set 1: Enable the Interrupt. Set 0: Disable the interrupt.
7	RXIE	R/W	Receive Data Ready Interrupt Enable. When the receive buffer contains valid data (the RDR bit in Status Register is set), an interrupt will be generated. Set 1: Enable the Interrupt. Set 0: Disable the interrupt.
6	TMODE	R/W	Transmit Mode. Set 1: Enable the TX machines. Set 0: Disable the TX machines.
5	RMODE	R/W	Receive Mode. Set 1: Enable the RX machines. Set 0: Disable the RX machines.
4	EVN	R/W	Even Parity. This bit is valid only when the PE bit is set. Set 1: The even parity checking is enforced (even number of 1s in frame).

			Set 0: Odd parity checking is enforced (odd number of 1s in frame).
3	PE	R/W	Parity Enable. Set 1: Enable the parity checking. Set 0: Disable the parity checking.
2-0	MODE	R/W	Modes of Operations.

(bit2, bit1, bit0)	MODE	Data Bits	Parity Bits	Stop Bits
(0 , 0 , 1)	Mode 1	7 or 8	1 or 0	1
(0 , 1 , 0)	Mode 2	9	N/A	1
(0 , 1 , 1)	Mode 3	8 or 9	1 or 0	1
(1 , 0 , 0)	Mode 4	7	N/A	1

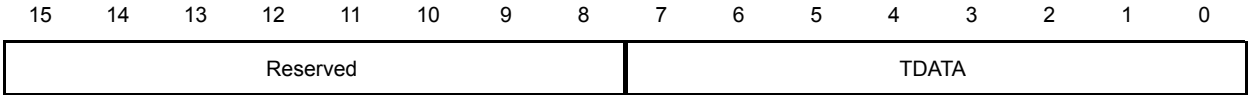
Register Offset: 82h
Register Name: Serial Port 0 Status Register
Reset Value : ----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					BRK1	BRK0	RB8	RDR	THRE	FER	OER	PER	TEMT	HS0	Rsvd

The Serial Port 0 Status Register provides information about the current status of Serial Port 0.

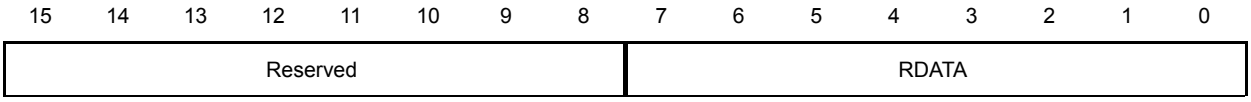
Bit	Name	Attribute	Description
15-11	Rsvd	RO	Reserved.
10	BRK1	R/W	Long Break Detected. This bit should be reset by software. When a long break is detected, this bit will be set high.
9	BRK0	R/W	Short Break Detected. This bit should be reset by software. When a short break is detected, this bit will be set high.
8	RB8	R/W	Received Bit 8. This bit should be reset by software. This bit contains the ninth data bit received in mode 2 and mode 3.
7	RDR	RO	Received Data Ready. Read only. The Received Data Register contains valid data. This bit is set high and can only be reset through reading the Serial Port 0 Receive Register.
6	THRE	RO	Transmit Holding Register Empty. Read only. When the Transmit Hold Register is ready to accept data, this bit will be set. This bit will be reset when data is written to the Transmit Hold Register.
5	FER	R/W	Framing Error detected. This bit should be reset by software. This bit is set when a framing error is detected.
4	OER	R/W	Overrun Error Detected. This bit should be reset by software. This bit is set when an overrun error is detected.
3	PER	R/W	Parity Error Detected. This bit should be reset by software. This bit is set when a parity error (for mode 1 and mode 3) is detected.
2	TEMT	RO	Transmitter Empty. This bit is read only. When the Transmit Shift Register is empty, this bit will be set.
1	HS0	RO	Handshake Signal 0. This bit is read only. This bit reflects the inverted value of the external CTS0_n pin.
0	Rsvd	RO	Reserved.

Register Offset: 84h
Register Name: Serial Port 0 Transmit Register
Reset Value : -----



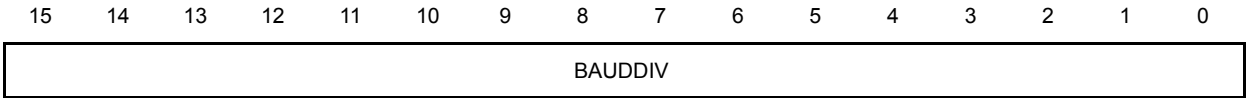
Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	TDATA	RO	Transmit Data. This register is written by software with data transmitted on Serial Port 0.

Register Offset: 86h
Register Name: Serial Port 0 Receive Register
Reset Value : -----



Bit	Name	Attribute	Description
15-8	Rsvd	RO	Reserved.
7-0	RDATA	RO	Receive DATA. In order to avoid invalid data being read, the RDR bit (82h.4) should be read as 1 before this register is read.

Register Offset: 88h
Register Name: Serial Port 0 Baud Rate Divisor Register
Reset Value : 0000h



Bit	Name	Attribute	Description
15-0	BAUDDIV	R/W	Baud Rate Divisor. The general formula for baud rate divisor is **Baud Rate = Microprocessor Clock / (16 x BAUDDIV)**. For example, if the microprocessor clock is 22.1184MHz and the BAUDDIV=12 (decimal), the baud rate of the serial port will be 115.2K.

Register Offset: 10h
Register Name: Serial Port 1 Control Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA			RISE	BRK	TB8	FC	TXIE	RXIE	TMODE	RMODE	EVN	PE	MODE		

These bit definitions are the same as those of Register 80h.

Register Offset: 12h
Register Name: Serial Port 1 Status Register
Reset Value : ----------

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					BRK1	BRK0	RB8	RDR	THRE	FER	OER	PER	TEMT	HS0	Rsvd

These bit definitions are the same as those of Register 82h.

Register Offset: 14h
Register Name: Serial Port 1 Transmit Register
Reset Value : ----------

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TDATA							

These bit definitions are the same as those of Register 84h.

Register Offset: 16h
Register Name: Serial Port 1 Receive Register
Reset Value : ----------

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								RDATA							

These bit definitions are the same as those of Register 86h.

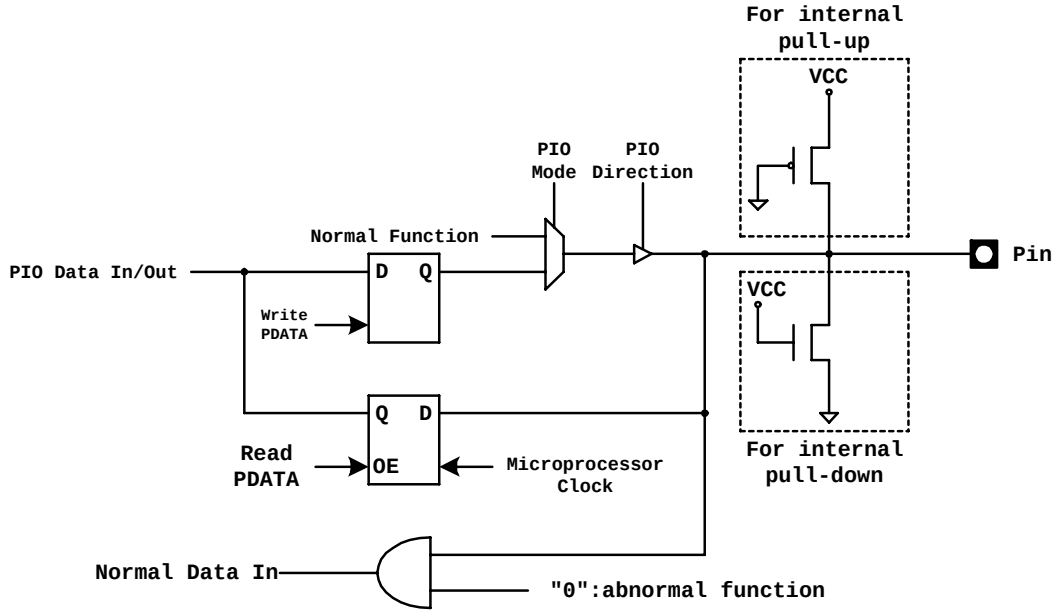
Register Offset: 18h
Register Name: Serial Port 1 Baud Rate Divisor Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAUDDIV															

These bit definitions are the same as those of Register 88h.

~~17.~~18. PIO Unit

The R8822 provides 32 programmable I/O signals, which are multi-function pins with other normal function signals. Through programming Registers 7Ah, 78h, 76h, 74h, 72h and 70h, software can configure these multi-function pins as PIOs or normal functions.



PIO Pin Operation Diagram

~~17.1~~18.1 PIO Multi-Function Pins

PIO No.	Pin No. (PQFP)	Multi Function	Reset status/PIO internal resistor
0	72	TMRIN1	Input with 10k pull-up
1	73	TMROUT1	Input with 10k pull-down
2	59	PCS6_n/A2	Input with 10k pull-up
3	60	PCS5_n/A1	Input with 10k pull-up
4	48	DT/R_n	Normal operation/Input with 10k pull-up
5	49	DEN_n	Normal operation/Input with 10k pull-up
6	46	SRDY	Normal operation/Input with 10k pull-down
7	22	A17/MA8	Normal operation/Input with 10k pull-up
8	20	A18	Normal operation/Input with 10k pull-up
9	19	A19	Normal operation/Input with 10k pull-up
10	74	TMROUT0	Input with 10k pull-down
11	75	TMRIN0	Input with 10k pull-up
12	77	DRQ0/INT5	Input with 10k pull-up
13	76	DRQ1/INT6	Input with 10k pull-up
14	50	MCS0_n	Input with 10k pull-up
15	51	MCS1_n/UCAS_n	Input with 10k pull-up
16	66	PCS0_n	Input with 10k pull-up
17	65	PCS1_n	Input with 10k pull-up
18	63	PCS2_n/CTS1_n/ENRX1_n	Input with 10k pull-up

19	62	PCS3_n/RTS1_n/RTR1_n	Input with 10k pull-up
20	3	RTS0_n/RTR0_n	Input with 10k pull-up
21	100	CTS0_n/ENRX0_n	Input with 10k pull-up
22	2	TXD0	Input with 10k pull-down
23	1	RXD0	Input with 10k pull-down
24	68	MCS2_n/LCAS_n	Input with 10k pull-up
25	69	MCS3_n/RAS1_n	Input with 10k pull-up
26	97	UZI_n	Input with 10k pull-up
27	98	TXD1	Input with 10k pull-up
28	99	RXD1	Input with 10k pull-up
29	96	S6/CLKDIV2_n	Input with 10k pull-up
30	52	INT4	Input with 10k pull-up
31	54	INT2	Input with 10k pull-up

Register Offset: 7Ah
Register Name: PIO Data 1 Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA [31:16]															

Bit	Name	Attribute	Description
15-0	PDATA [31:16]	R/W	PIO Data bits. These bits PDATA[31:16] are mapped to PIO[31:16], which indicate to the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 78h
Register Name: PIO Direction 1 Register
Reset Value : FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR [31:16]															

Bit	Name	Attribute	Description
15-0	PDIR[31:16]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input. Set 0: Configure the PIO pin as an output or normal function pin.

Register Offset: 76h
Register Name: PIO Mode 1 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE [31:16]															

Bit	Name	Attribute	Description
15-0	PMODE [31:16]	R/W	PIO Mode bits. PIO pin definitions are configured by the combination of PIO mode and PIO direction. The PIO pins are programmed individually. The definitions (PIO mode, PIO direction) for PIO pin functions: (0 , 0) – Normal operation , (0 , 1) – PIO input with pull-up/pull-down (1 , 0) – PIO output , (1 , 1) -- PIO input without pull-up/pull-down

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Register Offset: 74h
Register Name: PIO Data 0 Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDATA [15: 0]															

Bit	Name	Attribute	Description
15-0	PDATA [15:0]	R/W	PIO Data bits. These bits PDATA[15:0] are mapped to PIO[15:0], which indicate to the driven level when the PIO pin is as an output or reflect the external level when the PIO pin is as an input.

Register Offset: 72h
Register Name: PIO Direction 0 Register
Reset Value : FC0Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIR [15:0]															

Bit	Name	Attribute	Description
15-0	PDIR[15:0]	R/W	PIO Direction Register. Set 1: Configure the PIO pin as an input. Set 0: Configure the PIO pin as an output or normal function pin.

Register Offset: 70h
Register Name: PIO Mode 0 Register
Reset Value : 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PMODE [15:0]															

Bit	Name	Attribute	Description
15-0	PMODE[15:0]	R/W	PIO Mode bits.

19. DRAM Controller

The R8822 supports 16-bit EDO or FP DRAM control interface. The supporting types are 256K*16,128K*16, 64K*16 or 32K*16. The DRAM control pins are multiplexed pins, which have been described in the Pin Description Chapter. The Basic System Application Block Diagram shows the connection between the microcontroller and DRAM. The DRAM controller supports two banks and dual CAS_n signals (high byte signal UCAS_n and low byte signal LCAS_n operating modes) accesses. When bit 6 of LMCS (A2h) register is set to 1, bank 0 will be enabled and all the bit definitions of A2h are for bank 0 of the DRAM controller. When bit 6 of UMCS (A0h) is set to 1, bank 1 is enabled and all bit definitions of A0h are for bank 1 of the DRAM controller.

The memory block size of DRAM is programmable. The memory space of bank 0 is from 00000h to 7FFFFh. Users can program register A2h (LMCS) to select 64K-, 128K-, 256K- or 512K-byte memory block size. The memory space of bank 1 is from 80000h to FFFFFh. Users can configure register A0h (UMCS) to select 64K-, 128K-, 256K- or 512K-byte memory block size.

The Address Mapping of MA8 – MA0 & Row, Column Signals:

DRAM Address	Row Address Mapping	Column Address Mapping
MA0(A1)	A1	A2
MA1(A3)	A3	A4
MA2(A5)	A5	A6
MA3(A7)	A7	A8
MA4(A9)	A9	A10
MA5(A11)	A11	A12
MA6(A13)	A13	A14
MA7(A15)	A15	A16
MA8(A17)	A17	A18

BANK 0	RAS0_n (Pin 58)	UCAS_n (Pin 51)	LCAS_n (Pin 68)	WE_n (Pin 5)	OE_n (Pin 6)
BANK 1	RAS1_n (Pin 69)	UCAS_n (Pin 51)	LCAS_n (Pin 68)	WE_n (Pin 5)	OE_n (Pin 6)

*** The pin numbers are for PQFP configuration ***

19.1 Programmable Read/Write Cycle Time

The DRAM Controller read/write cycle depends on the external wait-state signal (ARDY or SRDY) and bit 0 and bit 1 of registers A0h and A2h. The default wait-state of bank 1 is 3 wait-states. The wait-state bits for bank 0 should be programmed after the CPU is reset.

19.2 Programmable Refresh Control

The DRAM controller provides self-refresh or CAS_n before RAS_n refresh control. The hardware will auto-stop the self-refresh operation when the controller accesses the DRAM data when the DRAM is in self-refresh mode. During a refresh cycle, the AD bus will drive the address to FFFFFh and the UCS_n signal won't be asserted. The CPU will enter the idle state during a refresh cycle and be held for 7 clock cycles. If two banks of DRAM are being used in a system, both banks will be refreshed at the same time.

The reload counter (E2h) should be set to more than 12h. Users should base on the system clock to configure the reload value. The normal refresh rate on a DRAM is 15.6us. The refresh counter will be started when the EN bit (bit 15 of E4h) is enabled.

Wait States & Refresh Counter Values for Reference:

System clock	DRAM Speed	Wait States	Refresh Cycle clocks	Refresh Reload Counter Value
25 MHz	70ns	0	7	186h
33MHz	70ns	1	7	203h
	60ns	0	7	203h
40MHz	70ns	2	7	270h
	60ns	1	7	270h
	50ns	0	7	270h
	40ns	0	7	270h

Register Offset: E2h
Register Name: Refresh Reload Value Counter Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RC[14:0]														

Bit	Name	Attribute	Description
15	Rsvd	RO	Reserved
14-0	RC[14:0]	R/W	Refresh Counter Reload Values. The counter value should be set to more than 12h.

Register Offset: E4h
Register Name: Refresh Counter Register
Reset Value : -----

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	T[14:0]														

Bit	Name	Attribute	Description
15	EN	R/W	Enable RCU. Set 1: Enable the refresh counter unit This bit will be cleared to 0 after hardware reset.
14-0	T[14:0]	RO	Refresh Count. Read-only bits. These bits present the value of the down counter which triggers refresh requests.

20. DC Electrical Characteristics

20.1 Absolute Maximum Rating

Symbol	Rating	Commercial	Unit	Note
V_{Term}	Terminal Voltage with Respect to GND	-0.5~V_{CC}+0.5	V	
T_A	Ambient Temperature	0~+70	°C	

20.2 Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5	5.25	V
GND	Ground	0	0	0	V
Vih	Input High Voltage (***Note 1***)	2.0	---	Vcc+0.5	V
Vih1	Input High Voltage (RST_n)	3	---	Vcc+0.5	V
Vih2	Input High Voltage (X1)	3	---	Vcc+0.5	V
Vil	Input Low voltage	-0.5	0	0.8	V

Note 1: *The RST_n and X1 pins are not included.*

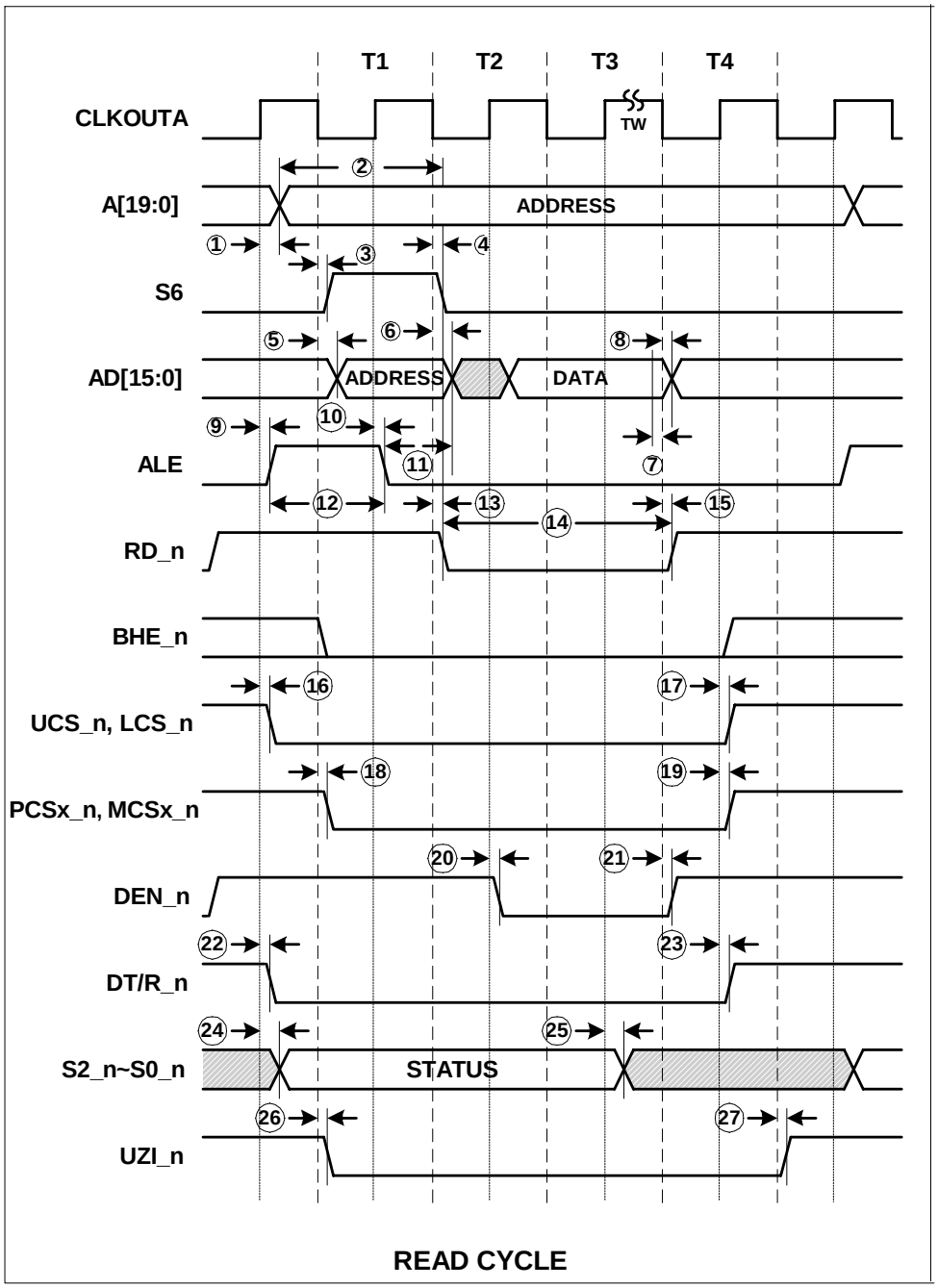
20.3 DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit
Ili	Input Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
Ili (with 10K pull R)	Input Leakage Current with Pull_R 10K enable	Vcc=Vmax Vin=GND to Vmax	-400	400	uA
Ili (with 50K pull R)	Input Leakage Current with Pull_R 50K	Vcc=Vmax Vin=GND to Vmax	-120	120	uA
Ilo	Output Leakage Current	Vcc=Vmax Vin=GND to Vmax	-10	10	uA
VOL	Output Low Voltage	Iol=6mA, Vcc=Vmin.	---	0.4	V
VOH	Output High Voltage	Ioh=-6mA, Vcc=Vmin.	2.4	---	V
Icc	Max Operating Current	Vcc=5.25V 40MHz	---	180	mA

Note 2: *Vmax=5.25V Vmin=4.75V*

Symbol	Parameter	Min.	Max.	Unit	Note
F_{Max}	Max operation clock frequency of commercial	---	40	MHz	$V_{CC} \pm 5\%$

21. AC Electrical Characteristics

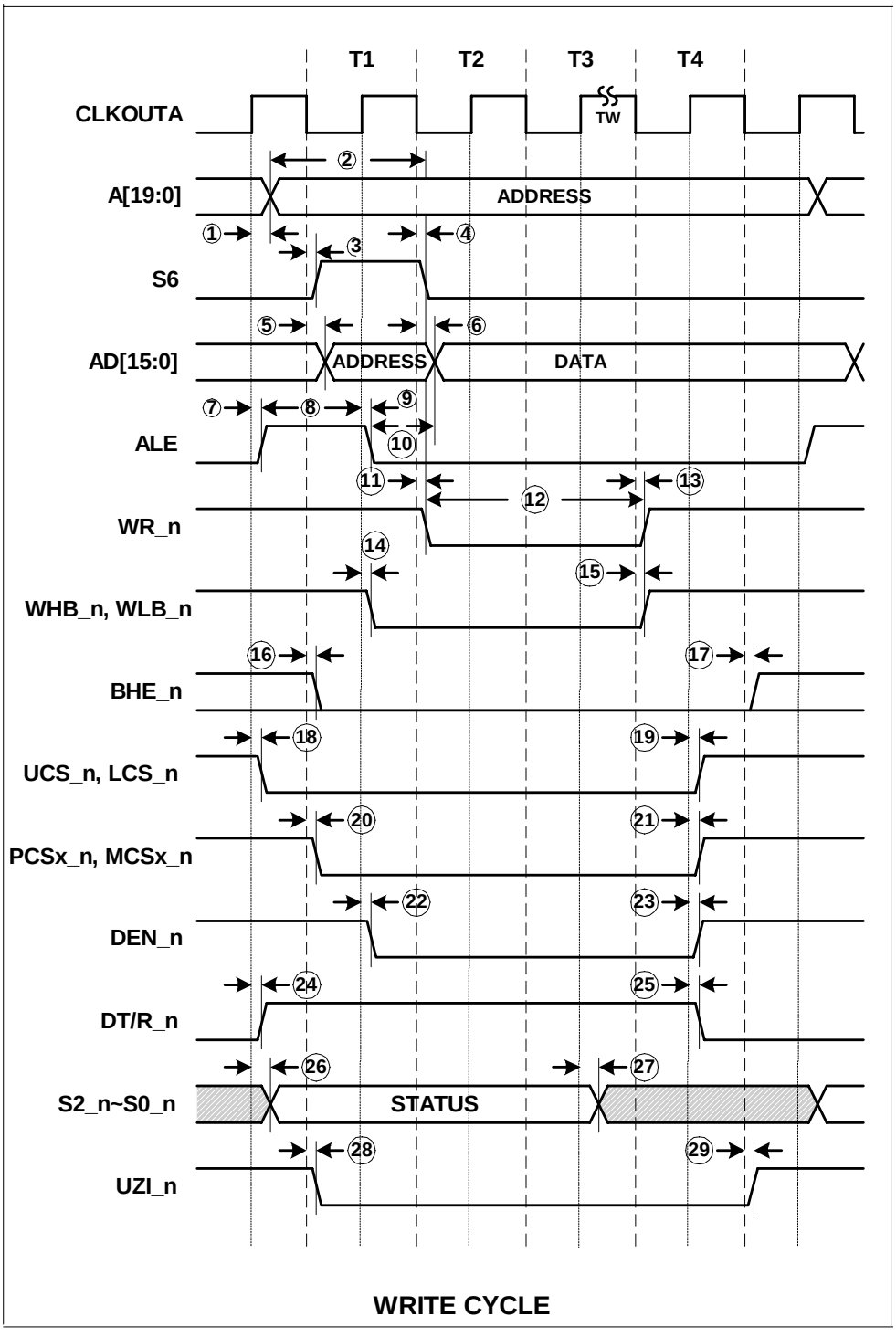


No.	Description	Min.	Max.	Unit
1	CLKOUTA high to A Address valid	0	12	ns
2	A address valid to RD_n low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address valid delay	0	12	ns
6	Address hold	0	12	ns
7	Data in setup	5		ns
8	Data in hold	2		ns
9	ALE active delay	0	12	ns
10	ALE inactive delay	0	12	ns
11	Address valid after ALE inactive	T/2-5		ns
12	ALE width	T-5		ns
13	RD_n active delay	0	12	ns
14	RD_n pulse width	2T-10		ns
15	RD_n inactive delay	0	12	ns
16	CLKOUTA high to LCS_n/UCS_n valid	0	15	ns
17	UCS_n/LCS_n inactive delay	0	15	ns
18	PCS_n/MCS_n active delay	0	15	ns
19	PCS_n/MCS_n inactive delay	0	15	ns
20	DEN_n active delay	0	15	ns
21	DEN_n inactive delay	0	15	ns
22	DT/R_n active delay	0	15	ns
23	DT/R_n inactive delay	0	15	ns
24	Status active delay	0	15	ns
25	Status inactive delay	0	15	ns
26	UZI_n active delay	0	15	ns
27	UZI_n inactive delay	0	15	ns

1. T means a clock period time

2. All timing parameters are measured at 1.5V with 50 pF loading on CLKOUTA

. All output test conditions are with CL=50 pF


T1
T2
T3
T4
CLKOUTA
TW
A[19:0]
ADDRESS
S6
AD[15:0]
ADDRESS
DATA
ALE
WR_n
WHB_n, WLB_n
BHE_n
UCS_n, LCS_n
PCSx_n, MCSx_n
DEN_n
DT/R_n
S2_n~S0_n
STATUS
UZI_n
1
2
3
4
5
6
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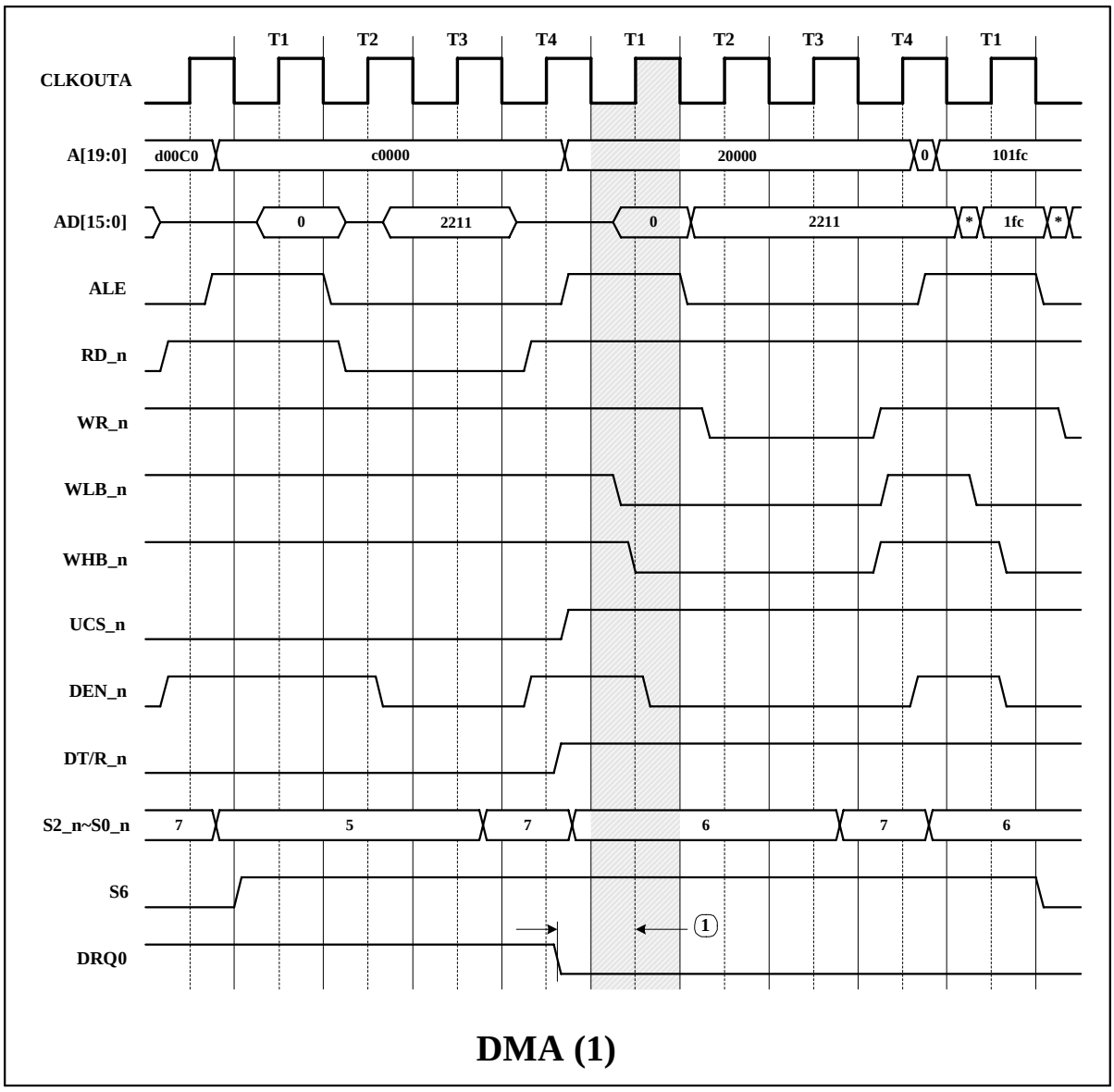
WRITE CYCLE

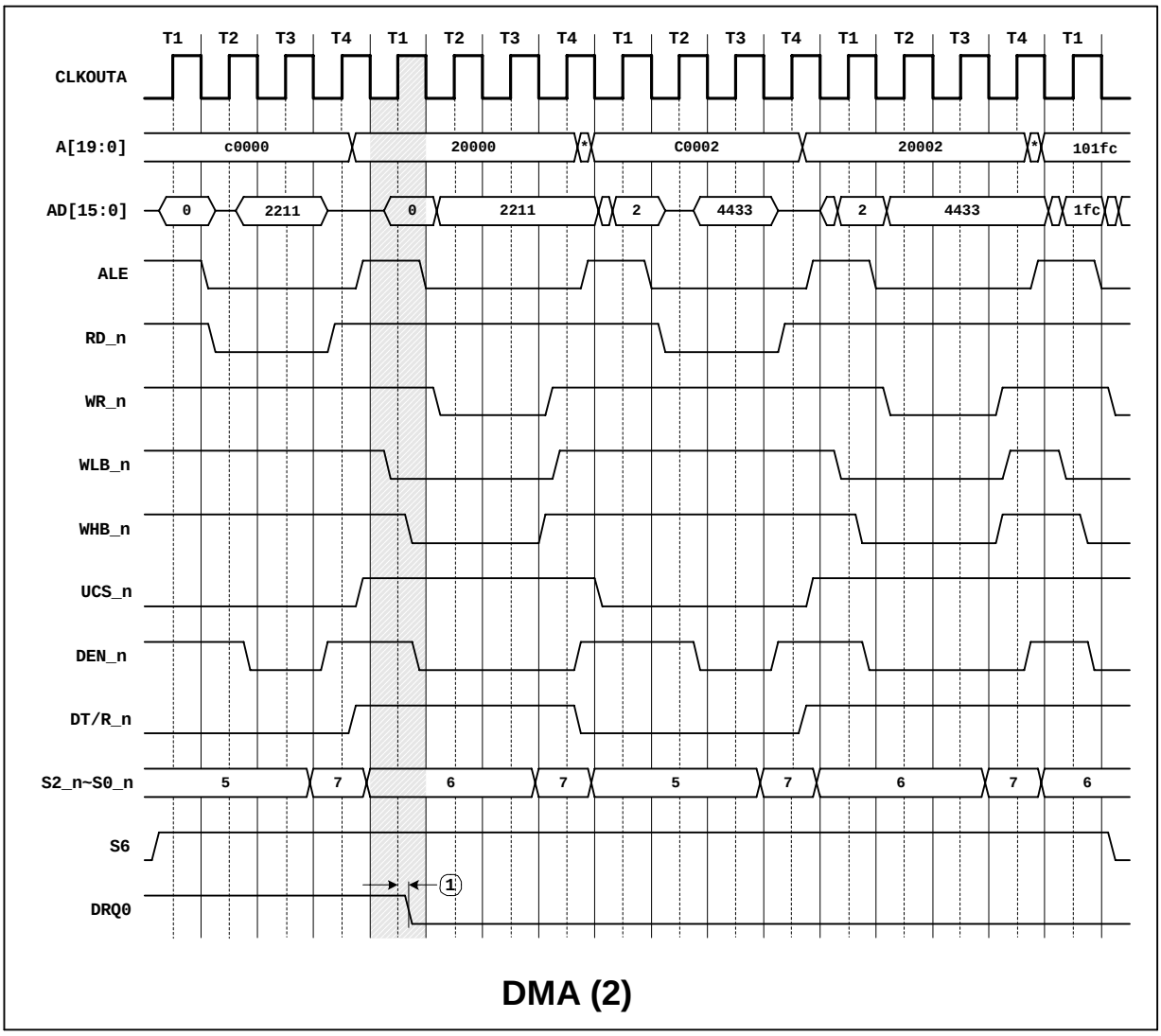
No.	Description	Min.	Max.	Unit
1	CLKOUTA high to A Address valid	0	12	ns
2	A address valid to WR_n low	1.5T-9		ns
3	S6 active delay	0	15	ns
4	S6 inactive delay	0	15	ns
5	AD address valid delay	0	12	ns
6	Address hold			ns
7	ALE active delay	0	12	ns
8	ALE width	T-10		ns
9	ALE inactive delay	0	12	ns
10	Address valid after ALE inactive	1/2T-5		ns
11	WR_n active delay	0	12	ns
12	WR_n pulse width	2T-10		ns
13	WR_n inactive delay	0	12	ns
14	WHB_n/WLB_n active delay	0	15	ns
15	WHB_n/WLB_n inactive delay	0	15	ns
16	BHE_n active delay	0	15	ns
17	BHE_n inactive delay	0	15	ns
18	CLKOUTA high to UCS_n/LCS_n valid	0	15	ns
19	UCS_n/LCS_n inactive delay	0	15	ns
20	PCS_n/MCS_n active delay	0	15	ns
21	PCS_n/MCS_n inactive delay	0	15	ns
22	DEN_n active delay	0	15	ns
23	DEN_n inactive delay	0	15	ns
24	DT/R_n active delay	0	15	ns
25	DT/R_n inactive delay	0	15	ns
26	Status active delay	0	15	ns
27	Status inactive delay	0	15	ns
28	UZI_n active delay	0	15	ns
29	UZI_n inactive delay	0	15	ns



DMA (1)

* The source-synchronized transfer is not followed immediately by another DMA transfer.

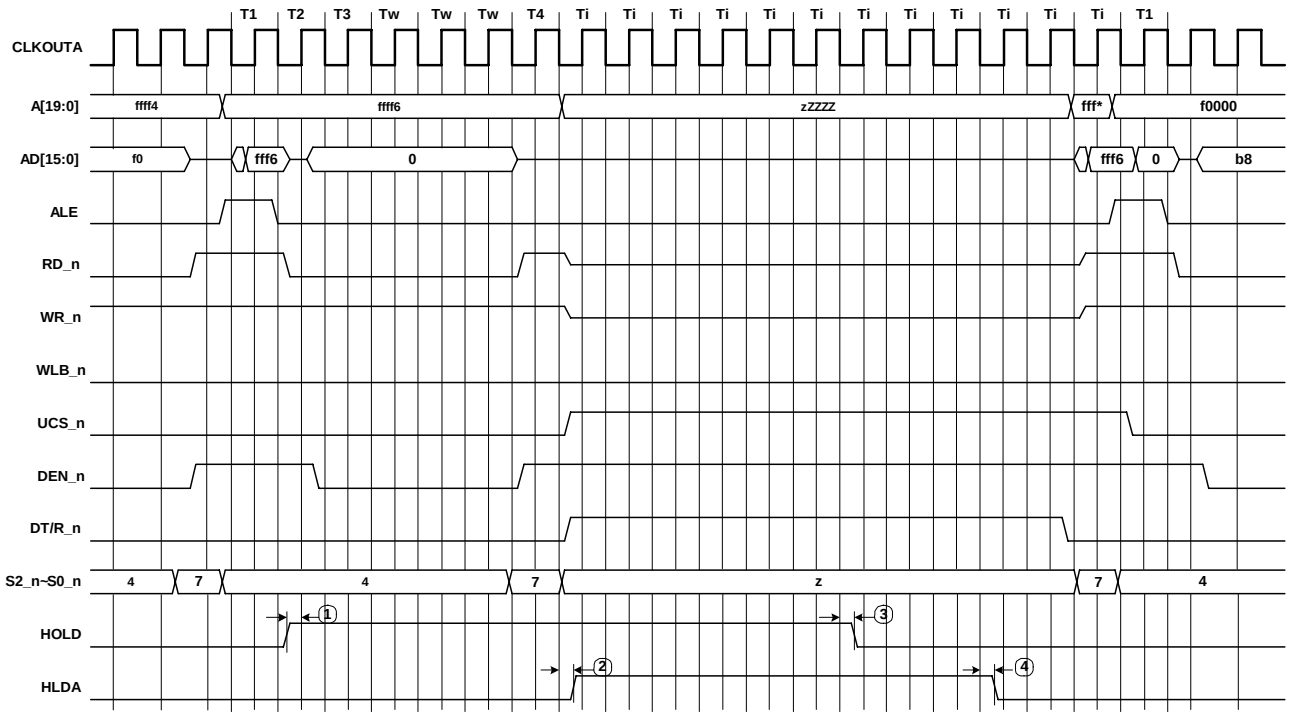
No.	Description	Min.	Max.	Unit
1	DRQ is confirmed time	5	1T-5	ns



DMA (2)

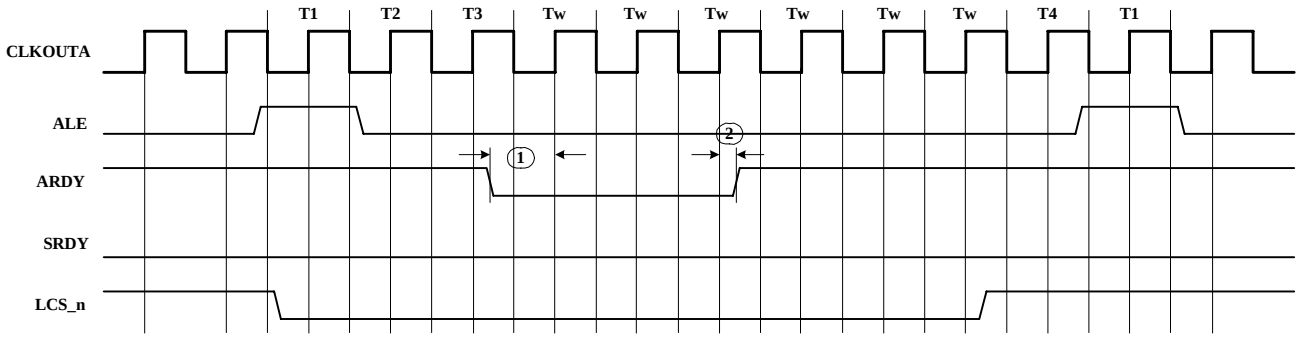
***** The source-synchronized transfer is followed immediately by another DMA transfer.

No.	Description	Min.	Max.	Unit
1	DRQ is confirmed time	2	0	ns



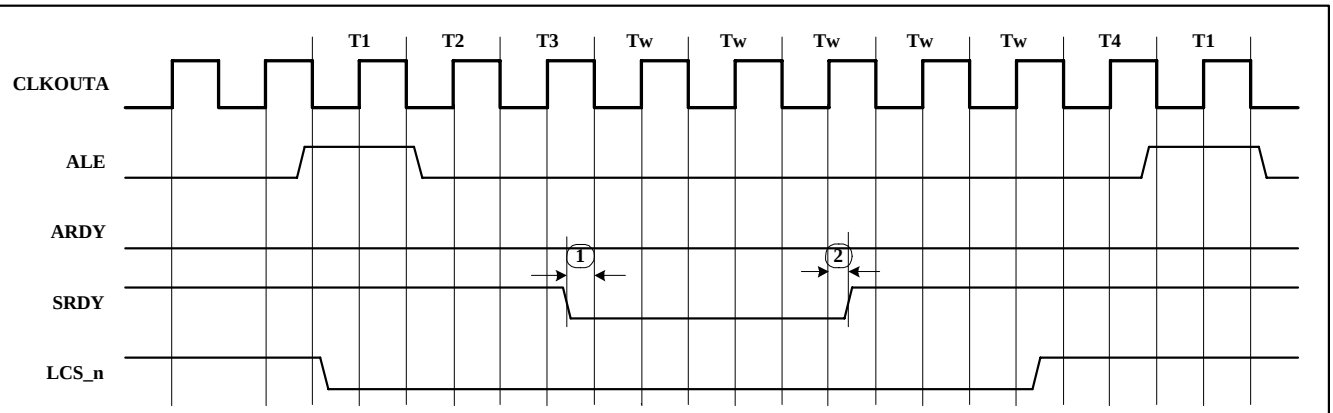
HOLD/HLDA Timing

No.	Description	Min.	Max.	Unit
1	HOLD setup time	5	0	ns
2	HLDA rising valid delay	0	15	ns
3	HOLD hold time	2	0	ns
4	HLDA falling valid delay	0	15	ns



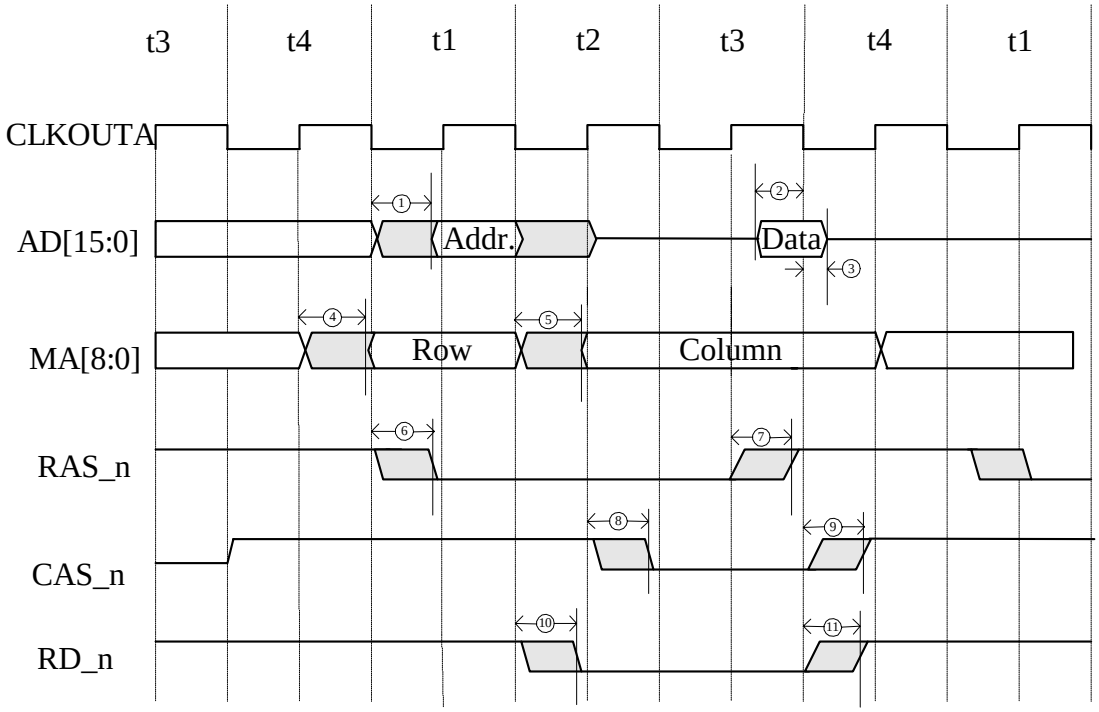
ARDY Timing

No.	Description	Min.	Max.	Unit
1	ARDY resolution transition setup time	5	0	ns
2	ARDY active hold time	5	0	ns



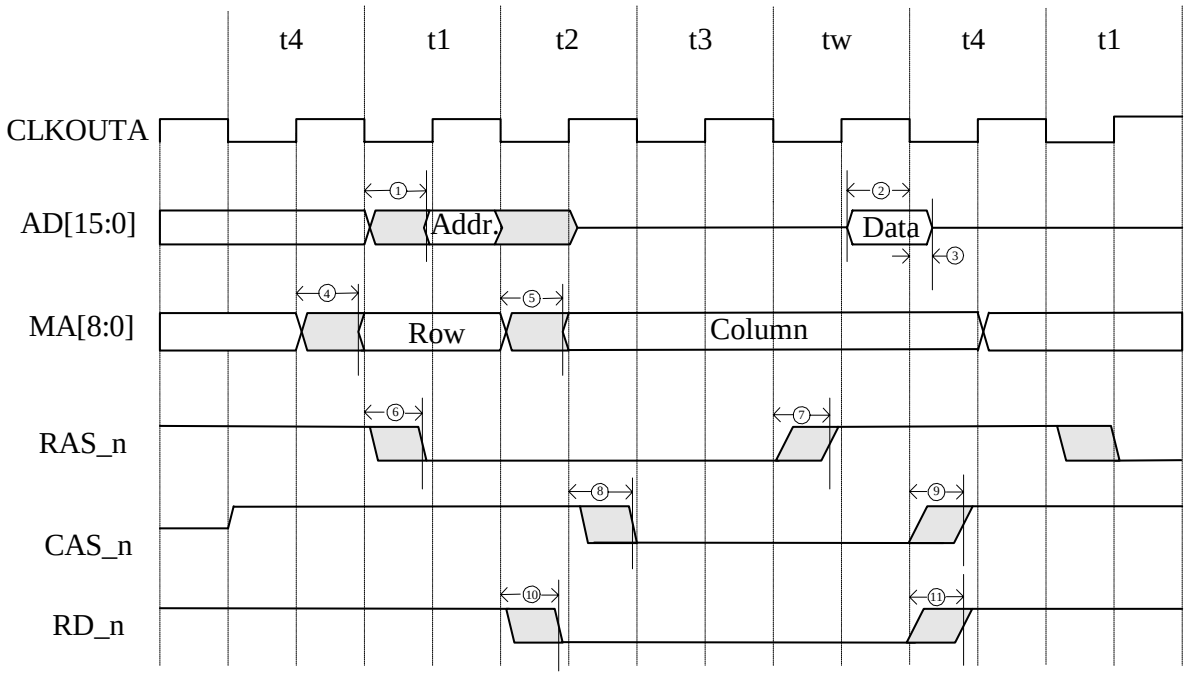
SRDY Timing

No.	Description	Min.	Max.	Unit
1	SRDY transition setup time	5	0	ns
2	SRDY transition hold time	5	0	ns



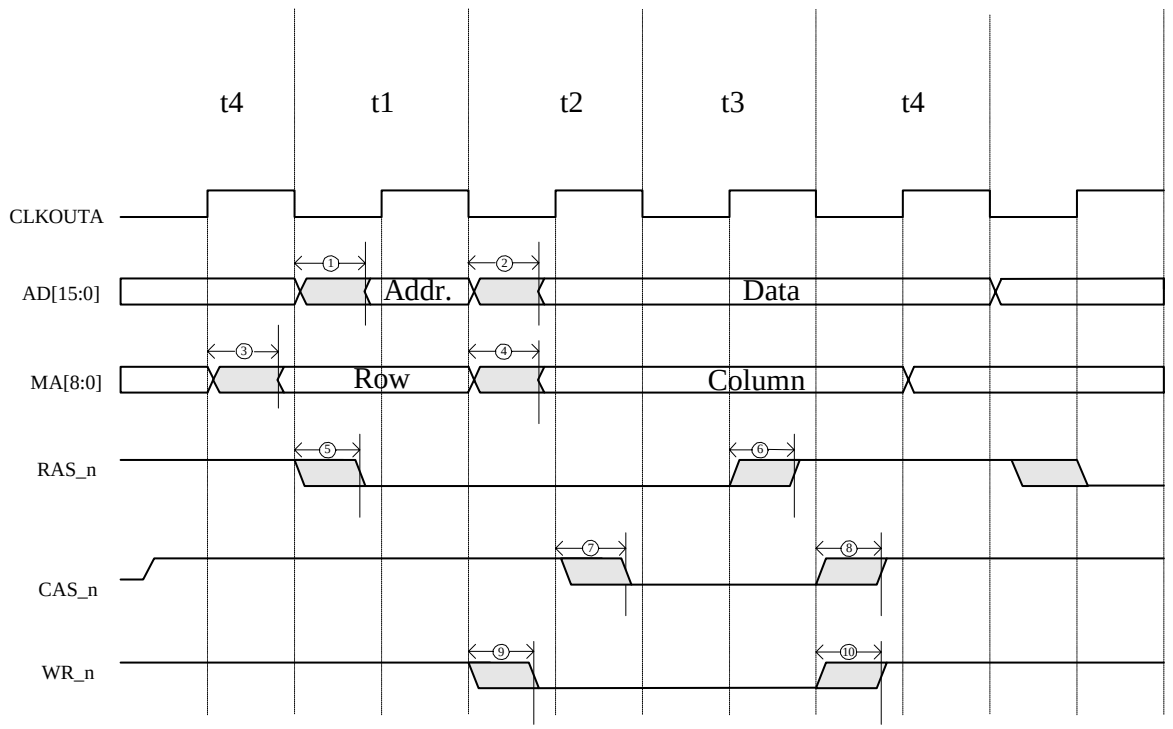
DRAM Read Cycle with No Wait States

No.	Description	Min.	Max.	Unit
1	CLKOUTA low to A Address valid	0	12	ns
2	Data setup time	5		ns
3	Data hold time	2		ns
4	CLKOUTA high to Row address valid	0	12	ns
5	CLKOUTA low to Column address valid	0	12	ns
6	CLKOUTA low to RAS_n active	3	12	ns
7	CLKOUTA high to RAS_n inactive	3	12	ns
8	CLKOUTA high to CAS_n active	3	12	ns
9	CLKOUTA low to CAS_n inactive	3	12	ns
10	CLKOUTA low to RD_n active	0	12	ns
11	CLKOUTA low to RD_n inactive	0	12	ns



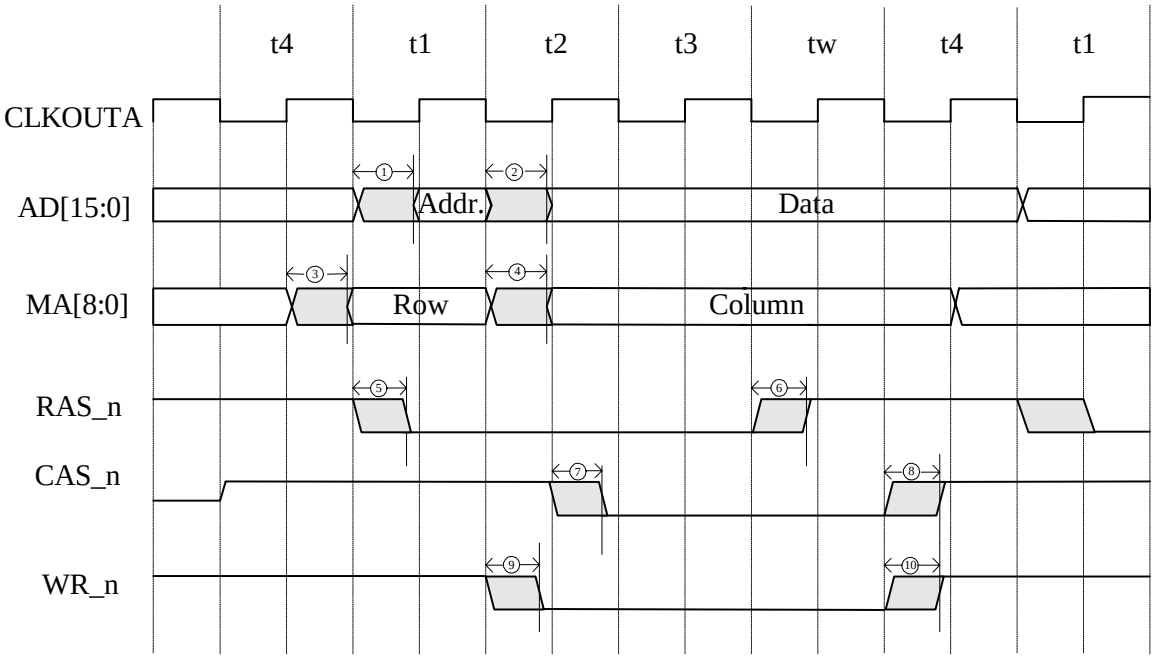
DRAM Read Cycle with Wait-States

No.	Description	Min.	Max.	Unit
1	CLKOUTA low to A Address valid	0	12	ns
2	Data setup time	5		ns
3	Data hold time	2		ns
4	CLKOUTA high to Row address valid	0	12	ns
5	CLKOUTA low to Column address valid	0	12	ns
6	CLKOUTA low to RAS_n active	3	12	ns
7	CLKOUTA high to RAS_n inactive	3	12	ns
8	CLKOUTA high to CAS_n active	3	12	ns
9	CLKOUTA low to CAS_n inactive	3	12	ns
10	CLKOUTA low to RD_n active	0	12	ns
11	CLKOUTA low to RD_n inactive	0		ns



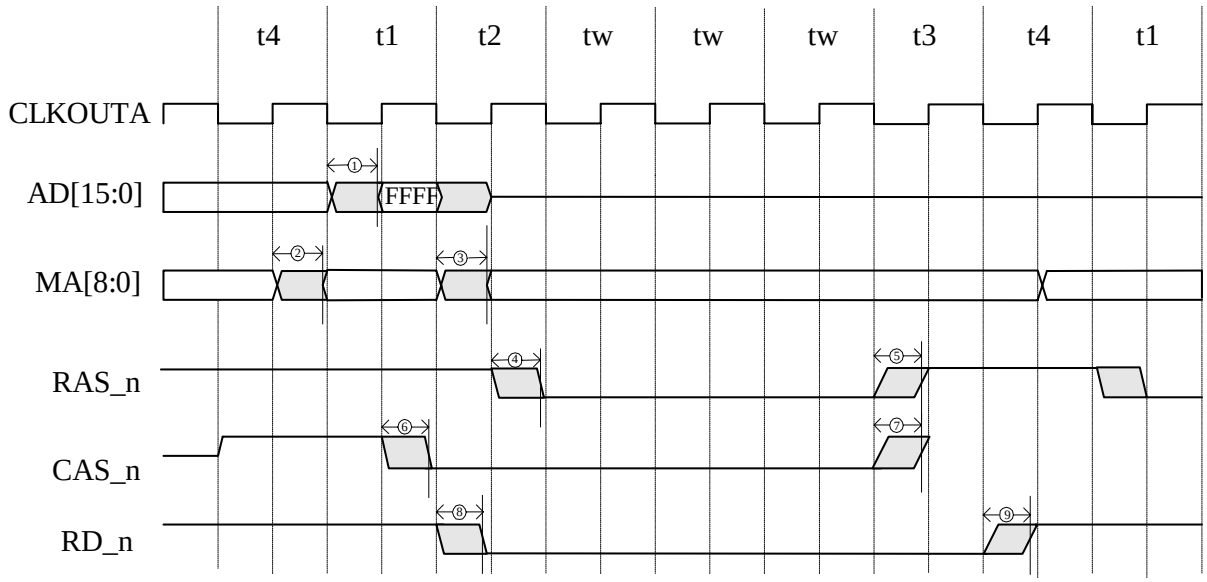
DRAM Write Cycle with No Wait-States

No.	Description	Min.	Max.	Unit
1	CLKOUTA low to A Address valid	0	12	ns
2	CLKOUTA low to A Data valid	0	12	ns
3	CLKOUTA high to Row address valid	0	12	ns
4	CLKOUTA low to Column address valid	0	12	ns
5	CLKOUTA low to RAS_n active	3	12	ns
6	CLKOUTA high to RAS_n inactive	3	12	ns
7	CLKOUTA high to CAS_n active	3	12	ns
8	CLKOUTA low to CAS_n inactive	3	12	ns
9	CLKOUTA low to WR_n active	0	12	ns
10	CLKOUTA low to WR_n inactive	0	12	ns



DRAM Write Cycle with Wait-States

No.	Description	Min.	Max.	Unit
1	CLKOUTA low to A Address valid	0	12	ns
2	CLKOUTA low to A Data valid	0	12	ns
3	CLKOUTA high to Row address valid	0	12	ns
4	CLKOUTA low to Column address valid	0	12	ns
5	CLKOUTA low to RAS_n active	3	12	ns
6	CLKOUTA high to RAS_n inactive	3	12	ns
7	CLKOUTA high to CAS_n active	3	12	ns
8	CLKOUTA low to CAS_n inactive	3	12	ns
9	CLKOUTA low to WR_n active	0	12	ns
10	CLKOUTA low to WR_n inactive	0	12	ns



DRAM Refresh Cycle

No.	Description	Min.	Max.	Unit
1	CLKOUTA high to Data drive FFFF	0	12	ns
2	CLKOUTA high to Row address valid	0	12	ns
3	CLKOUTA low to Column address valid	0	12	ns
4	CLKOUTA high to RAS_n active	3	12	ns
5	CLKOUTA low to RAS_n inactive	3	12	ns
6	CLKOUTA high to CAS_n active	3	12	ns
7	CLKOUTA low to CAS_n inactive	3	12	ns
8	CLKOUTA low to RD_n active	0	12	ns
9	CLKOUTA low to RD_n inactive	0	12	ns

22. Thermal Characteristics

θ_{JA}: thermal resistance from device junction to ambient temperature

P: operation power

T_A: maximum ambient temperature in operation mode

$T_A=T_J-(P\times\theta_{JA})$

Package/Board	Air Flow (m/s)	θ_{JA}
PQFP/2-Layer	0	48.8
	1	44.9
	2	42.7
	3	41.9
LQFP/2-Layer	0	53.6
	1	48.9
	2	45.5
	3	44.5
PQFP/4-Layer	0	38.9
	1	35.7
	2	33.8
	3	33.3
LQFP/4-Layer	0	42.6
	1	38.0
	2	36.1
	3	35.3

Unit: °C/Watt

Recommended Storage Temperature: –65°C to +125°C

Note: *The IC should be mounted on PCB within 7 days after the dry pack is opened. If the IC is out of dry pack more than 7 days, it should be burned in oven (+125°C, > 12 hours) before mounted on PCB.*

~~20.~~23. Instruction Set OP-Code and Clock Cycles

Function	Format				Clocks	Notes
DATA TRANSFER INSTRUCTIONS						
MOV = Move						
register to register/memory	1000100w	mod reg r/m			1/1	
register/memory to register	1000101w	mod reg r/m			1/6	
immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1	1/1	
immediate to register	1011w reg	data	data if w=1		1	
memory to accumulator	1010000w	addr-low	addr-high		6	
accumulator to memory	1010001w	addr-low	addr-high		1	
register/memory to segment register	10001110	mod 0 reg r/m			3/8	
segment register to register/memory	10001100	mod 0 reg r/m			2/2	
PUSH = Push						
memory	11111111	mod 110 r/m			8	
register	01010 reg				3	
segment register	000reg110				2	
immediate	011010s0	data	data if s=0		1	
POP = Pop						
memory	10001111	mod 000 r/m			8	
register	01011 reg				6	
segment register	000 reg 111	(reg≠01)			8	
PUSHA = Push all	01100000				36	
POPA = Pop all	01100001				44	
XCHG = Exchange						
register/memory	1000011w	mod reg r/m			3/8	
register with accumulator	10010 reg				3	
XTAL = Translate byte to AL	11010111				10	
IN = Input from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
OUT = Output from						
fixed port	1110010w	port			12	
variable port	1110110w				12	
LEA = Load EA to register	10001101	mod reg r/m			1	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod≠11)		14	
LES = Load pointer to ES	11000100	mod reg r/m	(mod≠11)		14	
ENTER = Build stack frame	11001000	data-low	data-high	L		
L = 0					7	
L = 1					11	
L > 1					11+10(L-1)	
LEAVE = Tear down stack frame	11001001				7	
LAHF = Load AH with flags	10011111				2	
SAHF = Store AH into flags	10011110				2	
PUSHF = Push flags	10011100				2	
POPF = Pop flags	10011101				11	
ARITHMETIC INSTRUCTIONS						
ADD = Add						
reg/memory with register to either	000000dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 000 r/m	data	data if sw=01	1/8	
immediate to accumulator	0000010w	data	data if w=1		1	

Function	Format				Clocks	Notes
ADC = Add with carry						
reg/memory with register to either	000100dw	mod reg r/m			1/7	
immediate to register/memory	100000sw	mod 010 r/m	data	data if sw=01	1/8	
immediate to accumulator	0001010w	data	data if w=1		1	
INC = Increment						
register/memory	1111111w	mod 000 r/m			1/8	
register	01000 reg				1	
SUB = Subtract						
reg/memory with register to either	001010dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 101 r/m	data	data if sw=01	1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
SBB = Subtract with borrow						
reg/memory with register to either	000110dw	mod reg r/m			1/7	
immediate from register/memory	100000sw	mod 011 r/m			1/8	
immediate from accumulator	0001110w	data	data if w=1		1	
DEC = Decrement						
register/memory	1111111w	mod 001 r/m			1/8	
register	01001 reg				1	
NEG = Change sign						
register/memory	1111011w	mod reg r/m			1/8	
CMP = Compare						
register/memory with register	0011101w	mod reg r/m			1/7	
register with register/memory	0011100w	mod reg r/m			1/7	
immediate with register/memory	100000sw	mod 111 r/m	data	data if sw=01	1/7	
immediate with accumulator	0011110w	data	data if w=1		1	
MUL = multiply (unsigned)	1111011w	mod 100 r/m				
register-byte					13	
register-word					21	
memory-byte					18	
memory-word					26	
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m				
register-byte					16	
register-word					24	
memory-byte					21	
memory-word					29	
register/memory multiply immediate (signed)	011010s1	mod reg r/m	data	data if s=0	23/28	
DIV = Divide (unsigned)	1111011W	mod 110 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
IDIV = Integer divide (signed)	1111011w	mod 111 r/m				
register-byte					18	
register-word					26	
memory-byte					23	
memory-word					31	
AAS = ASCII adjust for subtraction	00111111				3	
DAS = Decimal adjust for subtraction	00101111				2	
AAA = ASCII adjust for addition	00110111				3	
DAA = Decimal adjust for addition	00100111				2	
AAD = ASCII adjust for divide	11010101	00001010			14	
AAM = ASCII adjust for multiply	11010100	00001010			15	
CBW = Corrvert byte to word	10011000				2	
CWD = Convert word to double-word	10011001				2	

Function	Format				Clocks	Notes
BIT MANIPULATION INSTRUCTUIONS						
NOT = Invert register/memory	1111011w	mod 010 r/m			1/7	
AND = And						
reg/memory and register to either	001000dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 100 r/m	data	data if w=1	1/8	
immediate to accumulator	0010010w	data	data if w=1		1	
OR = Or						
reg/memory and register to either	000010dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1	1/8	
immediate to accumulator	0000110w	data	data if w=1		1	
XOR = Exclusive or						
reg/memory and register to either	001100dw	mod reg r/m			1/7	
immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1	1/8	
immediate to accumulator	0011010w	data	data if w=1		1	
TEST = And function to flags , no result						
register/memory and register	1000010w	mod reg r/m			1/7	
immediate data and register/memory	1111011w	mod 000 r/m	data	data if w=1	1/8	
immediate data and accumulator	1010100w	data	data if w=1		1	
Sifts/Rotates						
register/memory by 1	1101000w	mod TTT r/m			2/8	
register/memory by CL	1101001w	mod TTT r/m			1+n / 7+n	
register/memory by Count	1100000w	mod TTT r/m	count		1+n / 7+n	
STRING MANIPULATION INSTRUCTIONS						
MOVS = Move byte/word	1010010w				13	
INS = Input byte/word from DX port	0110110w				13	
OUTS = Output byte/word to DX port	0110111w				13	
CMPS = Compare byte/word	1010011w				18	
SCAS = Scan byte/word	101011w				13	
LODS = Load byte/word to AL/AX	1010110w				13	
STOS = Store byte/word from AL/AX	1010101w				7	
Repeated by count in CX:						
MOVS = Move byte/word	11110010	1010010w			4+9n	
INS = Input byte/word from DX port	11110010	0110110w			5+9n	
OUTS = Output byte/word to DX port	11110010	0110111w			5+9n	
CMPS = Compare byte/word	1111011z	1010011w			4+18n	
SCAS = Scan byte/word	1111001z	1010111w			4+13n	
LODS = Load byte/word to AL/AX	11110010	0101001w			3+9n	
STOS = Store byte/word from AL/AX	11110100	0101001w			4+3n	
PROGRAM TRANSFER INSTRUCTIONS						
Conditional Transfers — jump if:						
JE/JZ = equal/zero	01110100	disp			1/9	
JL/JNGE = less/not greater or equal	01111100	disp			1/9	
JLE/JNG = less or equal/not greater	01111110	disp			1/9	
JC/JB/JNAE = carry/below/not above or equal	01110010	disp			1/9	
JBE/JNA = below or equal/not above	01110110	disp			1/9	
JP/JPE = parity/parity even	01111010	disp			1/9	
JO = overflow	01110000	disp			1/9	
JS = sign	01111000	disp			1/9	
JNE/JNZ = not equal/not zero	01110101	disp			1/9	
JNL/JGE = not less/greater or equal	01111101	disp			1/9	
JNLE/JG = not less or equal/greater	01111111	disp			1/9	
JNC/JNB/JAE = not carry/not below /above or equal	01110011	disp			1/9	
JNBE/JA = not below or equal/above	01110111	disp			1/9	
JNP/JPO = not parity/parity odd	01111011	disp			1/9	
JNO = not overflow	01110001	disp			1/9	

Function	Format			Clocks	Notes
JNS = not sign	01111001	disp		1/9	
Unconditional Transfers					
CALL = Call procedure					
direct within segment	11101000	disp-low	disp-high	11	
reg/memory indirect within segment	11111111	mod 010 r/m		12/17	
indirect intersegment	11111111	mod 011 r/m	(mod≠11)	25	
direct intersegment	10011010	segment offset		18	
		selector			
RET = Retum from procedure					
within segment	11000011			16	
within segment adding immed to SP	11000010	data-low	data-high	16	
intersegment	11001011			23	
instersegment adding immed to SP	1001010	data-low	data-high	23	
JMP = Unconditional jump					
short/long	11101011	disp-low		9/9	
direct within segment	11101001	disp-low	disp-high	9	
reg/memory indirect within segment	11111111	mod 100 r/m		11/16	
indirect intersegment	11111111	mod 101 r/m	(mod ?11)	18	
direct intersegment	11101010	segment offset		11	
		selector			
Iteration Control					
LOOP = Loop CX times	11100010	disp		7/16	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp		7/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp		7/16	
JCXZ = Jump if CX = zero	11100011	disp		7/15	
Interrupt					
INT = Interrupt					
Type specified	11001101	type		41	
Type 3	11001100			41	
INTO = Interrupt on overflow	11001110			43/4	
BOUND = Detect value out of range	01100010	mod reg r/m		21-60	
IRET = Interrupt return	11001111			31	
PROCESSOR CONTROL INSTRUCTIONS					
CLC = clear carry	11111000			2	
CMC = Complement carry	11110101			2	
STC = Set carry	11111001			2	
CLD = Clear direction	11111100			2	
STD = Set direction	11111101			2	
CLI = Clear interrupt	11111010			5	
STI = Set interrupt	11111011			5	
HLT = Halt	11110100			1	
WAIT = Wait	10011011			1	
LOCK = Bus lock prefix	11110000			1	
ESC = Math coprocessor escape	11011MMM	mod PPP r/m		1	
NOP = No operation	10010000			1	
SEGMENT OVERRIDE PREFIX					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

~~21.~~24. R8822 Execution Timing

The above instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

1. The opcode, along with data or displacement required for execution, has been prefetched and resided in the instruction queue at the time needed.

2. No wait states or bus holds occur.

3. All word -data are located on even-address boundaries.

4. One RISC micro operation (*u*OP) maps one cycle (according to the pipeline stages described below), except the following case:

Pipeline stages for single micro operations (one cycle):

Fetch → Decode → op_r → ALU → WB (For ALU function *u*OP)

Fetch → Decode → EA → Access → WB (For memory function *u*OP)

4.1 *Memory read u*OP needs 6 cycles for bus.

Pipeline stages for *memory read u*OP (6 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB

Bus Cycle

4.2 *Memory push u*OP needs 1 cycle if it has no previous *memory push u*OP, and 5 cycles if it has previous *memory push* or *memory write u*OP.

Pipeline stages for *memory push u*OP after *memory push u*OP (another 5 cycles):

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → WB (1st *memory push u*OP)

(2nd *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

pipeline stall

4.3 *MUL u*OP and *DIV* of ALU function *u*OP for 8-bit operations need both 8 cycles, for 16-bit operations need both 16 cycles.

4.4 All jumps, calls, ret and loopXX instructions required to fetch the next instruction for the destination address (*unconditional fetch u*OP) will need 9 cycles.

Pipeline stages for unconditional fetch:

Fetch → Decode → EA → Access → Idle → T0 → T1 → T2 → T3 → Fetch (*Fetch u*OP)

(next *u*OP) Fetch → Decode → EA → Access → Access → Access → Access → Access → Idle → T0 → T1 → T2 → T3 → WB

will be flushed

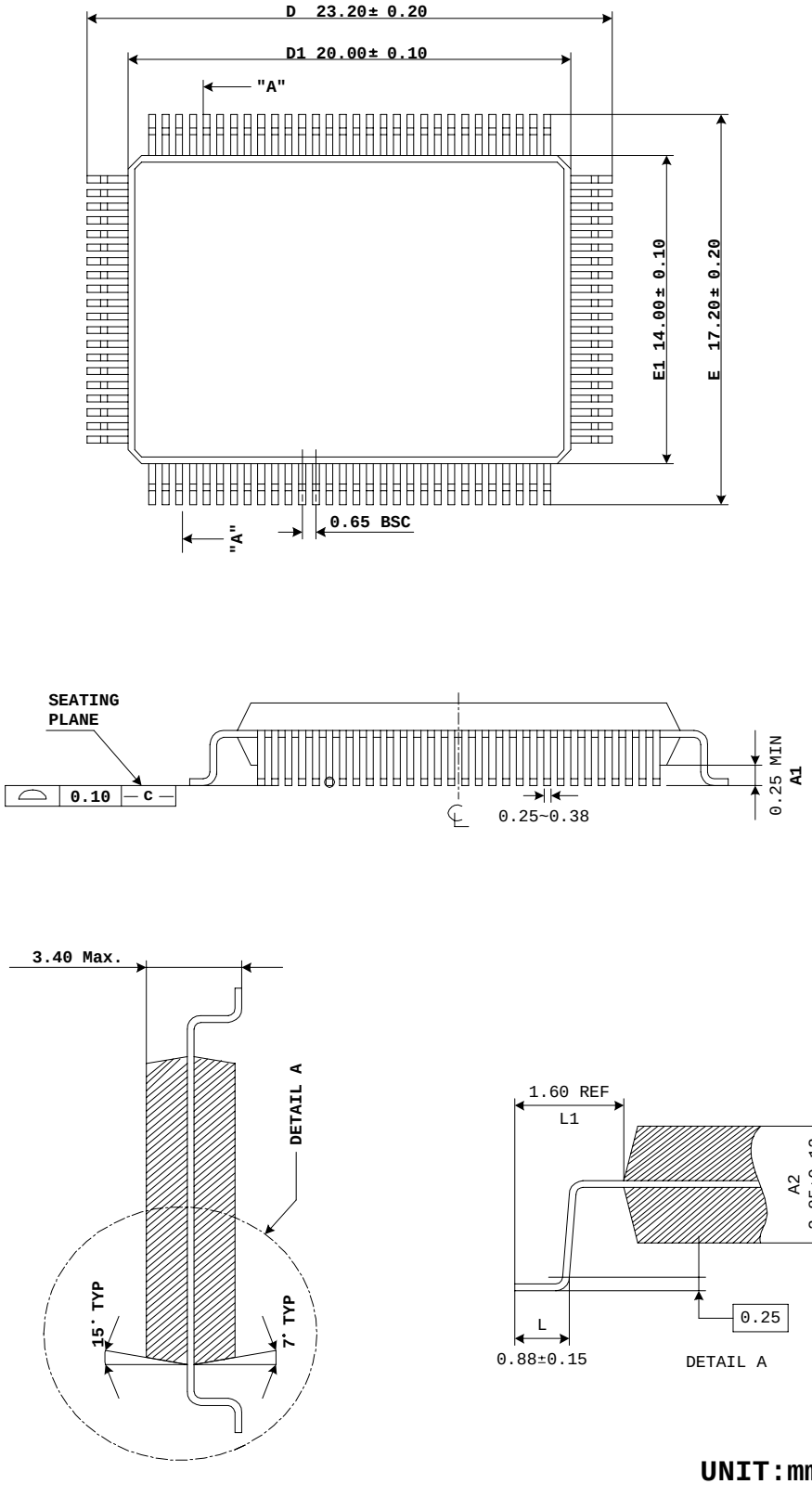
These 9 cycles cause branch penalty

→ Fetch → Decode → following stages...(New *u*OP)

***Note**: op_r: operand read stage; EA: Calculate Effective Address stage; Idle: Bus Idle stage; T0..T3: Bus T0..T3 stage; Access: Access data from cache memory stage.*

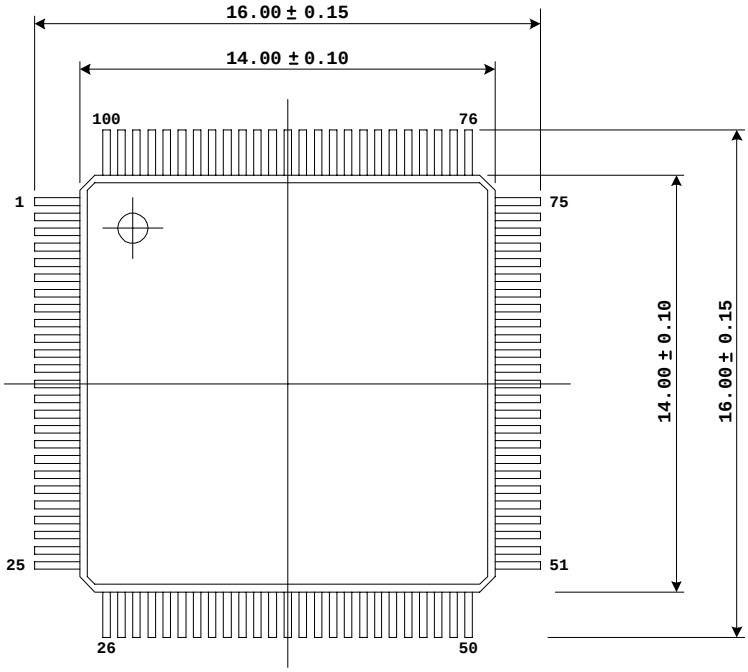
25. Package Information

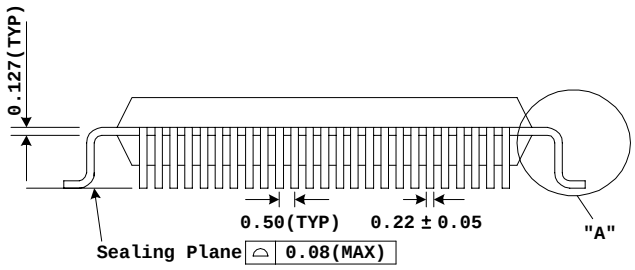
25.1 PQFP

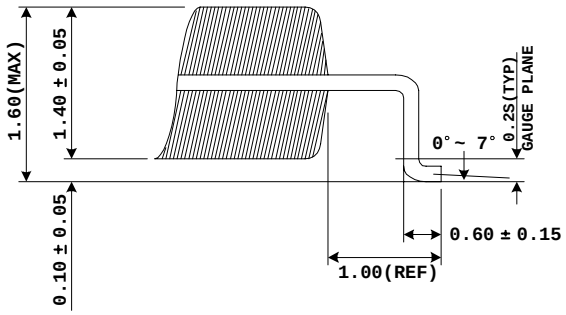


UNIT:mm

25.2 LQFP







UNIT:mm

26. Revision History

Rev.	Date	History
P10	2000/7/31	Preliminary Version
F11	2001/5/17	Final Version 1.1: Formal release
F12	2001/8/10	Modify Wait State Description (Page 30)
F13	2001/11/29	DC Characteristics
F14	2001/12/25	Modify Oscillator Characteristics
F15	2002/05/08	Modify Wait State Description
F16	2004/01/05	Modify DC Characteristics and add Thermal Characteristics.
F17	2005/05/19	Final Version 1.7 Page 120 & 121: Package Information modified.