2.1 Channel Digital Amplifier with 12V Driver Single Chip

BI30020B

Data Sheet

Rev.1.4, 2006.02.10

Biforst Technology Inc.

2.1 Channel Digital Amplifier with 12V Driver Single Chip

BI30020B

GENERAL DESCRIPTION

The BI30020B is the very right choice for 2.1 channel or 2 channel audio systems. The BI30020B is a newest generation of pure digital amplifier that is embedded with Digital Electronic Crossover, 12V Speaker Driver & Earphone Driver. Directly input 2 channel digital audio data, the BI30020B will generate 3 sets of signal for Left, Right and Sub-Woofer Channels. Each set of signal can select crossover frequency and Sub-Woofer's phase to drive speakers without external complicated Filter circuit. The powerful Audio Volume Control includes power-on Initial volume function, 32-Level Audio Volume Control and Mute Control. It also provides Volume Boost and Anti-Clipping function. The quality of sound is pure and full which is much different from the traditional Class AB Amplifier.

APPLICATION

- Note-book/Desktop PC/LCD Monitor/TV Surround Sound Systems
- Portable DVD/VCD/CD/MP3 Speakers and Headphones
- Video Game Speakers

FEATURE

- Operation Voltage:
  - Digital Part: 3.0 ~ 3.6V
  - Speaker Driver: 3.0 ~ 13.5V
  - Earphone Driver：3.0 ~ 3.6V
- Operation Frequency:
  - Accept 512xFS or 45.1584 ~ 49.152MHz For Operation
- Audio Data Input Interface:
  - When Use Internal SRC, Accept 29 ~ 96KHz Wide Continue Sample Rate Range
  - When Use External 512xFS Clock Source, Accept 8K ~ 96KHz Sample Rate
  - Support I^2S, Left-Justified, & Right-Justified Format
  - Auto Adapt Word Length For Left & Right Channel In I2S & Left-Justified Mode
  - Provide 24/20/18/16-Bits Word Length Select For Left & Right Channel In Right-Justified Mode
  - Provide Left/Right Frame Select Exchange Function
  - Provide Serial Clock Positive or Negative Latch Data Select
- Control Interface:
  - Provide Hardware Mode Without MCU
  - Provide I^2C Control Mode

- Crossover Frequency Select:
  - 14 Crossover Frequency Selects Through External Pin
  - Crossover Frequency from 150Hz To 800 Hz, 50Hz For Each Step
- Speaker Driver:
  - Provide 2 Channel or 2.1 Channel Output Configuration
  - Main Channel:
    - Output Can Select Bypass or Through Internal Digital High Pass Filter Circuit
    - Provide Embedded Left/Right Channel Speaker Driver
      (2 x 6.5W @13.5V, 10% THD, 8 Ohm Load at 2.1 Channel or
      2 x 11.8W @13.5V, 10% THD, 4 Ohm Load at 2 Channel)
  - Sub-Woofer Channel:
    - Generate Sub-Woofer Channel Data From Main Channel Data
    - Sub-Woofer Channel Can Select 0 or 180 degree Output Phase
    - Proved Embedded Sub-Woofer Channel Speaker Driver
      (1 x 11.8W @13.5V, 10% THD, 4 Ohm Load at 2.1 Channel)
  - Earphone Channel
    - Provide 3 or 4-Wire Type Earphone Connection
- Audio Volume Control:
  - Provide 32 Level Volume Select
  - Set Power-On Initial Volume Value Through External Pin (Volume Value: Mute, 9, 16 & Max)
  - Main & Sub-Woofer Channel Volume Adjust Independent or Together Through External Pin in Hardware Mode
  - Main & Sub-Woofer Channel Have Digital Audio Volume Control Separately
  - Main Channel & Earphone Use Same Volume Control
  - Provide Volume Boost & Anti-Clipping Function Enable/Disable
- Mute Control:
  - Set Main & Sub-Woofer Mute Enable/Disable
- Temperature Sensor:
  - Active Temperature Sensor Through External Pin
  - Temperature Sensor Will Shut Down Speaker Driver When Chip Internal Temperature Over 125℃
- Output Control Interface:
  - Treble Level Control
  - Bass Level Control
  - Balance Channel Control
- Package Type:
  - HQFP 100 Pin (14x20x3.2mm)

ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	PARAMETER	VALUE	UNIT
V_{DDA}	Speaker Driver Power Supply Voltage	-0.3 to 13.5	V
V_{DD}	Digital Amplifier Kernel Power Supply Voltage	-0.3 to 3.6	V
V_{IN}	Input Signal Voltage	-0.3 to V_{DD} +0.3	V
Ta	Operating Temperature	-40 ~ +85	℃
Tst	Storage Temperature	-40 ~ +150	℃

Note 1: Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	SPECIFICATION			UNIT
		MIN	TYP	MAX	
V_{DDA}	Speaker Driver Supply Voltage	3.0		13.5	V
V_{DD}	Digital Part Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.7			V
V_{IL}	Input Low Voltage			0.5	V
V_{OH}	Output High Voltage	3.5			V
V_{OL}	Output Low Voltage			0.6	V
Ta	Operating Temperature	-40		85	℃

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Ta=25℃, V_{DDA} =12V, V_{DD}=3.3V)

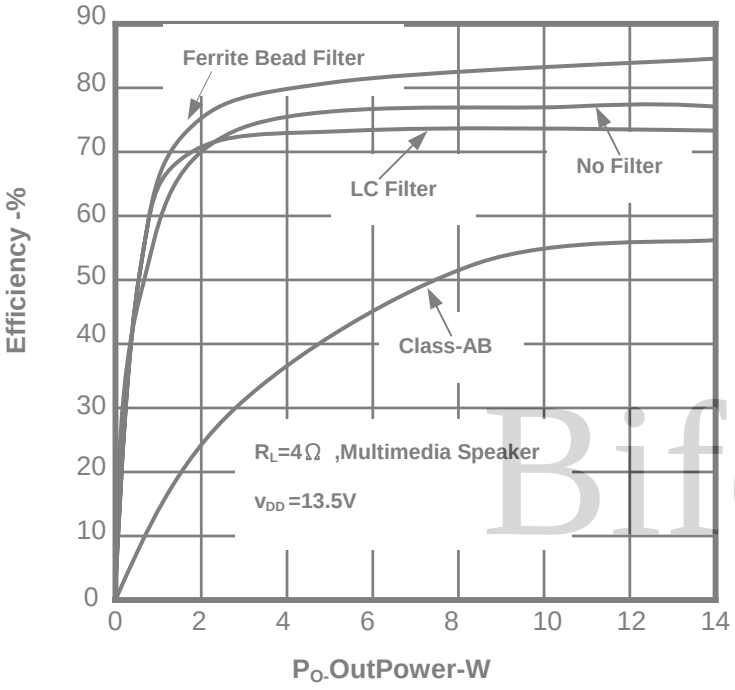
SYMBOL	PARAMETER	TEST CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
PSRR	Power supply rejection ratio	P V_{DDA} =12V		-77		dB
$\lvert I_{IH} \rvert$	High-level input current	P V_{DDA} =3.3V, V_I =P V_{DDA}			1	uA
$\lvert I_{IL} \rvert$	Low –level input current	P V_{DDA} =3.3V, V_I =0V			1	uA
I_{PWDN}	Power Down Current	Sysclk halt Audio output disable			1	uA

OPERATING CHARACTERISTICS (Ta=25℃, V_{DDA} =13.5V, V_{DD}=3.3V, R_L=4Ω, 2 channel; unless otherwise specified)

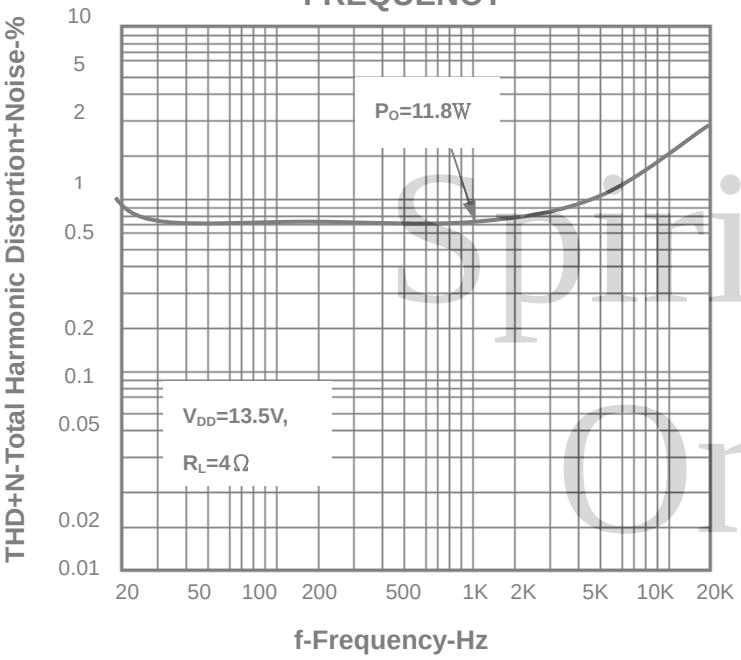
SYMBOL	PARAMETER	TEST CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
I_{DD}	DC Operating Current	I^2S input active		25		mA
P_O	Output Power	THD = 10%, R_L=4Ω		11.8		W
THD+N	Total Harmonic Distortion plus Noise	P_O = 8.3W			1%	
k_{SVR}	Supply ripple rejection ratio			-77		dB
SNR	Signal-to Noise Ratio	VR or VL Po = 0.6 W / one channel		88		dB
V_n	Noise output voltage			20		μ V_{Rms}

TYPICAL CHARACTERISTICS

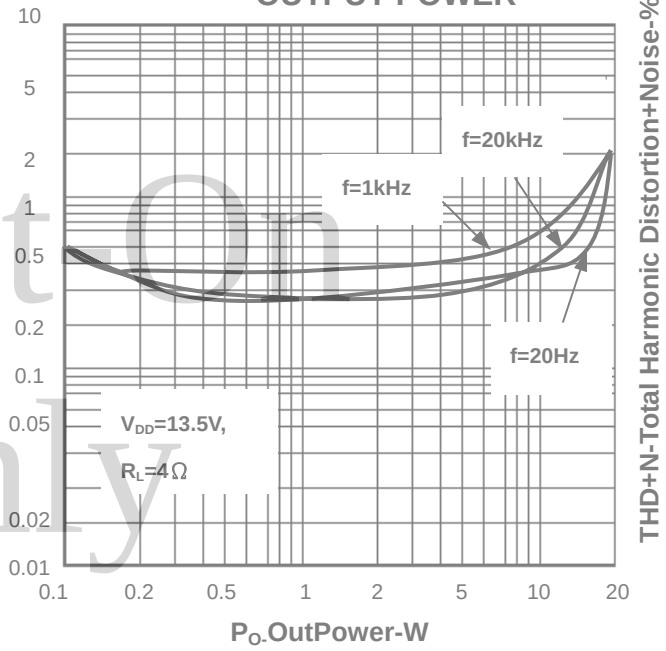
EFFICIENCY vs OUTPUT POWER



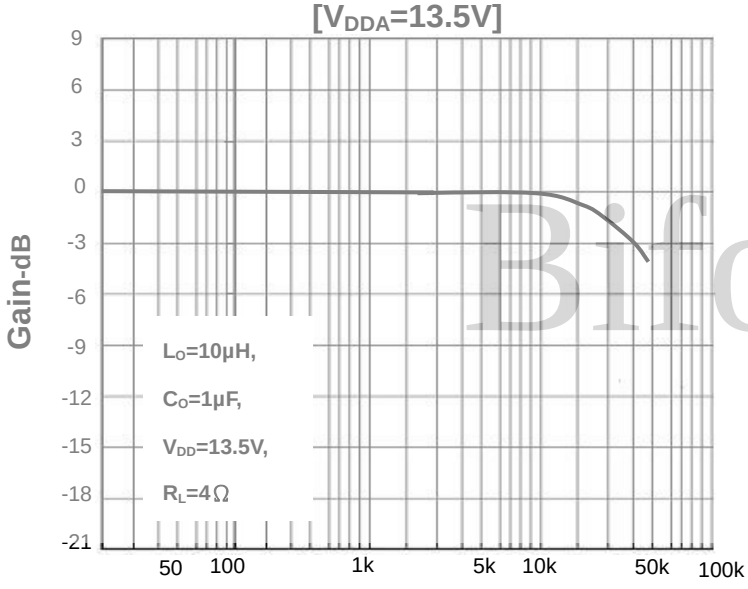
TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



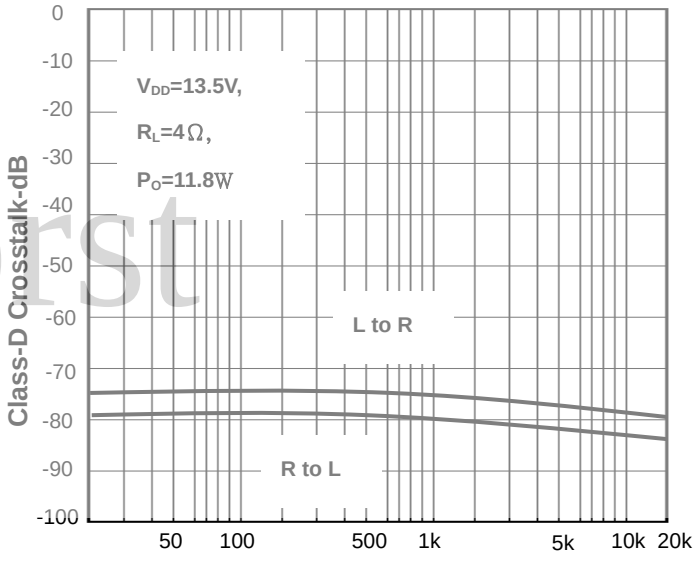
TOTAL HARMONIC DISTORTION+NOISE vs OUTPUT POWER



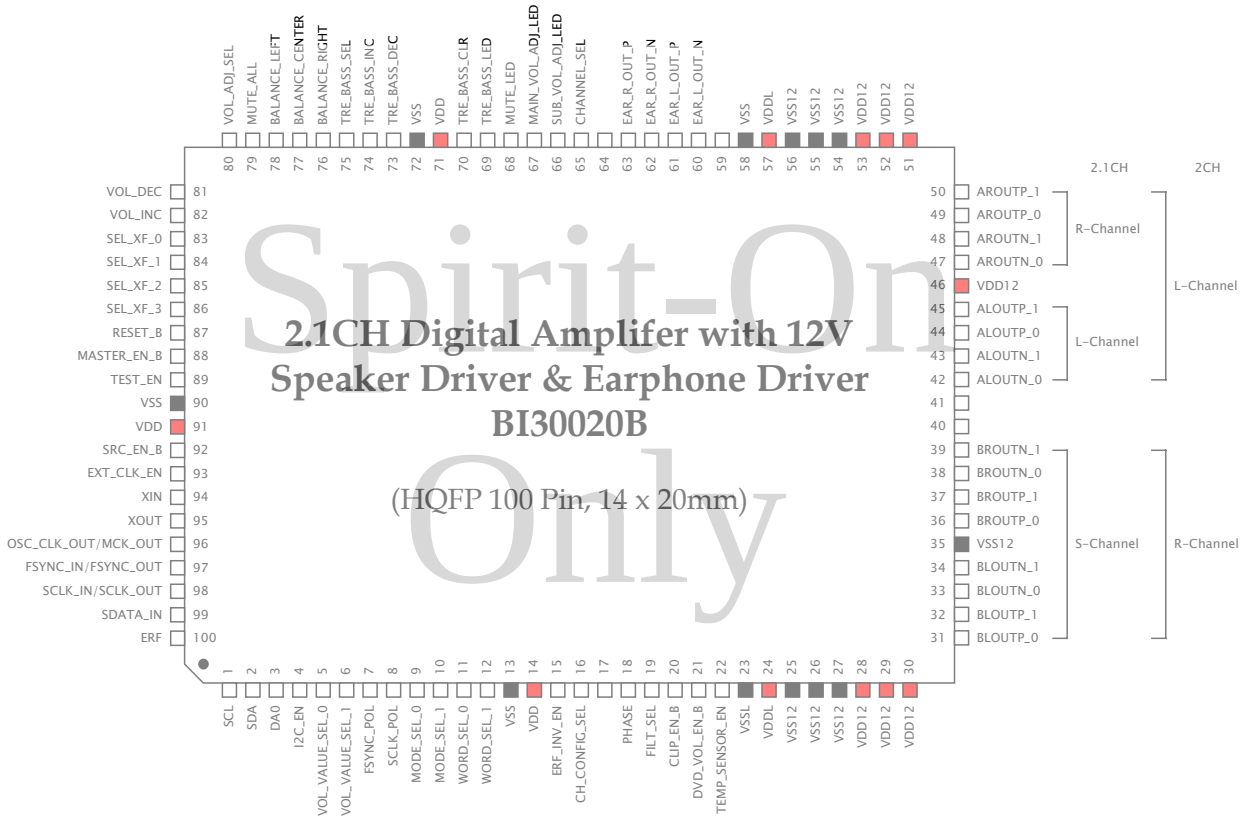
FREQUENCY CHARACTERISTICS [V_{DDA}=13.5V]



CROSSTALK



Pin Assignment



Pin List & Description

Pin No.	Pin	Type	I/O Pad Function
1	SCL	Input (3.3V)	I^2C Serial Clock Input
2	SDA	Bi-Direction (3.3V)	I^2C Serial Data Input with Open-Drain Output
3	DA0	Input (3.3V)	I^2C Device Address Select *0 : 0010_110* *1 : 0010_111*
4	I2C_EN	Input (3.3V)	Hardware Mode or I^2C Control Mode Select *0 : Hardware Mode* *1 : I^2C Control Mode*
5	VOL_VALUE_SEL_0	Input (3.3V)	Initial Volume Value Select *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 00 : Volume 31* *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 01 : Volume 16* *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 10 : Volume 9* *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 11 : Volume 0*
6	VOL_VALUE_SEL_1		
7	FSYNC_POL	Input (3.3V)	Serial Audio Data Signal “FSYNC_IN” Left/Right Frame Select *0 : Low Level = Right Channel, High Level = Left Channel* *1 : Low Level = Left Channel, High Level = Right Channel* (Must Set To VDD or Ground in I^2C Control Mode)

Pin No.	Pin	Type	I/O Pad Function
8	SCLK_POL	Input (3.3V)	Serial Audio Data Signal “SCLK_IN” Polarity Select *0 : Serial Clock Falling Edge Latch Data* *1 : Serial Clock Rising Edge Latch Data* (Must Set To VDD or Ground in I2C Control Mode)
9	MODE_SEL_0	Input (3.3V)	Serial Audio Data Input Format Select *(MODE_SEL_1, MODE_SEL_0) = 00 : I^2S Format Mode Select* *(MODE_SEL_1, MODE_SEL_0) = 01 : I^2S Format Mode Select* *(MODE_SEL_1, MODE_SEL_0) = 10 : Left-Justified Mode Select* *(MODE_SEL_1, MODE_SEL_0) = 11 : Right-Justified Mode Select* (Must Set To VDD or Ground in I2C Control Mode)
10	MODE_SEL_1		
11	WORD_SEL_0	Input (3.3V)	Serial Audio Data Input Length Select (For Right-Justified Mode Only) *(WORD_SEL_1, WORD_SEL_0) = 00 : 24-bits* *(WORD_SEL_1, WORD_SEL_0) = 01 : 20-bits* *(WORD_SEL_1, WORD_SEL_0) = 10 : 18-bits* *(WORD_SEL_1, WORD_SEL_0) = 11 : 16-bits* (Must Set To VDD or Ground in I2C Control Mode)
12	WORD_SEL_1		
13	VSS	Power	3.3V Ground Input
14	VDD	Power	3.3V VDD Input
15	ERF_INV_EN	Input (3.3V)	Digital Amplifier Error Flag Input *(ERF_INV_EN, ERF = 00) : Enable Digital Amplifier* *(ERF_INV_EN, ERF = 01) : Disable Digital Amplifier* *(ERF_INV_EN, ERF = 10) : Disable Digital Amplifier* *(ERF_INV_EN, ERF = 11) : Enable Digital Amplifier*
16	CH_CONFIG_SEL	Input (3.3V)	2/2.1 Channel Output Select *0 : 2.1 Channel* *1 : 2 Channel* (Must Set To VDD or Ground in I2C Control Mode)
17	NC		
18	PHASE	Input (3.3V)	Sub-Woofer Channel Output Phase Select *0 : 0 Degree* *1 : 180 Degree* (Must Set To VDD or Ground in I2C Control Mode)
19	FILT_SEL	Input (3.3V)	Main Channel Digital High Pass Filter Bypass Enable Signal Input *0 : Digital High Pass Filter Active, Cross Over Frequency Set from SEL_XF_0 ~ SEL_XF_3* *1 : Digital High Pass Filter Bypass* (Must Set To VDD or Ground in I2C Control Mode)
20	CLIP_EN_B	Input (3.3V)	Speaker Output Anti-Clipping Enable *0 : Internal Speaker Output Anti-Clipping Circuit Disable* *1 : Internal Speaker Output Anti-Clipping Circuit Enable* (Must Set To VDD or Ground in I2C Control Mode)
21	DVD_VOL_EN_B	Input (3.3V)	Speaker Output Volume Boost Enable *0 : Volume Boost Enable (Loud than DVD_VOL_EN = 0)* *1 : Volume Boost Disable* (Must Set To VDD or Ground in I2C Control Mode)

Pin No.	Pin	Type	I/O Pad Function
22	TEMP_SENSOR_EN	Input (3.3V)	Temperature Sensor Enable *0 : Temperature. Sensor Disable* *1 : Temperature. Sensor Enable*
23	VSSL	Power	Speaker Driver 3.3V Ground Input
24	VDDL	Power	Speaker Driver 3.3V VDD Input
25	VSS12	Power	Speaker Driver 12V Ground Input
26	VSS12		
27	VSS12		
28	VDD12	Power	Speaker Driver 12V VDD Input
29	VDD12		
30	VDD12		
31	BLOUTP_0	Driver (3.3 ~ 12V)	CH_CONFIG_SEL = 0 : Sub-Woofer Channel Positive PWM Signal Output CH_CONFIG_SEL = 1 : Right Channel Positive PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
32	BLOUTP_1		
33	BLOUTN_0	Driver (3.3 ~ 12V)	CH_CONFIG_SEL = 0 : Sub-Woofer Channel Negative PWM Signal Output CH_CONFIG_SEL = 1 : Right Channel Negative PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
34	BLOUTN_1		
35	VSS12	Power	Speaker Driver 12V Ground Input
36	BROUTP_0	Driver (3.3 ~ 12V)	CH_CONFIG_SEL = 0 : Sub-Woofer Channel Positive PWM Signal Output CH_CONFIG_SEL = 1 : Right Channel Positive PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
37	BROUTP_1		
38	BROUTN_0	Driver (3.3 ~ 12V)	CH_CONFIG_SEL = 0 : Sub-Woofer Channel Negative PWM Signal Output CH_CONFIG_SEL = 1 : Right Channel Negative PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
39	BROUTN_1		
40	NC		
41	NC		
42	ALOUTN_0	Driver (3.3 ~ 12V)	Left Channel Negative PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
43	ALOUTN_1		
44	ALOUTP_0	Driver (3.3 ~ 12V)	Left Channel Positive PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
45	ALOUTP_1		
46	VDD12	Power	Speaker Driver 12V VDD Input
47	AROUTN_0	Driver (3.3 ~ 12V)	CH_CONFIG_SEL = 0 : Right Channel Negative PWM Signal Output CH_CONFIG_SEL = 1 : Left Channel Negative PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
48	AROUTN_1		
49	AROUTP_0	Driver (3.3 ~ 12V)	CH_CONFIG_SEL = 0 : Right Channel Positive PWM Signal Output CH_CONFIG_SEL = 1 : Left Channel Positive PWM Signal Output *(Output Voltage Level Dependent On VDD12)*
50	AROUTP_1		
51	VDD12	Power	Speaker Driver 12V VDD Input
52	VDD12		
53	VDD12		

Pin No.	Pin	Type	I/O Pad Function
54	VSS12	Power	Speaker Driver 12V Ground Input
55	VSS12		
56	VSS12		
57	VDDL	Power	Speaker Driver 3.3V VDD Input
58	VSS	Power	Earphone Driver Ground Input
59	NC		
60	EAR_L_OUT_N	Driver (3.3V)	Earphone Left Channel Negative PWM Signal Output *(Output Voltage Level Dependent On VDD)*
61	EAR_L_OUT_P	Driver (3.3V)	Earphone Left Channel Positive PWM Signal Output *(Output Voltage Level Dependent On VDD)*
62	EAR_R_OUT_N	Driver (3.3V)	Earphone Right Channel Negative PWM Signal Output *(Output Voltage Level Dependent On VDD)*
63	EAR_R_OUT_P	Driver (3.3V)	Earphone Right Channel Positive PWM Signal Output *(Output Voltage Level Dependent On VDD)*
64	NC		
65	CHANNEL_SEL	Input (3.3V)	Speaker Driver or Earphone Driver Output Select *0 : Speaker Driver Output Enable* *1 : Earphone Driver Output Enable*
66	SUB_VOL_ADJ_LED	Output (3.3V)	Sub-Channel Volume Adjust Indication Output *0 : Sub-Woofer Channel Volume Adjust Disable* *1 : Sub-Woofer Channel Volume Adjust Enable*
67	MAIN_VOL_ADJ_LED	Output (3.3V)	Main-Channel Volume Adjust Indication Output *0 : Main-Channel Volume Adjust Disable* *1 : Main-Channel Volume Adjust Enable*
68	MUTE_LED	Output (3.3V)	Main & Sub-Channel Mute LED Indication Output *0 : Main & Sub-Woofer Channel Mute Disable* *1 : Main & Sub-Woofer Channel Mute Enable*
69	TRE_BASS_LED	Output (3.3V)	Adjust Treble or Bass Level Control Indication LED *0 : Adjust Treble Level Enable* *1 : Adjust Bass Level Enable*
70	TRE_BASS_CLR	Input (3.3V)	Clear Treble & Bass Level To Default Value Signal Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
71	VDD	Power	3.3V VDD Input
72	VSS	Power	3.3V Ground Input
73	TRE_BASS_DEC	Input (3.3V)	Decrease Treble or Bass Level Signal Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
74	TRE_BASS_INC	Input (3.3V)	Increase Treble or Bass Level Signal Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
75	TRE_BASS_SEL	Input (3.3V)	Adjust Treble or Bass Level Control Select *Initial → Adjust Bass Level → Adjust Treble Level → Loop Again* (Must Set To VDD or Ground in I2C Control Mode)
76	BALANCE_RIGHT	Input (3.3V)	Reduce Left Channel Without Affecting the Right Channel Signal Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)

Pin No.	Pin	Type	I/O Pad Function
77	BALANCE_CENTER	Input (3.3V)	Clear Balance Channel Setting Signal Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
78	BALANCE_LEFT	Input (3.3V)	Reduce Right Channel Without Affecting the Left Channel Signal Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
79	MUTE_ALL	Input (3.3V)	All Channel Mute Trigger Signal Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
80	VOL_ADJ_SEL	Input (3.3V)	Select Main Channel & Sub-Woofer Channel Volume Adjust Independently or Adjust Together *Initial → Adjust Together → Adjust Main Channel → Adjust Sub-Woofer Channel → Loop Again* (Must Set To VDD or Ground in I2C Control Mode)
81	VOL_DEC	Input (3.3V)	Audio Volume Decrease Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
82	VOL_INC	Input (3.3V)	Audio Volume Increase Input *Low Level Pulse Trigger Active* (Must Set To VDD or Ground in I2C Control Mode)
83	SEL_XF_0	Input (3.3V)	Cross Over Frequency Select *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0000 : 150Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0001 : 200Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0010 : 250Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0011 : 300Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0100 : 350Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0101 : 400Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0110 : 450Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 0111 : 500Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1000 : 550Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1001 : 600Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1010 : 650Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1011 : 700Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1100 : 750Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1101 : 800Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1110 : 800Hz* *SEL_XF_3, SEL_XF_2, SEL_XF_1, SEL_XF_0 = 1111 : 800Hz* (Must Set To VDD or Ground in I2C Control Mode)
84	SEL_XF_1		
85	SEL_XF_2		
86	SEL_XF_3		
87	RESET_B	Input (3.3V)	Reset Signal Input *0 : Reset Active (Must Maintain Low Level Great than 1ms)* *1 : Normal Operation*

Pin No.	Pin	Type	I/O Pad Function
88	MASTER_EN_B	Input (3.3V)	Digital Amplifier Receive Serial Audio Data in Master or Slave Mode *0 : In Master Mode, Pin 97 Switch to FSYNC_OUT function, & Pin 98 Switch to SCLK_OUT function* *1 : In Slave Mode, Pin 97 Switch to FSYNC_IN function, & Pin 98 Switch to SCLK_IN function*
89	TEST_EN	Input (3.3V)	Test Mode Enable *0 : Test Mode Disable* *1 : Test Mode Enable*
90	VSS	Power	3.3V Ground Input
91	VDD	Power	3.3V VDD Input
92	SRC_EN_B	Input (3.3V)	Internal SRC Circuit Enable *0 : SRC Enable* *1 : SRC Disable*
93	EXT_CLK_EN	Input (3.3V)	External Clock Input Enable *0 : Reserve* *1 : Use 45.1584 ~ 49.152MHz or 512xFS Clock to XIN Pin*
94	XIN	Input (3.3V)	External Clock Input Path *External 45.1584 ~ 49.152MHz or 512xFS Clock Input Path*
95	XOUT	Output	Floating In Normal Operate
96	OSC_CLK_OUT/ MCK_OUT	Output (3.3V)	TEST_EN = 0, BI30020B Internal System Clock Output TEST_EN = 1, Internal Chip OSC Clock Output Probe Point
97	FSYNC_IN/ FSYNC_OUT	Bi-Direction (3.3V)	Serial Audio Data Left/Right Frame Input/Output ♦ *MASTER_EN_B = 0, Serial Audio Data Left/Right Frame Output* ♦ *MASTER_EN_B = 1, Serial Audio Data Left/Right Frame Input*
98	SCLK_IN/ SCLK_OUT	Bi-Direction (3.3V)	Serial Audio Data Latch Clock Input/Output ♦ *MASTER_EN_B = 0, Serial Audio Data Latch Clock Output* ♦ *MASTER_EN_B = 1, Serial Audio Data Latch Clock Input*
99	SDATA_IN	Input (3.3V)	Serial Audio Data Input
100	ERF	Input (3.3V)	Digital Amplifier Error Flag Input *(ERF_INV_EN, ERF = 00) : Enable Digital Amplifier* *(ERF_INV_EN, ERF = 01) : Disable Digital Amplifier* *(ERF_INV_EN, ERF = 10) : Disable Digital Amplifier* *(ERF_INV_EN, ERF = 11) : Enable Digital Amplifier*

FUNCTION DESCRIPTION

Operation Clock Select

BI30020B requires a clock for internal circuit operation. There are two types of clocks can be accepted. One is external input of 512xFS and the other is to connect a Clock of 45.1584 ~ 49.152MHz.

The use and detail description is illustrated as below.

512xFS –512xFS clock is used when the system can provide the clock and this clock can syncronally generate the input audio data. To use the clock, the external pin of BI30020B “SRC_EN_B” is set to HIGH, and “EXT_CLK_EN” set to HIGH. The BI30020B will disable the

internal SRC (Sample Rate Converter) and input 512xFS clock to external pin of XIN for BI30020B's operation. The setting of "SRC_EN_B" is as Table 1 and "EXT_CLK_EN" as Table 2. Besides, Figure 1 shows the application circuit when BI30020B use external 512xFS clock and the internal SRC is disable.

(*The FS is the Sample Rate of Input Audio Data. For example, FS is 44.1KHz and 512xFS is 22.5792MHz. Table 3 lists the Operation Clock most frequently used)

Table 1. SRC_EN_B Configuration

SRC_EN_B	SRC Circuit Enable
0	SRC Enable
1	SRC Disable

Table 2. EXT_CLK_EN Configuration

EXT_CLK_EN	External Clock Input Enable
0	Reserve
1	External Clock Input Enable (Clock Input Through XIN Pin)

Table 3. General BI30020B Operation Clock (512xFS) List

FS (Sample Rate)	BI30020B Operation Clock: 512xFS
32K	16.384MHz
44.1K	22.5792MHz
48K	24.576MHz
88.2K	45.1584MHz
96K	49.152MHz

External Clock – When system cannot provide 512xFS Clock to BI30020B, "SRC_EN_B" must be set to LOW and "EXT_CLK_EN" set to HIGH. The BI30020B is required to connect a Clock of 45.1584 ~ 49.152MHz which 49.152MHz is highly recommended. Therefore, BI30020B can generate internal clock. Only directly input Digital Audio Data to BI30020B, it will automatically judge and adjust the best condition for operation according to the input Digital Audio Data. Figure 2 shows the application circuit when BI30020B use external Clock of 45.1584 ~ 49.152MHz and the internal SRC is enable.

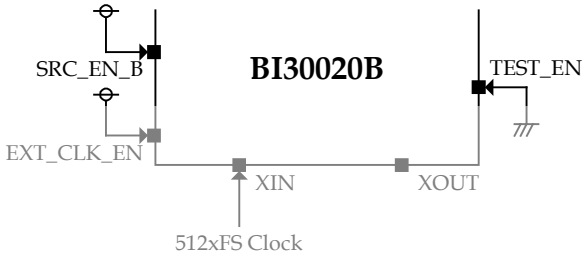


Figure 1. BI30020B Use External 512xFS Clock In SRC Disable

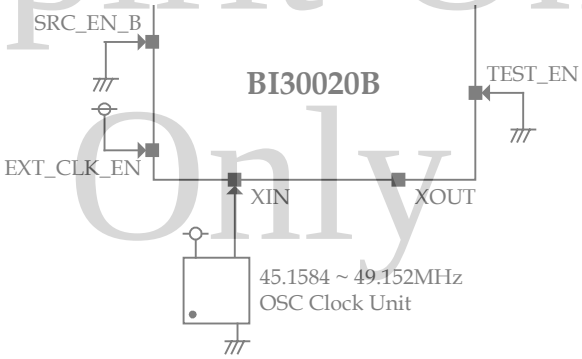


Figure 2. BI30020B Use External 45.1584~49.152MHz Clock In SRC Enable

Temperature Sensor Configuration

Temperature Sensor is built in BI30020B for detecting the temperature of embedded Speaker Driver. It can be turned on or off via pin of TEMP_SENSOR_EN. When TEMP_SENSOR_EN is set to Low, the Temperature Sensor is disable. While TEMP_SENSOR_ EN is set to High, the Temperature Sensor will be turned on. If the temperature of Speaker Driver is greater than 125℃, BI30020B will automatically shut down the Speaker Driver until the temperature back to normal operation range. BI30020B will automatically start the operation, again. Table 4 is the setup for Temperature Sensor.

Table 4. Temperature Sensor Configuration

TEMP_SENSOR_EN	Temperature Sensor Status
0	Disable
1	Enable

Reset

RESET_B pin of BI30020B is the Global Reset for all internal circuit. Table 5 is the setup of RESET_B. When reset BI30020B, RESET_B must be set to Low, and remain Low at least 1ms.Then return to High to complete the process of Reset. Therefore, it is recommended to discharge RC in the application circuit and design a simple circuit of Power On Reset to stable BI30020B after power on.

Table 5. RESET_B Configuration

RESET_B	BI30020B Status
0	Reset
1	Normal Operation

Digital Audio Data Interface in Master Mode & Slaver Mode

Setting BI30020B through the external pin of MASTER_EN_B can operate the Digital Audio Data Interface in Master Mode or Slaver Mode. When MASTER_EN_B is set to LOW, the Digital Audio Data Interface is in Master Mode. When MASTER_EN_B is set to HIGH, Digital Audio Data Interface is then in Slaver Mode. Table 6 lists the setup of MASTER_EN_B.

Figure 3 is the 1st example of BI30020B in Slaver Mode. When using the external 512xFS Clock as System Clock and disabling internal SRC, BI30020B receive Digital Audio Data via pins of FSYNC_IN, SCLK_IN and SDATA_IN.

Figure 4 is the 2nd example of BI30020B in Slaver Mode. When using the 49.152MHz Crystal to generate System Clock and enabling internal SRC, BI30020B receive Digital Audio Data via pins of FSYNC_IN, SCLK_IN and SDATA_IN.

Figure 5 is the example of BI30020B in Master Mode. When using the 49.152MHz Crystal to generate System Clock and enabling internal SRC, BI30020B receive Digital Audio Data via SDATA_IN and output FSYNC_OUT (48KHz) and SCLK_OUT (3.072MHz).

Table 6. MASTER_EN_B Configuration

MASTER_EN_B	BI30020B
0	Pin 97, FSYNC_OUT
	Pin 98, SCLK_OUT
1	Pin 97, FSYNC_IN
	Pin 98, SCLK_IN

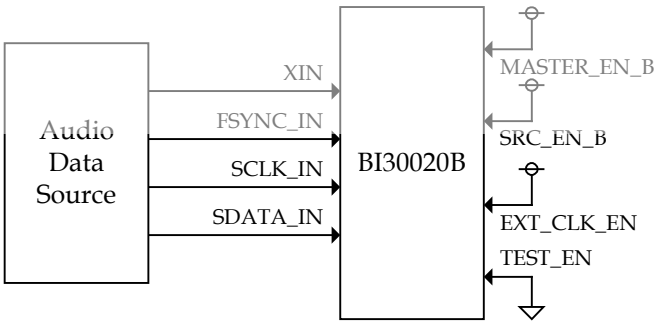


Figure 3. Example 1 – BI30020B Operate In Slaver Mode

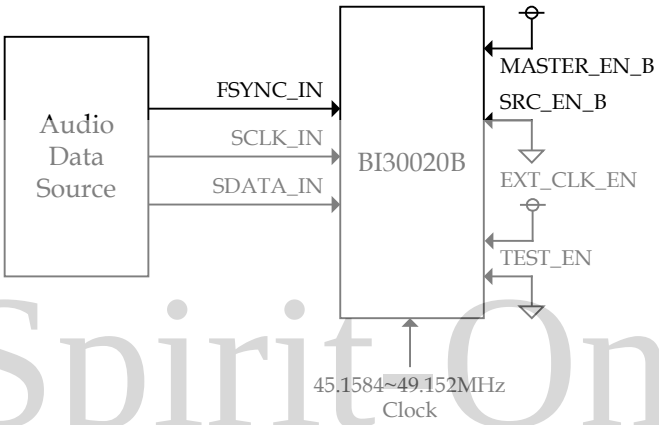


Figure 4. Example 2 – BI30020B Operate In Slaver Mode

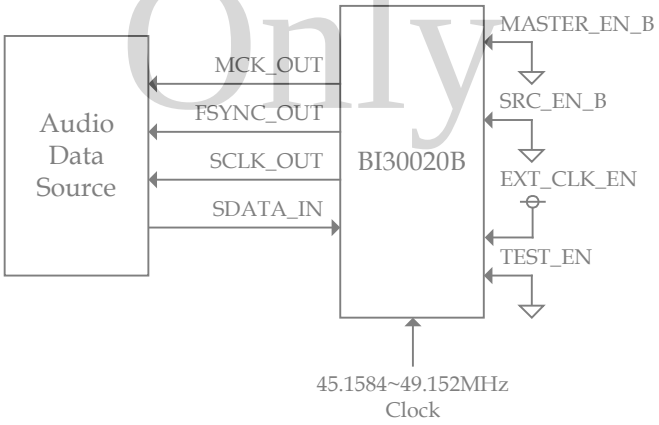


Figure 5. Example – BI30020B Operate In Master Mode

In addition, when TEST_EN is set to Low, the pin of OSC_CLK_OUT/MCK_OUT will become MCK_OUT output pin. Table 7 lists the configuration of OSC_CLK_OUT/MCK_OUT, TEST_EN and SRC_EN_B. Please note, when BI30020B operates with an external 49.152MHz Crystal and SRC enable, the MCK_OUT will output 12.288MHz in Master Mode and internal circuit will operate based on 48KHz Sample Rate.

Table 7. OSC_CLK_OUT/MCK_OUT Configuration

TEST_EN	SRC_EN_B	Muti-Output Pin "OSC_CLK_OUT/MCK_OUT"	Output Frequency
0	0	MCK_OUT	When XIN Pin Input 49.152MHz: In Slaver Mode: Audio Data's FS<64KHz, MCK_OUT=12.288MHz Audio Data's FS>64KHz, MCK_OUT=24.576MHz In Master Mode: MCK_OUT=12.288MHz
0	1	MCK_OUT	Same As Clock Frequency Input in XIN Pin/2
1	X	OSC_CLK_OUT	Same As Clock Frequency Input in XIN Pin

Speaker Driver & Earphone Driver Configuration

BI30020B provides 3 sets of 12V Speaker Driver. When CH_CONFIG_SEL is set to Low in Hardware Mode or Channel Configure Select (Address 0 Bit 0) is set to Low in I^2C Control Mode, BI30020B can connect 3 Speakers becoming 2.1Channel. Figure 6 shows the pins for connecting 3 Speakers of Left, Right and Sub-Woofer.

Besides, when CH_CONFIG_SEL is set to High in Hardware Mode or Channel Configure Select (Address 0 Bit 0) is set to High in I^2C Control Mode, BI30020B can connect 2 Speakers becoming 2 Channel. Figure 7 shows the pins for connecting 2 Speakers of Left and Right. Table 8 lists BI30020B Channel Configure Select Configuration.

Table 8. BI30020B Channel Configure Select Configuration

Channel Configure Select	Hardware Mode	I^2C Control Mode
2.1	Pin "CH_CONFIG_SEL" = 0	Channel Configure Select (Address 0 Bit 0) = 0
2	Pin "CH_CONFIG_SEL" = 1	Channel Configure Select (Address 0 Bit 0) = 1

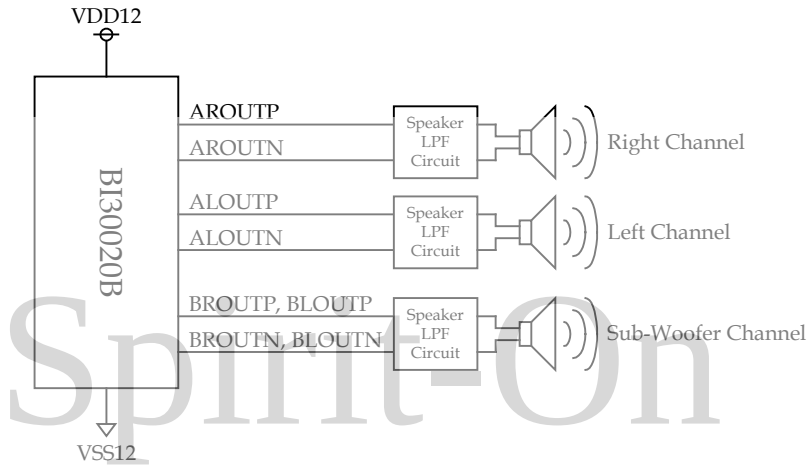


Figure 6. BI30020B Configure In 2.1 Channel

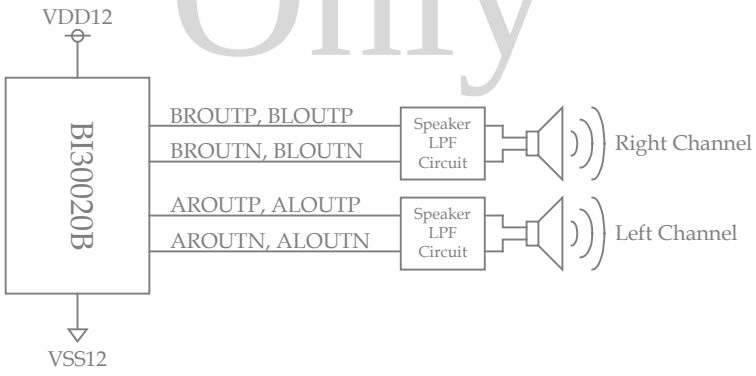


Figure 7. BI30020B Configure In 2 Channel

BI30020B also provides a set of Earphone Driver to connect 3 or 4-wire Earphone. Figure 8 demonstrates the connection. By wiring L- and R- signal output together as shown, BI30020B can connect to a 3-wire Earphone. BI30020B can also connect to a 4-wire Earphone by wiring each L- and R- to the Earphone. To select to output by Speaker Driver or Earphone is thus by setting the external pin of CHANNEL_SEL. Table 9 lists the configuration.

Table 9. BI30020B Speaker or Earphone Driver Output Select

CHANNEL_SEL Pin	Speaker or Earphone Driver Output Select
0	Speaker Driver Output
1	Earphone Driver Output

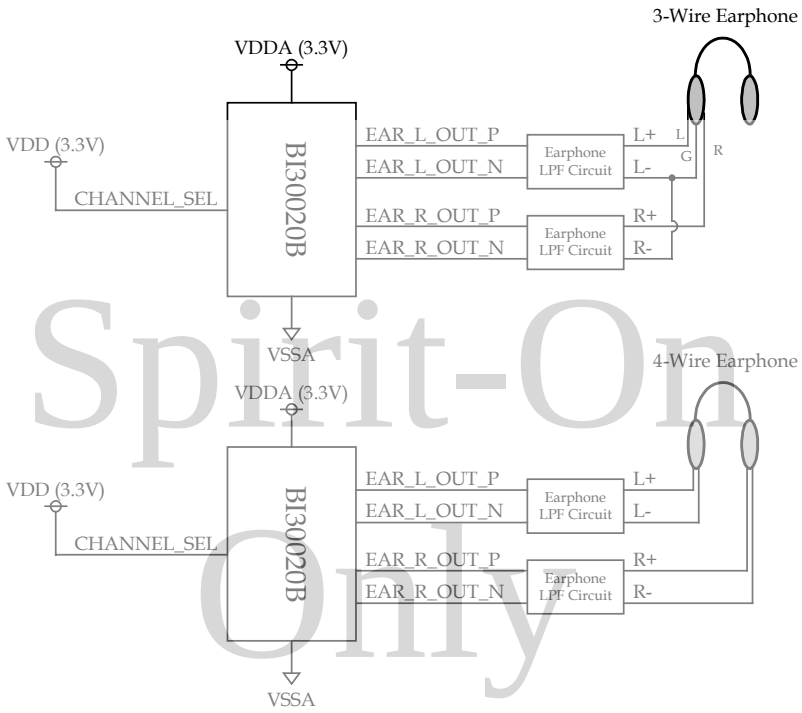


Figure 8. BI30020B Earphone Connection

Speaker Driver Capability

Here list the relationships of Driver Capability for 2.1 channel of Left/Right/Sub-Woofer Channels and 2 channel of Left/Right Channels when BI30020B is input 1KHz 0DB Sin Wave with 4 & 8 ohm load and output THD1% and 10%. The circuit for test and measurement is in Figure 9.

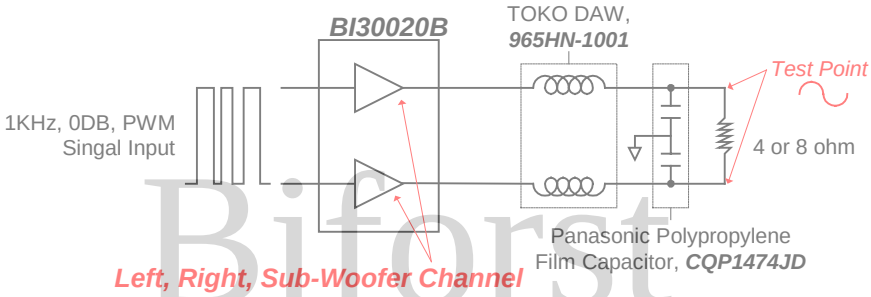


Figure 9. BI30020B Speaker Driver Capability Test Circuit

- **Left / Right Channel In 2.1 Channel Driver Capability**

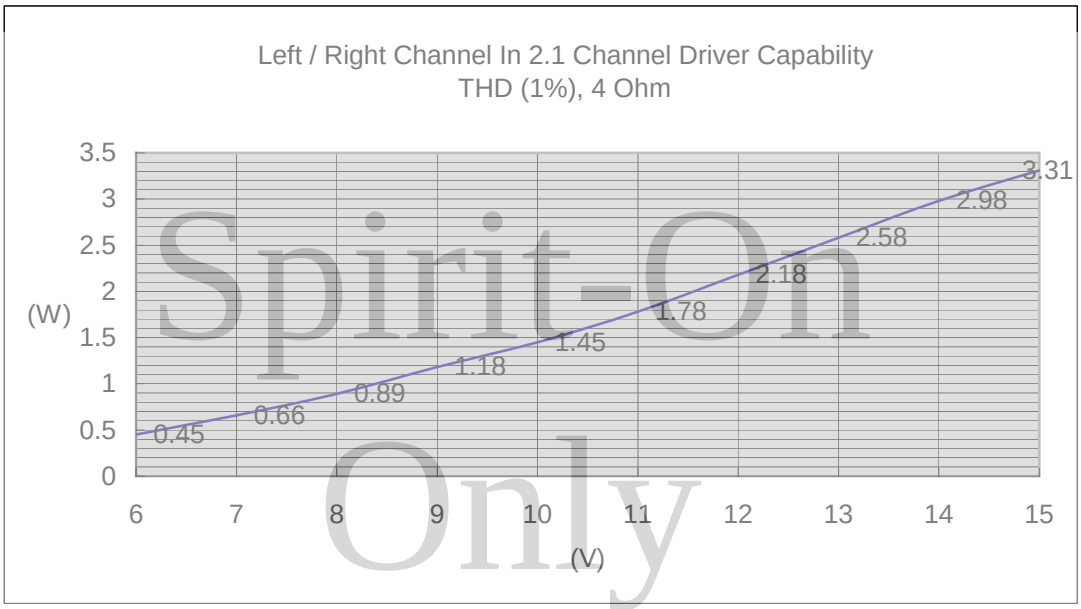


Figure 10. Left/Right Channel In 2.1 Channel Driver Capability (4 Ohm at THD 1%)

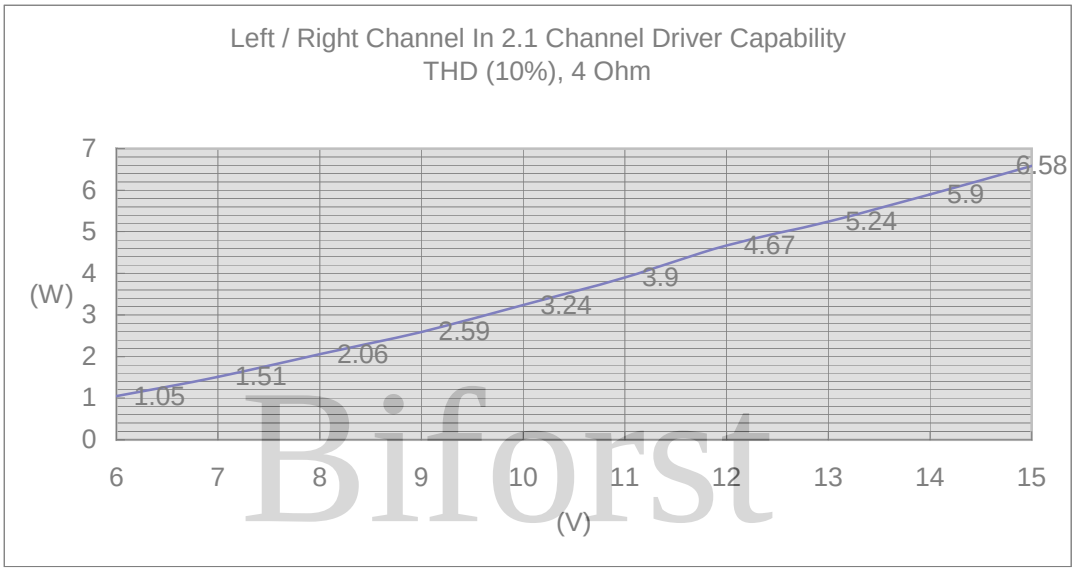


Figure 11. Left/Right Channel In 2.1 Channel Driver Capability (4 Ohm at THD 10%)

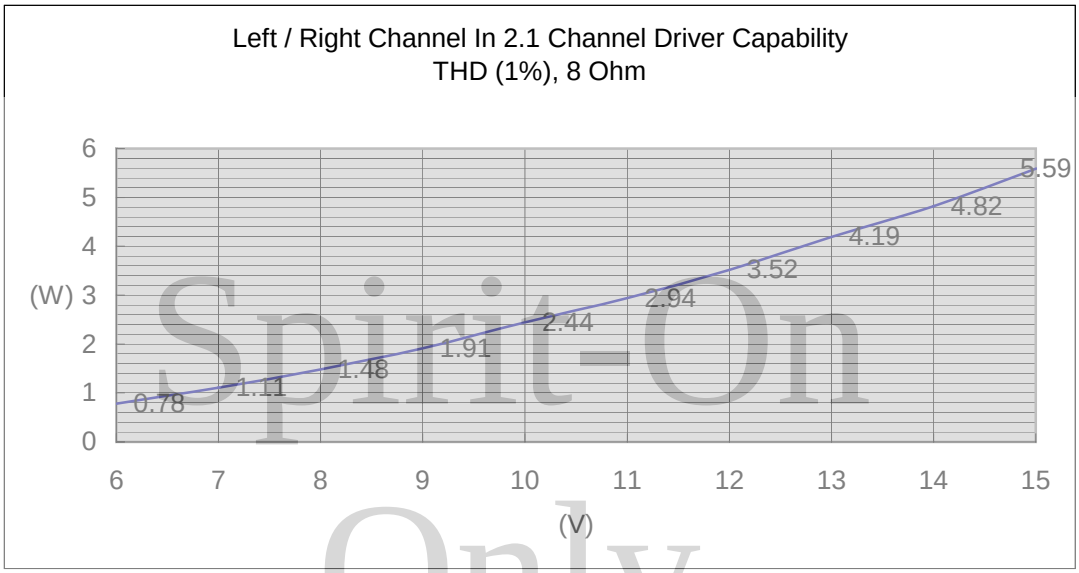


Figure 12. Left/Right Channel In 2.1 Channel Driver Capability (8 Ohm at THD 1%)

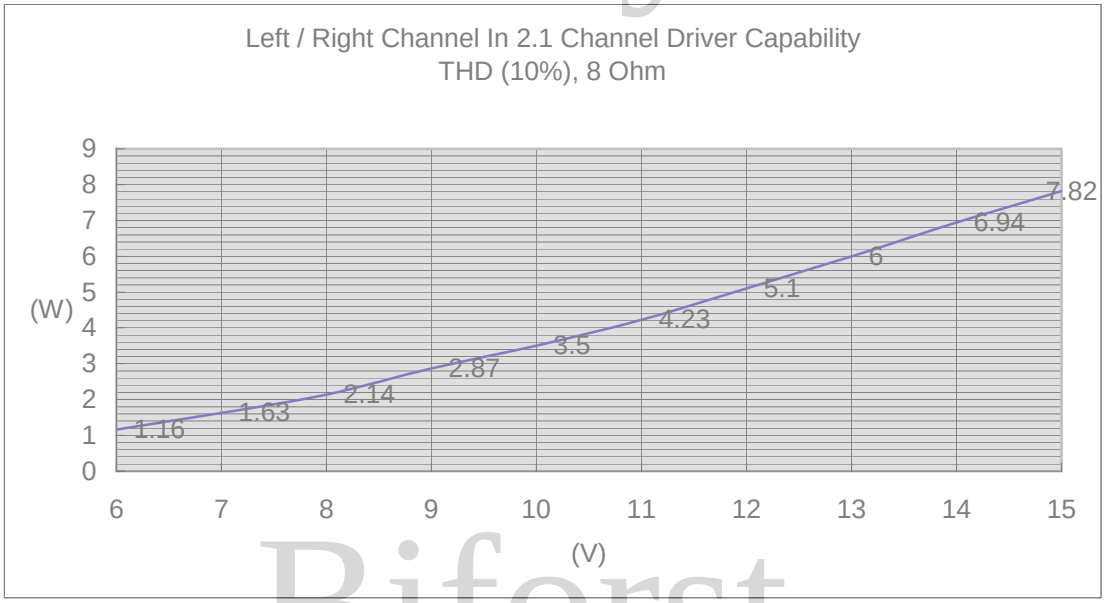


Figure 13. Left/Right Channel In 2.1 Channel Driver Capability (8 Ohm at THD 10%)

- **Sub-Woofer Channel In 2.1 Channel Driver Capability**

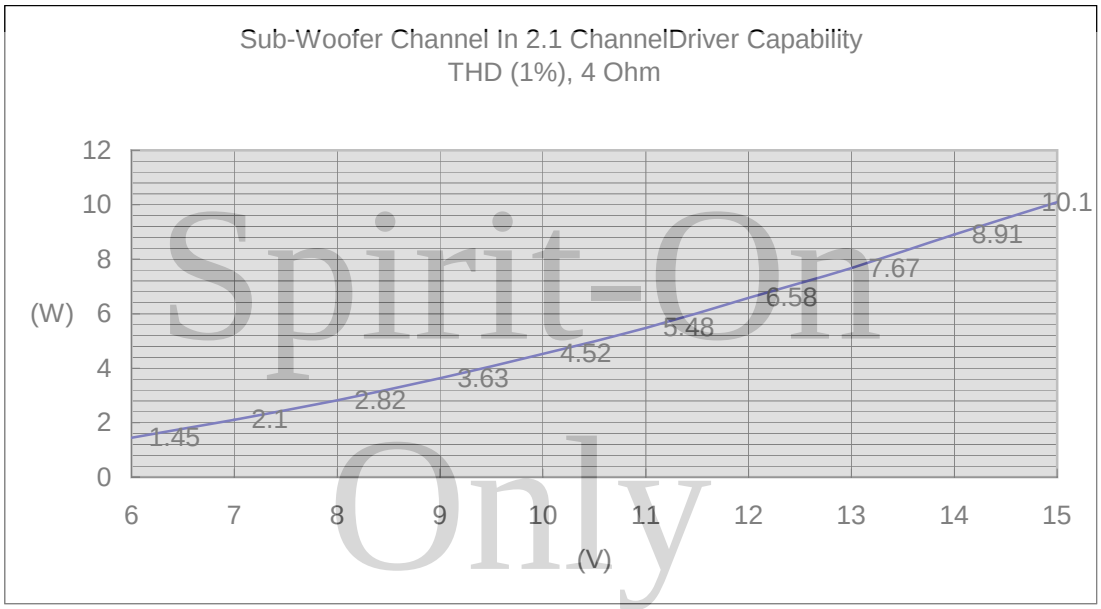


Figure 14. Sub-Woofer Channel In 2.1 Channel Driver Capability (4 Ohm at THD 1%)

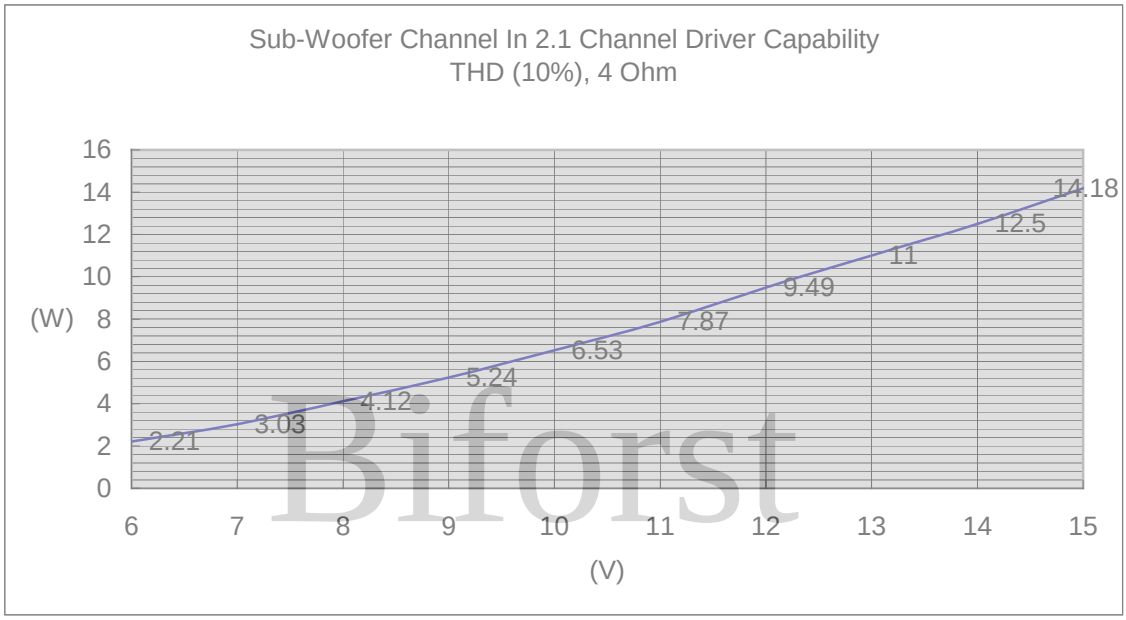


Figure 15. Sub-Woofer Channel In 2.1 Channel Driver Capability (4 Ohm at THD 10%)

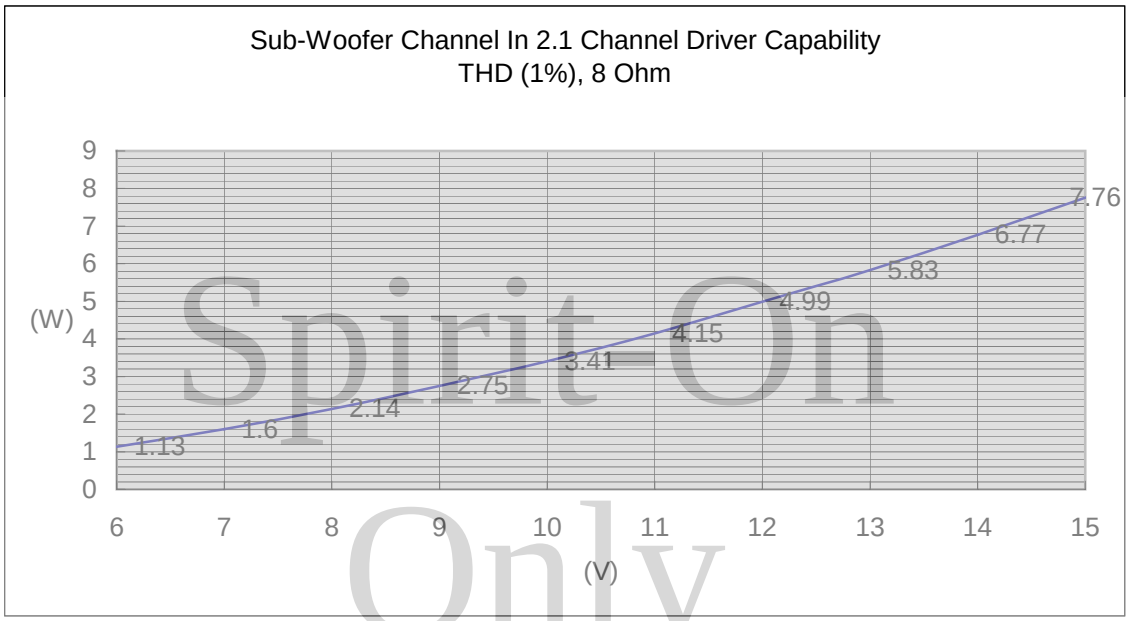


Figure 16. Sub-Woofer Channel In 2.1 Channel Driver Capability (8 Ohm at THD 1%)

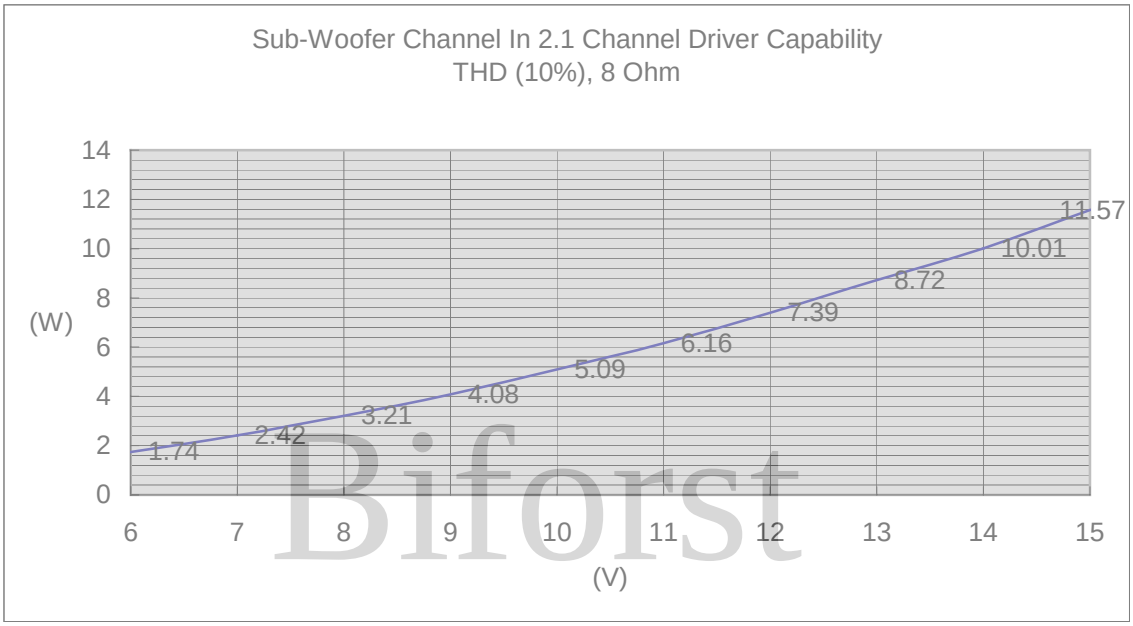


Figure 17. Sub-Woofer Channel In 2.1 Channel Driver Capability (8 Ohm at THD 10%)

- **Left / Right Channel In 2 Channel Driver Capability**

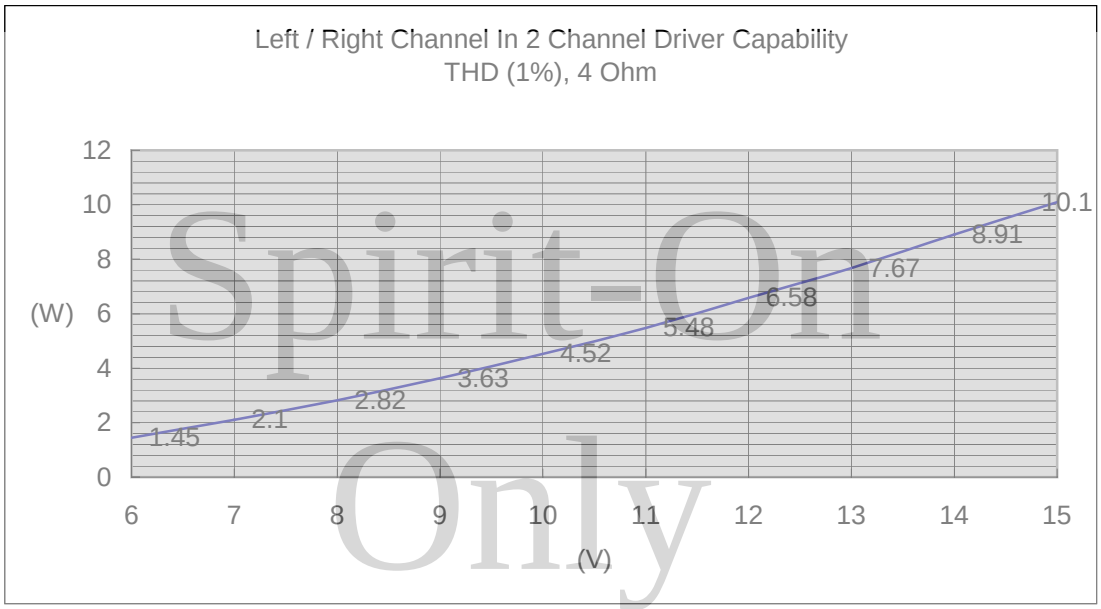


Figure 18. Left/Right Channel In 2 Channel Driver Capability (4 Ohm at THD 1%)

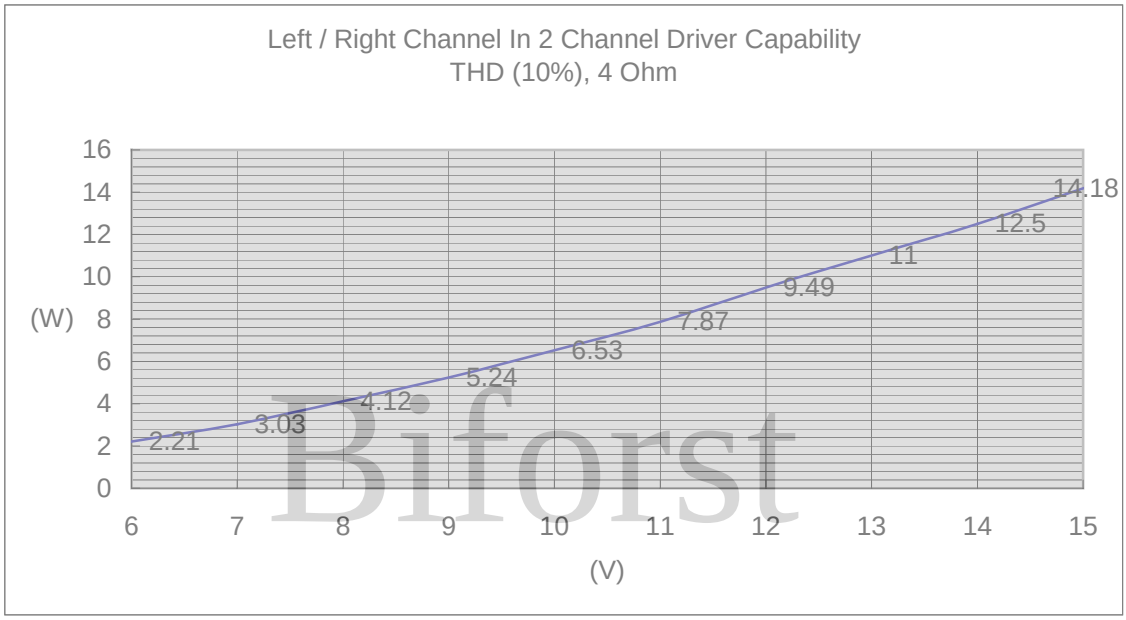


Figure 19. Left/Right Channel In 2 Channel Driver Capability (4 Ohm at THD 10%)

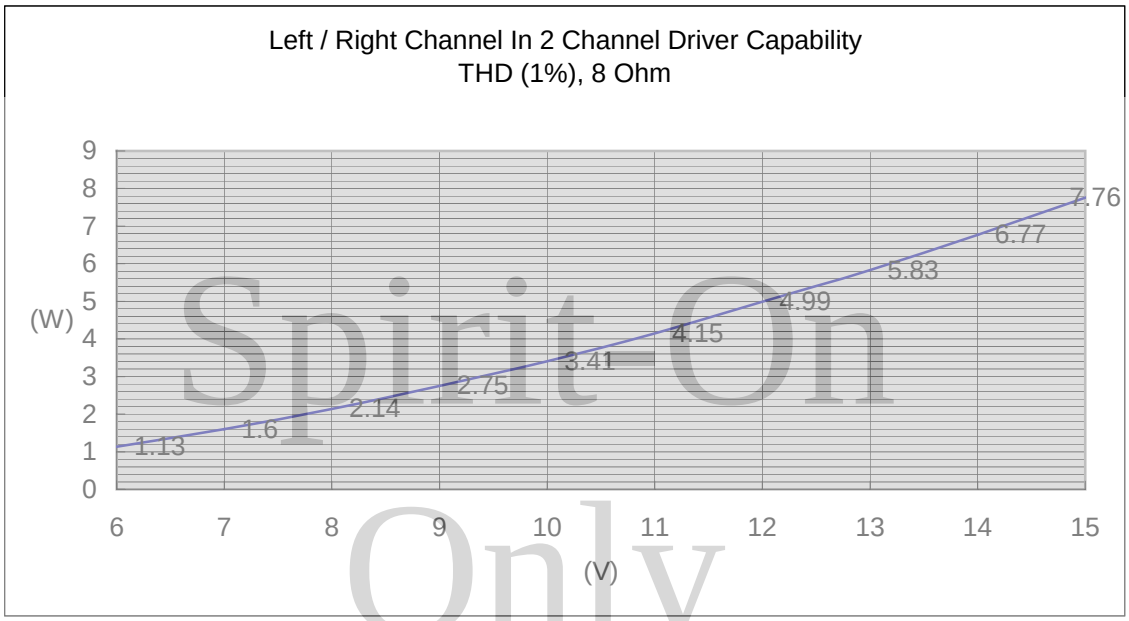


Figure 20. Left/Right Channel In 2 Channel Driver Capability (8 Ohm at THD 1%)

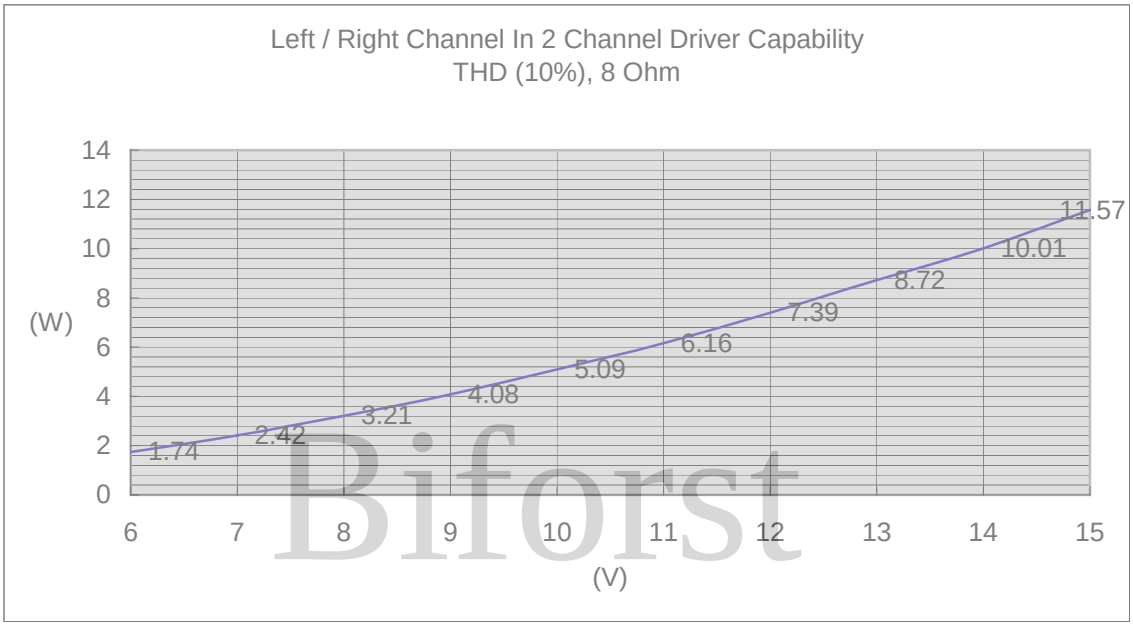


Figure 21. Left/Right Channel In 2 Channel Driver Capability (8 Ohm at THD 10%)

Operation Mode Select

BI30020B provides two control modes, Hardware Mode and I^{2}C Control Mode. When I2C_EN is set to Low, BI30020B will operate in Hardware Mode. When I2C_EN is set to High, BI30020B will then operate in I^{2}C Control Mode. Table 10 lists the configuration of I2C_EN.

Following chapters will detail explain how to control BI30020B thru I^{2}C in I^{2}C Control Mode and the functions of BI30020B's pins in Hardware Mode.

Table 10. I2C_EN Configuration

I2C_EN	BI30020B Control Mode
0	Hardware Mode
1	I^{2}C Control Mode

I^{2}C Control Mode

I^{2}C Bus Access Protocol

When I2C_EN of BI30020B is set to High, BI30020B will be operated in I^{2}C Control Mode and become a Slaver waiting for control signal from Master on I^{2}C Bus. In this mode, BI30020B will be controlled by internal register of BI30020B which are accessed through I^{2}C Bus.

There are two recognized Device Address in I^{2}C Bus of BI30020B. When DA0 pin is set to High, BI30020B's Device Address is predefined to **001_0111** (binary digit). When DA0 is set to Low, BI30020B's Device Address is predefined to **001_0110** (binary digit).

BI30020B supports two transfer speeds of Standard-Mode (100Kbits/s) and Fast-Mode (400Kbits/s) which are defined in Philips I^{2}C Bus Specification Version 2.1.

Figure 22 lists all I^{2}C Bus Access Protocols that BI30020B recognizes. There are two Write Protocols, **Byte Write** and **Multi-Byte Write**, are written data into BI30020B Control Register by I^{2}C Bus. There are four Read Protocols, **Current Address Read**, **Random Address Read**, **Sequential Current Read** and **Sequential Random Read**, are read from BI30020B Control Register by I^{2}C Bus.

Byte Write:	Beginning from START condition, first send the predefined Device Address and then the Sub-Address of Control Register. Secondly, input the data of 8-bits into Control Register. Finally, issue STOP condition to terminate the communication.
Multi-Byte Write:	Beginning from START condition, first send the predefined Device Address and then the Sub-Address of Control Register. Secondly, sequentially output every 8-bits data of Control Register. After each data is transferred, the internal address counter ofBI30020B will auto-increment and "roll-over" to starting address location

	and continue the auto-increment. Finally, issue STOP condition to terminate the communication.
Current Address Read:	Beginning from START condition, first send the predefined Device Address. Right after, BI30020B will send out the data addressed by the internal address counter. If BI30020B has never been accessed, Current Address Read will get data from location 0. Finally, issue STOP condition to terminate the communication.
Random Address Read:	A dummy Write is first performed to load the address into this address counter but without sending a STOP condition. Then, restart another START condition; send predefined Device Address. BI30020B will output the data in the specified Control Register. Finally, issue STOP condition to terminate the communication.
Sequential Current Read:	Similar to Current Address Read. However, BI30020B will output data in Control Register of consecutive byte addresses with the internal address counter auto-incremented after each byte output.
Sequential Random Read:	Similar to Random Address Read. However, BI30020B will output data in Control Register of consecutive byte addresses with the internal address counter auto-incremented after each byte output

Figure 23 lists the Timing Diagram of I^2C Bus. For more information of I^2C Bus, please refer to Philips Semiconductors “The I^2C-bus specification Version 2.1” for detail explanation.

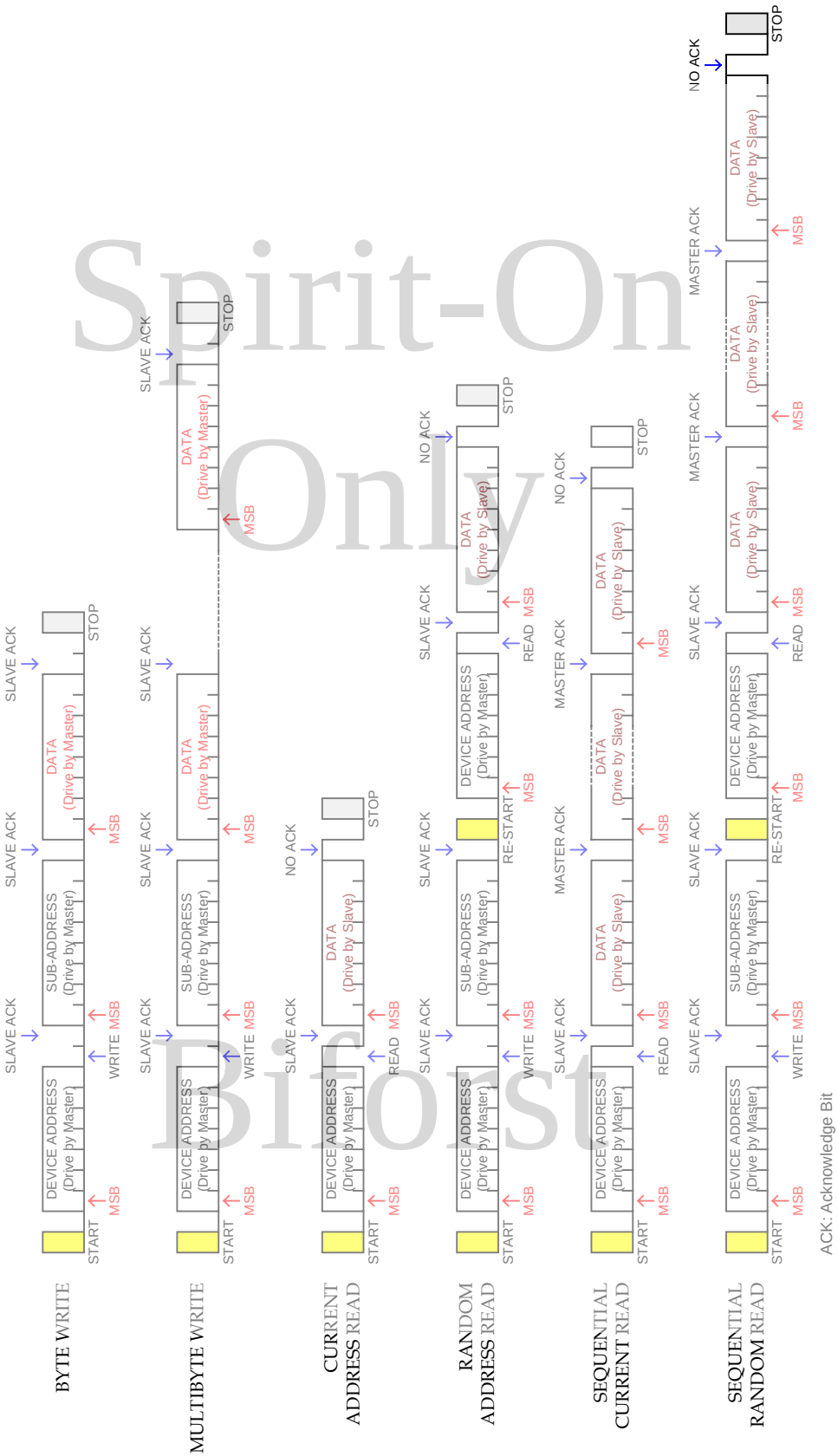
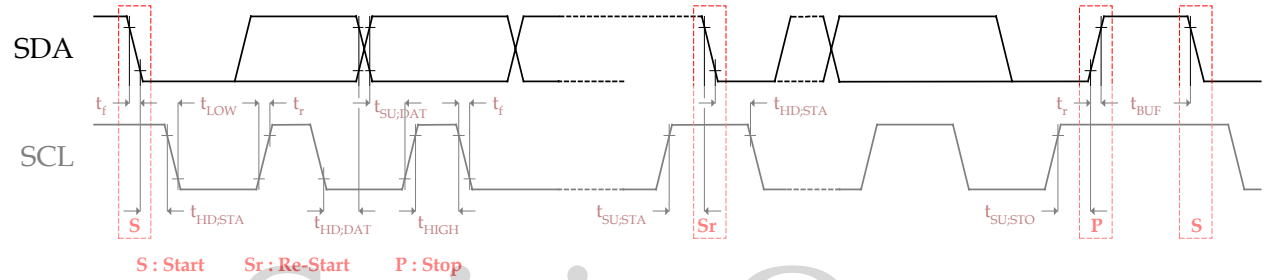


Figure 22. BI30020B I²C Bus Access Protocol



PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	µs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data set-up time	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	$20 + 0.1C_b$	300	ns
Fall time of both SDA and SCL signals	t_f	-	300	$20 + 0.1C_b$	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	-	$0.2V_{DD}$	-	V

Figure 23. I²C Bus Timing Diagram

BI30020B I²C Control Register Map

There are 12 8-Bits Control Registers inside BI30020B. The location of Control Register is 0 ~11 where 0 ~ 3 is to control the basic setup of BI30020B, 4 ~ 9 is to control the volume and mute, 10 is to control the adjustment of Balance and 11 is to control the adjustment of Treble and Bass. Figure 24 lists the Control Register Map inside BI30020B. The following sections will detail illustrate the setups

by location of Control Register consequently.

Sub-Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0			DVD_VOL_EN_B	CLIP_EN_B				CH_CONFIG_SEL
1			WORD_SEL_1	WORD_SEL_0	SCLK_POL	FSYNC_POL	MODE_SEL_1	MODE_SEL_0
2			FILT_SEL	PHASE	SEL_XF_3	SEL_XF_2	SEL_XF_1	SEL_XF_0
3	D_AMP_EN							
4				MAIN_VOL_C_4	MAIN_VOL_C_3	MAIN_VOL_C_2	MAIN_VOL_C_1	MAIN_VOL_C_0
5				MAIN_VOL_4	MAIN_VOL_3	MAIN_VOL_2	MAIN_VOL_1	MAIN_VOL_0
6				SUB_VOL_C_4	SUB_VOL_C_3	SUB_VOL_C_2	SUB_VOL_C_1	SUB_VOL_C_0
7				SUB_VOL_4	SUB_VOL_3	SUB_VOL_2	SUB_VOL_1	SUB_VOL_0
8	INC_DEC_SEL			MASTER_VOL_4	MASTER_VOL_3	MASTER_VOL_2	MASTER_VOL_1	MASTER_VOL_0
9						MUTE_ALL	SUB_MUTE	MAIN_MUTE
10					BALANCE_C_3	BALANCE_C_2	BALANCE_C_1	BALANCE_C_0
11	BASS_C_3	BASS_C_2	BASS_C_1	BASS_C_0	TREBLE_C_3	TREBLE_C_2	TREBLE_C_1	TREBLE_C_0

Figure 24. BI30020B I²C Control Register Map

BI30020B Control Register Address 0

BI30020B Control Register Address 0				
Bit	**Read/ Write**	**Function Description**	**When Pin I2C_EN = 1 Initial Value**	**When Pin I2C_EN = 0 Initial Value**
0	R/W	Channel Configure Select	0	Pin “CH_CONFIG_SEL”
1	R	Reserve	0	0
2	R	Reserve	0	0
3	R	Reserve	0	0
4	R/W	Anti-Clipping Enable	0	Pin “CLIP_EN_B”
5	R/W	Volume Boost Enable	0	Pin “DVD_VOL_EN_B”
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I2C Control Mode：**

- Channel Configure Select (Address 0 Bit 0) is to determine BI30020B’s operation in 2 Channel or 2.1 Channel. Table 11 lists the setup. Table 11 also lists the corresponding the output pins of Left/Right/Sub-Woofer Channel in 2.1/2 Channel.
- Anti-Clipping Enable (Address 0 Bit 4) is to control BI30020B’s internal Anti-Clipping circuit

enable. When Address 0 Bit 4 is set to Low, Anti-Clipping circuit will be disable and allow the wow effect. When Address 0 Bit 4 is set to High, Anti-Clipping circuit will be enable and automatically limit the signal not to distort. Table 12 lists the setup.

- Volume Boost Enable (Address 0 Bit 5) is to determine if BI30020B double output of the volume. When Address Bit 5 is set to Low, BI30020B will output double volume of current setting. When Address Bit 5 is set to High, BI30020B will output volume of current setting. Table 13 lists the setup.

- **Hardware Mode：**
- Channel Configure Select (Address 0 Bit 0) is to setup via CH_CONFIG_SEL.
- Anti-Clipping Enable (Address 0 Bit 4) is to setup via CLIP_EN_B.
- Volume Boost Enable (Address 0 Bit 5) is to setup via DVD_VOL_EN_B.

Table 11. Channel Configure Select (Address 0 Bit 0)

Address 0 Bit 0	Channel Configure Select	Left Channel Pin Map	Right Channel Pin Map	Sub-Woofer Channel Pin Map
0	2.1 Channel	ALOUTP & ALOUTN	AROUTP & AROUTN	BROUTP & BROUTN & BLOUTN & BLOUTP
1	2 Channel	AROUTP & AROUTN & ALOUTP & ALOUTN	BROUTP & BROUTN & BLOUTN & BLOUTP	

Table 12. Anti-Clipping Enable (Address 0 Bit 4)

Address 0 Bit 4	Anti-Clipping Enable
0	Disable
1	Enable

Table 13. Volume Boost Enable (Address 0 Bit 5)

Address 0 Bit 5	Volume Boost Enable
0	Enable
1	Disable

BI30020B Control Register Address 1

BI30020B Control Register Address 1				
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value
0	R/W	Digital Audio Data Format Select 0	0	Pin “MODE_SEL_0”
1	R/W	Digital Audio Data Format Select 1	0	Pin “MODE_SEL_1”
2	R/W	Digital Audio Data L/R Frame Select	0	Pin “FSYNC_POL”
3	R/W	Digital Audio Data Latch Clock Select	0	Pin “SCLK_POL”
4	R/W	Digital Audio Data Word Select 0	0	Pin “WORD_SEL_0”
5	R/W	Digital Audio Data Word Select 1	0	Pin “WORD_SEL_1”
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I^2C Control Mode：**

- Digital Audio Data Format Select 0~1 (Address 1 Bit 0~1) is to select the input format of Digital Audio Data. Table 14 lists the setup. BI30020B supports 3 input formats of I^2S, Left Justified and Right Justified.
- Digital Audio Data Left/Right Frame Select (Address 1 Bit 2) is to input or output FSYNC_IN /FSYNC_OUT signal of High or Low and the input Digital Audio Data of SDATA_IN is for Left or Right Channel in the time frame. Table 15 lists the setup. When Digital Audio Data Left/Right Frame Select (Address 1 Bit 2) is set to High, the data input to Right Channel is at High of FSYNC_IN/FSYNC_OUT and the data input to Left Channel is at Low of FSYNC_IN/FSYNC_ OUT. Besides, when Digital Audio Data Left/Right Frame Select (Address 1 Bit 2) is set to Low, the data input to Left Channel is at High of FSYNC_IN/FSYNC_OUT and the data input to Right Channel is at Low of FSYNC_IN/FSYNC_ OUT.
- Digital Audio Data Latch Clock Select (Address 1 Bit 3) is to determine the latch of Audio Data Clock via SCLK_IN/SCLK_ OUT. Table 16 lists the setup, which can use SCLK_ IN/SCLK_OUT to latch Audio Data by Rising or Falling Edge.
- Digital Audio Data Word Select 0~1 (Address 1 Bit 4~5) is to set up the input Word Length of Right-Justified in 24/20/18/16 Bits. Table 17 lists the setup. However, when in I^2S and Left-Justified, BI30020B will automatically adjust the data Word Length not to be controlled by

these 2 Bits.

- Figure 25 shows the setups and Digital Audio Data Input Formats that BI30020B can support. User may find out the correct setting from this figure.

- **Hardware Mode：**

- Digital Audio Data Format Select 0~1 (Address 1 Bit 0~1) is to setup via MODE_ SEL_0 and MODE_SEL_1.
- Digital Audio Data Left/Right Frame Select (Address 1 Bit 2) is to setup via FSYNC_POL.
- Digital Audio Data Latch Clock Select (Address 1 Bit 3) is to setup via SCLK_POL.
- Digital Audio Data Word Select 0~1 (Address 1 Bit 4~5) is to setup via WORD_ SEL_0 and WORD_SEL_1.

Table 14. Digital Audio Data Input Format Select (Address 1 Bit 0 ~ 1)

Address 1 Bit 1	Address 1 Bit 0	Digital Audio Data Input Format Select
0	0	I^2S Audio Data Format Input
0	1	
1	0	Left-Justified Audio Data Format Input
1	1	Right-Justified Audio Data Format Input

Table 15. Digital Audio Data Left/Right Frame Select (Address 1 Bit 2)

Address 1 Bit 2	Digital Audio Data Left/Right Frame Select
0	FSYNC_IN/OUT = 1 : Left Channel, FSYNC_IN/OUT = 0 : Right Channel
1	FSYNC_IN/OUT = 1 : Right Channel, FSYNC_IN/OUT = 0 : Left Channel

Table 16. Digital Audio Data Latch Clock Select (Address 1 Bit 3)

Address 1 Bit 3	Digital Audio Data Latch Clock Select
0	Falling Edge Latch Audio Data
1	Rising Edge Latch Audio Data

Table 17. Digital Audio Data Input Length Select in Right-Justified Mode Only

(Address 1 Bit 4 ~ 5)

Address 1 Bit 5	Address 1 Bit 4	Serial Audio Data Input Length Select
0	0	24-bits
0	1	20-bits
1	0	18-bits
1	1	16-bits

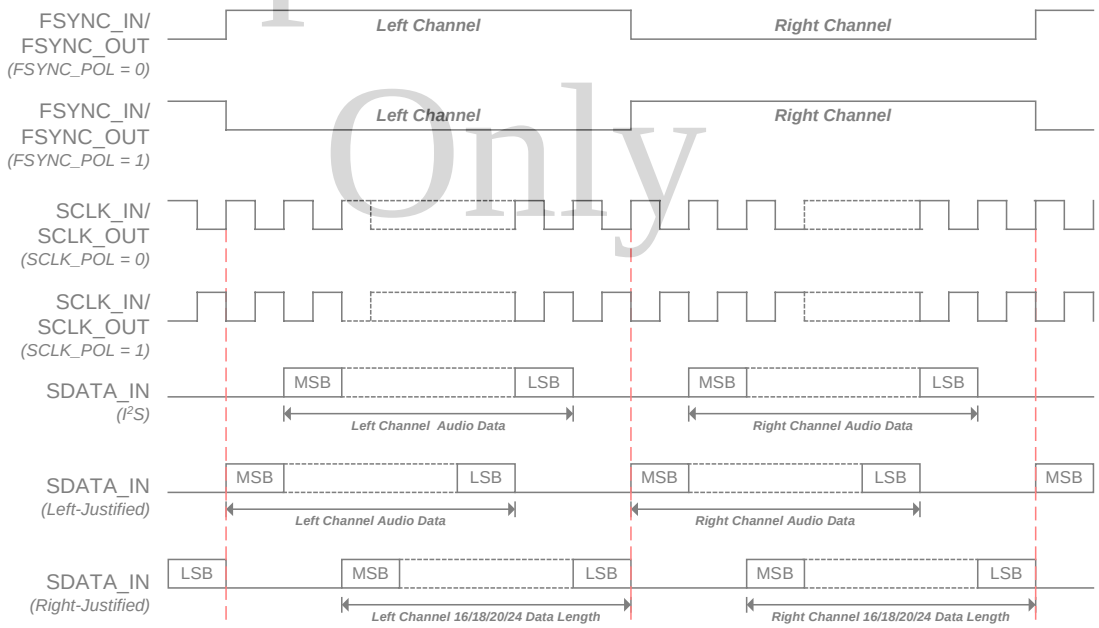


Figure 25. Digital Audio Data Input Format

BI30020B Control Register Address 2

BI30020B Control Register Address 2				
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value
0	R/W	Crossover Frequency Select 0	0	Pin “SEL_XF_0”
1	R/W	Crossover Frequency Select 1	0	Pin “SEL_XF_1”
2	R/W	Crossover Frequency Select 2	0	Pin “SEL_XF_2”
3	R/W	Crossover Frequency Select 3	0	Pin “SEL_XF_3”
4	R/W	Sub-Woofer Output Phase Select	0	Pin “PHASE”
5	R/W	Main Channel HPF Bypass	0	Pin “FILT_SEL”
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I²C Control Mode：**

- Crossover Frequency Select 0~3 (Address 2 Bit 0~3) is to determine the Crossover Frequency. Table 18 lists the setup. BI30020B can select up to 14 Crossover Frequency ranging from 150Hz to 800Hz by step of 50Hz. Sub-Woofer Channel will output the frequency lower than setup and Main Channel output the higher frequency.
- Sub-Woofer Output Phase Select (Address 2 Bit 4) is to determine the output phase of Sub-Woofer. Table 19 lists the setup to output 0 degree or 180 degree.
- Main Channel HPF Bypass (Address 2 Bit 5) is to determine the output of Main Channel pass through High Pass Filter or not. Table 18 lists the setup. When the setup is Low, Main Channel’s output will pass through High Pass Filter. The Crossover Frequency of High Pass Filter is controlled by Crossover Frequency Select 0~3 (Address 2 Bit 0~3). When the setup is High, Main Channel will output the full range frequency.

- **Hardware Mode：**

- Crossover Frequency Select 0~3 (Address 2 Bit 0~3) is to setup via SEL_XF_0 ~ SEL_XF_3.
- Sub-Woofer Output Phase Select (Address 2 Bit 4) is to setup via PHASE.
- Main Channel HPF Bypass (Address 2 Bit 5) is to setup via FILT_SEL.

Table 18. Cross Over Frequency Select

Address 2 Bit5	Address 2 Bit3	Address 2 Bit2	Address 2 Bit1	Address 2 Bit0	Left/Right Main Channel Output Frequency Range	Sub-Woofer Channel Output Frequency Range
0	0	0	0	0	> 150 Hz	< 150 Hz
	0	0	0	1	> 200 Hz	< 200 Hz
	0	0	1	0	> 250 Hz	< 250 Hz
	0	0	1	1	> 300 Hz	< 300 Hz
	0	1	0	0	> 350Hz	< 350Hz
	0	1	0	1	> 400 Hz	< 400 Hz
	0	1	1	0	> 450 Hz	< 450 Hz
	0	1	1	1	> 500 Hz	< 500 Hz
	1	0	0	0	> 550 Hz	< 550 Hz
	1	0	0	1	> 600 Hz	< 600 Hz
	1	0	1	0	> 650 Hz	< 650 Hz
	1	0	1	1	> 700 Hz	< 700 Hz
	1	1	0	0	> 750 Hz	< 750 Hz
	1	1	0	1	> 800 Hz	< 800 Hz
	1	1	1	0	> 800 Hz	< 800 Hz
	1	1	1	1	> 800 Hz	< 800 Hz
1	0	0	0	0	Full Range	< 150 Hz
	0	0	0	1		< 200 Hz
	0	0	1	0		< 250 Hz
	0	0	1	1		< 300 Hz
	0	1	0	0		< 350Hz
	0	1	0	1		< 400 Hz
	0	1	1	0		< 450 Hz
	0	1	1	1		< 500 Hz
	1	0	0	0		< 550 Hz
	1	0	0	1		< 600 Hz
	1	0	1	0		< 650 Hz
	1	0	1	1		< 700 Hz
	1	1	0	0		< 750 Hz
	1	1	0	1		< 800 Hz
	1	1	1	0		< 800 Hz
	1	1	1	1		< 800 Hz

Table 19. Sub-Woofer Output Phase Select (Address 2 Bit4)

Address 2 Bit 4	Sub-Woofer Output Phase Select
0	0 Degree
1	180 Degree

BI30020B Control Register Address 3

BI30020B Control Register Address 3				
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value
0	R	Reserve	0	0
1	R	Reserve	0	0
2	R	Reserve	0	0
3	R	Reserve	0	0
4	R	Reserve	0	0
5	R	Reserve	0	0
6	R	Reserve	0	0
7	R/W	Digital Amplifier Enable	0	Depend On Pin “ERF” & “ERF_INV_EN”

- **I^2C Control Mode：**

- Digital Amplifier Enable (Address 3 Bit 7) is to control the enable/disable of Digital Amplifier where Table 20 lists the setup. When the setup is Low, Digital Amplifier is disabled. When the setup is High, Digital Amplifier is enabled. Please notice that BI30020B is in I^2C Control Mode, the external pin of ERF_INV_EN has to set to Low or Digital Amplifier could not be enabled.

- **Hardware Mode：**

- Digital Amplifier Enable (Address 3 Bit 7) is to setup via the relation of ERF and ERF_INV_EN to turn-on/off the Digital Amplifier.

Table 20. Digital Amplifier Enable (Address 3 Bit7)

Address 3 Bit 7	Digital Amplifier Enable
0	Disable
1	Enable

BI30020B Control Register Address 4

BI30020B Control Register Address 4				
Bit	**Read/ Write**	**Function Description**	**When Pin I2C_EN = 1 Initial Value**	**When Pin I2C_EN = 0 Initial Value**
0	R/W	Main Channel Vol. Control bit 0	Initial Value Depend On Pin "VOL_VALUE_SEL_0" & "VOL_VALUE_SEL_1"	
1	R/W	Main Channel Vol. Control bit 1		
2	R/W	Main Channel Vol. Control bit 2		
3	R/W	Main Channel Vol. Control bit 3		
4	R/W	Main Channel Vol. Control bit 4		
5	R	Reserve	0	0
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I²C Control Mode：**

- Main Channel Volume Control (Address 4 Bit 0~4) is to control the volume of Main Channel. The value is set from 0 (Mute) to 31 (Max.). The initial value of Main Channel Volume Control will be reset via the external pins of VOL_VALUE_SEL_0 and VOL_VALUE_SEL _1. Table 21 lists the setup. BI30020B can be set for 4 initial volume setups of 0, 9, 16 and 31.

- **Hardware Mode：**

- Main Channel Volume Control (Address 4 Bit 0~4) is controlled via external pins of VOL_INC, VOL_ DEC and VOL_ADJ_SEL. The initial value of Main Channel Volume Control will be reset via VOL_VALUE_SEL_0 and VOL_VALUE_SEL _1.

Table 21. Initial Volume Setting After Reset

VOL_VALUE_SEL_1	VOL_VALUE_SEL_0	Main Channel Volume Control				
		Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	0	0	1
1	1	0	0	0	0	0

BI30020B Control Register Address 5

BI30020B Control Register Address 5				
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value
0	R	Main Channel Vol. Bit 0	Initial Value Depend On Pin "VOL_VALUE_SEL_0" & "VOL_VALUE_SEL_1"	
1	R	Main Channel Vol. Bit 1		
2	R	Main Channel Vol. Bit 2		
3	R	Main Channel Vol. Bit 3		
4	R	Main Channel Vol. Bit 4		
5	R	Reserve	0	0
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I²C Control Mode：**

- Main Channel Volume (Address 5 Bit 0~4) stores the final value of the plus/minus of Main Channel Volume Control (Address 4 Bit 0~4) and Master Volume Control (Address 8 Bit 0~ 4). This value will be the actual volume output of Main Channel while the initial value will be reset via VOL_VALUE_SEL_0 and VOL_VALUE_SEL _1. Table 21 lists the initial value setup. Besides, the Main Channel Volume can only read not to write.

BI30020B Control Register Address 6

BI30020B Control Register Address 6				
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value
0	R/W	Sub-Woofer Vol. Control bit 0	Depend On Pin "VOL_VALUE_SEL_0" & "VOL_VALUE_SEL_1"	
1	R/W	Sub-Woofer Vol. Control bit 1		
2	R/W	Sub-Woofer Vol. Control bit 2		
3	R/W	Sub-Woofer Vol. Control bit 3		
4	R/W	Sub-Woofer Vol. Control bit 4		
5	R	Reserve	0	0
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I²C Control Mode：**

- Sub-Woofer Volume Control (Address 6 Bit 0~4) is to control the volume of Sub-Woofer Channel.

The value is set from 0 (Mute) to 31 (Max.). The initial value of Sub-Woofer Channel Volume Control will be reset via the external pins of VOL_VALUE_SEL_0 and VOL_VALUE_SEL _1. Table 21 lists the setup. BI30020B can be set for 4 initial volume setups of 0, 9, 16 and 31.

- **Hardware Mode：**

- Sub-Woofer Volume Control (Address 4 Bit 0~4) is controlled via VOL_INC, VOL_ DEC and VOL_ADJ_SEL. The initial value will be reset via the external pins of VOL_VALUE_SEL_0 and VOL_VALUE_SEL _1

BI30020B Control Register Address 7

BI30020B Control Register Address 7				
Bit	**Read/ Write**	**Function Description**	**When Pin I2C_EN = 1 Initial Value**	**When Pin I2C_EN = 0 Initial Value**
0	R	Sub-Woofer Vol. Bit 0	Depend On Pin “VOL_VALUE_SEL_0” & “VOL_VALUE_SEL_1”	
1	R	Sub-Woofer Vol. Bit 1		
2	R	Sub-Woofer Vol. Bit 2		
3	R	Sub-Woofer Vol. Bit 3		
4	R	Sub-Woofer Vol. Bit 4		
5	R	Reserve	0	0
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I^2C Control Mode：**

- Sub-Woofer Volume (Address 7 Bit 0~4) stores the final value of the plus/minus Sub-Woofer Volume Control (Address 4 Bit 0~4) and Master Volume Control (Address 8 Bit 0~ 4). This value will be the actual volume output of Sub-Woofer Channel while the initial value will be reset via VOL_VALUE_SEL_0 and VOL_VALUE_SEL _1. Table 21 lists the initial value setup. Besides, the Sub-Woofer Channel Volume can only read not to write.

BI30020B Control Register Address 8

BI30020B Control Register Address 8				
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value
0	R/W	Master Volume Control bit 0	0	0
1	R/W	Master Volume Control bit 1	0	0
2	R/W	Master Volume Control bit 2	0	0
3	R/W	Master Volume Control bit 3	0	0
4	R/W	Master Volume Control bit 4	0	0
5	R	Reserve	0	0
6	R	Reserve	0	0
7	R/W	Increase / Decrease Control	0	0

- **I^2C Control Mode：**

- Master Volume Control (Address 8 Bit 0~4) is to set the dependent volume value of Main Channel and Sub-Woofer Channel. The value is from 0 to 31.
- Increases/Decrease Control (Address 8 Bit 7) is to concurrent increase/decrease volume value of Main Channel and Sub-Woofer Channel. Table 22 lists the setup. While this Bit is set to Low, it is to concurrent increase the volume value of Main Channel and Sub-Woofer Channel. While this Bit is set to High, it is to concurrent decrease the volume value of Main Channel and Sub-Woofer Channel.

Table 22. Increase/Decrease Control (Address 8 Bit)

Address 8 Bit 7	Increase / Decrease Control
0	Increase
1	Decrease

BI30020B Control Register Address 9

BI30020B Control Register Address 9				
Bit	**Read/ Write**	**Function Description**	**When Pin I2C_EN = 1 Initial Value**	**When Pin I2C_EN = 0 Initial Value**
0	R/W	Main Channel Mute Enable	0	0
1	R/W	Sub-Woofer Mute Enable	0	0
2	R/W	All Channel Mute Enable	0	0 *(MUT_ALL)*
3	R	Reserve	0	0
4	R	Reserve	0	0
5	R	Reserve	0	0
6	R	Reserve	0	0
7	R	Reserve	0	0

- **I²C Control Mode：**

- Main Channel Mute Enable (Address 9 Bit 0) is to control Mute of Main Channel.
- Sub-Woofer Mute Enable (Address 9 Bit 1) is to control Mute of Sub-Woofer Channel.
- All Channel Mute Enable (Address 9 Bit 2) is to control Mute of Main Channel and Sub-Woofer Channel in the same time. Table 23 lists the configurations of Main Channel Mute Enable, Sub-Woofer Mute Enable and All Channel Mute Enable. When it is set to High, Mute is enabled for the corresponding Channel. When it is set to Low, Mute is then disabled.

- **Hardware Mode：**

- To change the setup of All Channel Mute Enable (Address 9 Bit 2) is only via the external pin of MUTE_ALL when Main Channel Mute Enable (Address 9 Bit 0) and Sub-Woofer Mute Enable (Address 9 Bit 1) can be set to Low.

Table 23. Mute Control (Address 9 Bit 0 ~ 2)

Address 9 Bit 0 ~ 2	Mute Function Status
0	Mute Disable
1	Mute Enable

BI30020B Control Register Address 10

BI30020B Control Register Address 10					
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value	
0	R	Balance Control bit 0	0	0	*Control By Pin "BALANCE_RIGHT" & "BALANCE_CENTER" & "BALANCE_LEFT"*
1	R	Balance Control bit 1	0	0	
2	R	Balance Control bit 2	0	0	
3	R	Balance Control bit 3	0	0	
4	R	Reserve	0	0	
5	R	Reserve	0	0	
6	R	Reserve	0	0	
7	R	Reserve	0	0	

- **I²C Control Mode：**

- Balance Control (Address 10 Bit 0~3) is to control the function of Channel Balance. Bit3 is to choose Left or Right Channel to decrease the volume. When Bit3 is set to High, the Left Channel will be decreased the volume gradually but not affect Right Channel. When Bit3 is set to Low, the Right Channel will be decreased the volume gradually but not affect Left Channel. Bit0 ~ Bit2 is to set the level to decrease the volume of Left or Right Channel. It is divided into 8 levels ranging from 100% to 0% (Mute). Table 24 is the configuration setup of Channel Balance.

- **Hardware Mode：**

- To change the setup of Balance Control (Address 10 Bit 0~3) is only via the external pins of BALANCE_RIGHT, BALANCE_CENTER and BALANCE_LEFT.

Table 24. Balance Control (Address 10 Bit 0 ~ 3)

Address 10				Left Channel Output	Right Channel Output
Bit3	Bit2	Bit1	Bit0	Level	Level
0	1	1	1	100%	0% (Mute)
0	1	1	0	100%	1.5625%
0	1	0	1	100%	3.125%
0	1	0	0	100%	6.25%
0	0	1	1	100%	12.5%
0	0	1	0	100%	25%
0	0	0	1	100%	50%
0	0	0	0	100%	100%
1	0	0	0		
0	0	0	0	100%	100%
1	0	0	0		
1	0	0	1	50%	100%
1	0	1	0	25%	100%
1	0	1	1	12.5%	100%
1	1	0	0	6.25%	100%
1	1	0	1	3.125%	100%
1	1	1	0	1.5625%	100%
1	1	1	1	0% (Mute)	100%

BI30020B Control Register Address 11

BI30020B Control Register Address 11					
Bit	Read/ Write	Function Description	When Pin I2C_EN = 1 Initial Value	When Pin I2C_EN = 0 Initial Value	
0	R	Treble Control bit 0	1	1	*Control By Pin "TRE_BASS_SEL" & "TRE_BASS_INC" & "TRE_BASS_DEC"*
1	R	Treble Control bit 1	1	1	
2	R	Treble Control bit 2	1	1	
3	R	Treble Control bit 2	0	0	
4	R	Bass Control bit 0	1	1	*Control By Pin "TRE_BASS_SEL" & "TRE_BASS_INC" & "TRE_BASS_DEC"*
5	R	Bass Control bit 1	1	1	
6	R	Bass Control bit 2	0	0	
7	R	Bass Control bit 2	0	0	

- **I^2C Control Mode：**

- Treble Control (Address 11 Bit 0~3) is to control the Level of Treble. Table 25 lists the setup.
- Bass Control (Address 11 Bit 4~7) is to control the Level of Bass. Table 26 lists the setup.
- In addition, when Channel Configure Select (Address 0 Bit 0) is set to High, BI30020B will operate in 2 Channel. If Main Channel HPF Bypass (Address 2 Bit 5) is also set to High, there will be no control to Treble and Bass. However, if Main Channel HPF Bypass (Address 2 Bit 5) is set to Low, there will be controls to both Treble and Bass.

- **Hardware Mode：**

- To change the setups of Treble Control (Address 11 Bit 0~3) and Bass Control (Address 11 Bit 4~7) are only via external pins of TRE_BASS_SEL, TRE_BASS_INC and TRE_BASS_DEC.

Table 25. Treble Control (Address 11 Bit 0 ~ 3)

Address 11				Output Treble Level
Bit3	Bit2	Bit1	Bit0	
0	0	0	0	50%
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	62.5%
0	1	0	1	75%
0	1	1	0	87.5%
0	1	1	1	100%
1	0	0	0	112.5
1	0	0	1	125%
1	0	1	0	137.5%
1	0	1	1	150%
1	1	0	0	162.5%
1	1	0	1	175%
1	1	1	0	187.5%
1	1	1	1	200%

Table 26. Bass Control (Address 11 Bit 4 ~ 7)

Address 11				Output Bass Level
Bit7	Bit6	Bit5	Bit4	
0	0	0	0	25%
0	0	0	1	50%
0	0	1	0	75%
0	0	1	1	100%
0	1	0	0	125%
0	1	0	1	150%
0	1	1	0	175%
0	1	1	1	200%
1	0	0	0	225%
1	0	0	1	250%
1	0	1	0	275%
1	0	1	1	300%
1	1	0	0	325%
1	1	0	1	350%
1	1	1	0	375%
1	1	1	1	400%

Hardware Control Mode

Digital Audio Data Input Format Select

BI30020B is to drive Speaker just by inputting the Digital Audio Data. It supports the PCM Format from CD player, DVD decoded chip or DSP decoder such as (Portable MP3 Player).

BI30020B can receive Digital Audio Data input format by setting the external pins of MODE_SEL_1, MODE_SEL_0, FSYNC_POL, SCLK_POL, WORD_SEL_1 and WORD_SEL_0. MODE_SEL_1 and MODE_SEL_0 are to set MSB starting position of Digital Audio Data. BI30020B supports I^2S, Left-Justified and Right-Justified. Table 27 illustrates the setup list. FSYNC_POL is to adjust Serial Audio Data Left/Right Frame and SCLK_POL is to select Audio Data Signal "SCLK_IN" Polarity. Table 28 and Table 29 are the lists.

Figure 26 illustrates how the actual receiving data format relates to the pin setup. While in Left-Justified Mode, each Audio Data's MSB position is left aligned to Rising/Falling of FSYNC_IN/FSYNC_OUT's signal. While in Right-Justified Mode, each Audio Data's LSB position is right aligned to Rising/Falling of FSYNC_IN/FSYNC_OUT's signal. Compared to Left-Justified Mode,

one Clock Cycle shift of SCLK_IN is occurred for each Audio Data's MSB position under I^2S Mode.

When BI30020B is set to I^2S and Left-Justified Modes, BI30020B can automatically catch the data following the signal change of FSYNC_IN/FSYNC_OUT and SCLK_IN/SCLK_OUT. However, when BI30020B is set to Right-Justified Mode, it is required to setup the word length of the input data format or BI30020B cannot catch the accurate data. WORD_SEL_0 and WORD_SEL_1 are to set the audio data word length. BI30020B can accept 4 types of length in 24/20/18/16-bits. Table 30 lists the setup. While the setup is greater than actual input data word length, BI30020B will automatically stop receiving the data internally.

Table 27. Digital Audio Data Input Format Select

MODE_SEL_1	MODE_SEL_0	Digital Audio Data Input Select
0	0	I^2S Audio Data Format Input
0	1	
1	0	Left-Justified Audio Data Format Input
1	1	Right-Justified Audio Data Format Input

Table 28. Digital Audio Data Left/Right Frame Select

FSYNC_POL	Digital Audio Data Left/Right Frame Select
0	FSYNC_IN = 1 : Left Channel / FSYNC_IN = 0 : Right Channel
1	FSYNC_IN = 1 : Right Channel / FSYNC_IN = 0 : Left Channel

Table 29. Digital Audio Data Latch Clock Select

SCLK_POL	Digital Audio Data Latch Clock Select
0	Falling Edge Latch Audio Data
1	Rising Edge Latch Audio Data

Table 30. Digital Audio Data Input Length Select (Right-Justified Mode Only)

WORD_SEL_1	WORD_SEL_0	Digital Audio Data Input Length Select
0	0	24-bits
0	1	20-bits
1	0	18-bits
1	1	16-bits

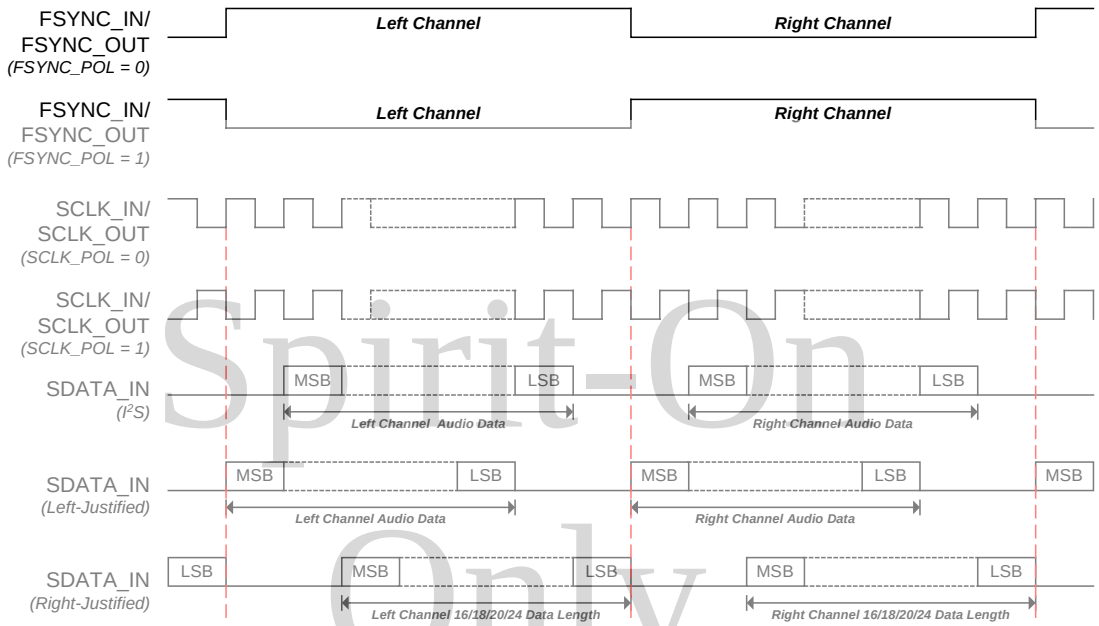


Figure 26 Digital Audio Data Input Format

Cross Over Frequency Configuration

BI30020B is embedded an Electronic Digital Crossover. By setting the external pins of SEL_XF_0, SEL_XF_1, SEL_XF_2, and SEL_XF_3 to select the crossover frequency for output signals. In addition, by setting “FILT_SEL”, the Main Channel can be determined if the output signals pass through High Pass Filter or not. However, Sub-Woofer Channel will pass through Low Pass Filter.

Table 31 lists the Crossover Frequency setup for BI30020B. The frequency is ranging from 150Hz to 800Hz, and step in 50 Hz. For example, when SEL_XF_3 = 0, SEL_XF_2 = 1, SEL_XF_1 = 0, SEL_XF_0 = 1 and FILT_SEL = 0, BI30020B will only output the audio signal greater than 400 Hz to Main Channel and deliver the audio signal less than 400Hz to Sub-Woofer Channel. The setup of crossover frequency is determined by speaker’s characteristics, which requires the hearing test to decide the appropriate setting.

Table 31. Cross Over Frequency Select

FILT_SEL	SEL_XF_3	SEL_XF_2	SEL_XF_1	SEL_XF_0	Left/Right Main Channel Output Frequency Range	Sub-Woofer Channel Output Frequency Range
0	0	0	0	0	> 150 Hz	< 150 Hz
	0	0	0	1	> 200 Hz	< 200 Hz
	0	0	1	0	> 250 Hz	< 250 Hz
	0	0	1	1	> 300 Hz	< 300 Hz
	0	1	0	0	> 350Hz	< 350Hz
	0	1	0	1	> 400 Hz	< 400 Hz
	0	1	1	0	> 450 Hz	< 450 Hz
	0	1	1	1	> 500 Hz	< 500 Hz
	1	0	0	0	> 550 Hz	< 550 Hz
	1	0	0	1	> 600 Hz	< 600 Hz
	1	0	1	0	> 650 Hz	< 650 Hz
	1	0	1	1	> 700 Hz	< 700 Hz
	1	1	0	0	> 750 Hz	< 750 Hz
	1	1	0	1	> 800 Hz	< 800 Hz
	1	1	1	0	> 800 Hz	< 800 Hz
	1	1	1	1	> 800 Hz	< 800 Hz
1	0	0	0	0	Full Range	< 150 Hz
	0	0	0	1		< 200 Hz
	0	0	1	0		< 250 Hz
	0	0	1	1		< 300 Hz
	0	1	0	0		< 350Hz
	0	1	0	1		< 400 Hz
	0	1	1	0		< 450 Hz
	0	1	1	1		< 500 Hz
	1	0	0	0		< 550 Hz
	1	0	0	1		< 600 Hz
	1	0	1	0		< 650 Hz
	1	0	1	1		< 700 Hz
	1	1	0	0		< 750 Hz
	1	1	0	1		< 800 Hz
	1	1	1	0		< 800 Hz
	1	1	1	1		< 800 Hz

Phase Configuration

When BI30020B is set to 2.1 Channel, the output phase of Sub-Woofer Channel can be set through the external pin of PHASE. When PHASE is set to Low, Sub-Woofer Channel's output phase is 0 degree. While PHASE is set to High, Sub-Woofer Channel's outputs in reverse phase of 180 degree. Table 32 is the setup of PHASE.

Table 32. Phase Configuration

PHASE	Sub-Woofer Channel Output Phase Select
0	0 Degree
1	180 Degree

Power-On Initial Volume Configuration

In certain application, it is required to have volume output or mute output without adjusting volume right after power-on. Therefore, BI30020B provides the function to setup the initial volume value when power-on. The setup is via external pins of VOL_VALUE_SEL_0 and VOL_VALUE_SEL_1 to determine the initial volume value of Main Channel and Sub-Woofer Channel. There are 4 values for setup: 0 (Mute)、9、16 and 31 (Max.). Table 33 is the corresponding list for setup.

Table 33. BI30020B Initial Volume Configuration In Hardware Mode

VOL_VALUE_SEL_1	VOL_VALUE_SEL_0	Initial Volume Value	
		Left/Right Main Channel	Sub-Woofer Channel
0	0	31	
0	1	16	
1	0	9	
1	1	0 (Mute)	

Volume Control Configuration

BI30020B has 32-Level digital volume control individually for each Main Channel and Sub-Woofer Channel by setup pins of VOL_INC, VOL_DEC, and VOL_ADJ_SEL. It can also select if the volume control of Main Channel and Sub-Woofer Channel is dependent and independent adjustment. Further, BI30020B provides the LED output to indicate the volume adjustment of Main Channel and Sub-Woofer Channel.

VOL_INC, VOL_DEC and VOL_ADJ_SEL are to input Low Pulse to activate the action. Figure 27 is the Timing Diagram of input signal. The minimum Low Pulse is 600μs, and so is the interval. The application circuit is shown as Figure 28. The application circuit is use Switch as example to activate the action of VOL_INC, VOL_DEC and VOL_ADJ_SEL and use MAIN_VOL_ADJ_ LED and SUB_VOL_ADJ_LED to indicate the current status.

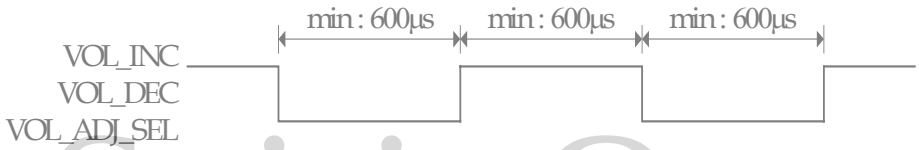


Figure 27. VOL_DEC、VOL_INC & VOL_ADJ_SEL Input Timing Diagram

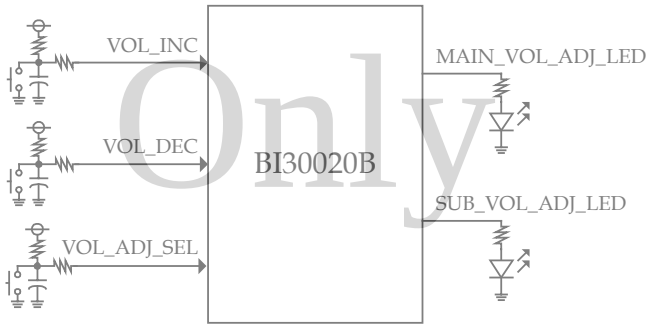


Figure 28. Volume Control & Volume Control Indication LED Application Circuit

VOL_INC is used for the increase of the volume and VOL_DEC for decrease of the volume. VOL_ADJ_SEL is thus to select the channel to control the volume. Table 34 lists relationship of output LED of MAIN_VOL_ADJ_LED/SUB_VOL_ADJ_LED and the continuous Low Pulse into VOL_ADJ_SEL. For example,

Case 1) To increase volume of Main Channel only – First, continuously activate VOL_ADJ_SEL until MAIN_VOL_ADJ_LED output to High, and SUB_VOL_ADJ_ LED to Low. Then, activate VOL_INC to increase the volume of Main Channel.

Case 2) To decrease volume of Sub-Woofer only – First, continuously activate VOL_ADJ_SEL until MAIN_VOL_ADJ_LED output to Low, and SUB_VOL_ADJ_ LED to High. Then, activate VOL_DEC to decrease the volume of Sub-Woofer Channel.

Case 3) To increase both volumes of Main Channel and Sub-Woofer – First, continuously activate VOL_ADJ_SEL until MAIN_VOL_ADJ_LED output to High, and SUB_VOL_ADJ_ LED to High. Then, activate VOL_INC to increase the volume of Main Channel and Sub-Woofer Channel.

Table 34. VOL_ADJ_SEL Configuration

VOL_ADJ_SEL	Main Channel Volume Adjust Enable MAIN_VOL_ADJ_LED	Sub-Woofer Channel Volume Adjust Enable SUB_VOL_ADJ_LED	Volume Control Status
Initial Value	1	1	Left/Right Main Channel & Sub-Woofer Channel Volume Control Together
Low Pulse (1)	1	0	Left/Right Main Channel Volume Control Only
Low Pulse (2)	0	1	Sub-Woofer Channel Volume Control Only
Low Pulse (3)	1	1	Left/Right Main Channel & Sub-Woofer Channel Volume Control Together

Volume Mute Configuration

BI30020B is triggered to mute all of the output via the external pin of MUTE_ALL. MUTE_ALL is to input Low Pulse to activate the action. Figure 29 illustrates the Timing Diagram of input signal. The minimum low pulse is 600μs, and so is the interval. The application circuit is shown as Figure 30. The application circuit is use Switch as example to activate the action of MUTE_ALL and use MAIN_MUTE_ LED and SUB_MUTE_LED to indicate the current status.

Table 35 lists the relationship of output LED of MAIN_MUTE_LED/SUB_MUTE_LED and the continuous Low Pulse into MAIN_MUTE, SUB_ MUTE and MUTE_ALL. Further, when mute function is activated and then deactivated, the previous volume value will not be changed.

Figure 29. MUTE_ALL Input Timing Diagram

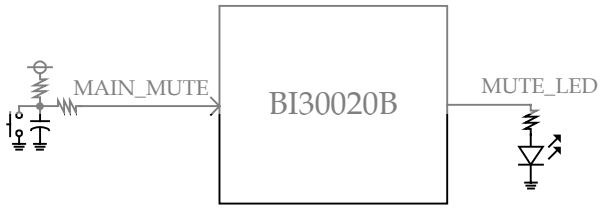


Figure 30. MUTE_ALL & Mute Indication LED Application Circuit

Table 35. MUTE_ALL Configuration

MUTE_ALL	MUTE_LED	Mute Control Status
Initial Value	0	All Channel Mute Disable
Low Pulse (1)	1	All Channel Mute Enable
Low Pulse (2)	0	All Channel Mute Disable

ERF Configuration

ERF is to control the emergency shut down of BI30020B and ERF_INV_EN is to trigger the selection. Table 36 lists the setup. Assume ERF_INV_EN is set to Low while ERF is set to High, BI30020B will emergency shut down the internal Digital Amplifier and set all of the Speaker Drivers to Low. Only after ERF input back to Low, BI30020B's internal Digital Amplifier will re-operate. Also, when ERF is activated, BI30020B will remain the internal setting of volume but will not be clear as the initial volume values setup.

Table 36. ERF & ERF_INV_EN Configuration

ERF_INV_EN	ERF	Error Flag Input
0	0	BI30020B Digital Amplifier Normal Operation
0	1	BI30020B Digital Amplifier Shut-Down, All Driver Output Low Level
1	0	BI30020B Digital Amplifier Shut-Down, All Driver Output Low Level
1	1	BI30020B Digital Amplifier Normal Operation

Volume Boost & Anti-Clipping Enable Configuration

BI30020B provides Volume Boost and Anti-Clipping functions through external pin of DVD_VOL_EN_B to control enable/disable of Volume Boost and CLIP_EN_B for Anti-Clipping. The setups are listed in Table 37 and 38.

The function of Volume Boost is to double the output volumes of BI30020B. For example, if volume set to 9 and DVD_VOL_EN_B is set to High, BI30020B will actually output the volume of 9. When DVD_VOL_EN_B is set to Low, BI30020B will actually output the volume of 18 to enhance the auditory sensation.

The function of Anti-Clipping is to control the wow effect when output signal is over the maximum amplitude. For example, when CLIP_EN_B is set to High, BI30020B will enable the internal Anti-Clipping circuit to automatically control and decrease the wow effect to eliminate sound of clip. When CLIP_EN_B is set to Low, BI30020B will disable the internal Anti-Clipping circuit to allow the wow effect and hear the sound of clip. Therefore, it is highly recommended to set both Low for DVD_VOL_EN_B and CLIP_EN_B when play DVD Movie, and set both to High when listening to CD for better performance of auditory sensation.

Table 37. DVD_VOL_EN_B Configuration

DVD_VOL_EN_B	Volume Boost Enable
0	Enable
1	Disable

Table 38. CLIP_EN_B Configuration

CLIP_EN_B	Anti-Clipping Enable
0	Disable
1	Enable

Balance Control

BI30020B provides the function of Balance Control via the external pins of BALANCE_RIGHT, BALANCE_CENTER and BALANCE_LEFT to control the volume level of Left and Right Channels. To input Low Pulse will activate the actions of BALANCE_RIGHT, BALANCE_CENTER and BALANCE_LEFT. Figure 31 illustrates the Timing Diagram of input signal. The minimum low pulse is 600μs, and so is the interval.

Figure 32 illustrates the State Machine controlled by BALANCE_RIGHT, BALANCE_CENTER and BALANCE_LEFT. BALANCE_CENTER is back to 100% output for both Left and Right Channels. Each time triggering BALANCE_RIGHT is to shift one step towards R7. When step to R7, the Left Channel will be mute and Right Channel will maintain the output of 100%. For BALANCE_LEFT, each time triggering is to shift one step towards L7. When step to L7, the Right Channel will be mute and Left Channel will maintain the output of 100%. Table 39 lists the L&R Channels' output Levels of L7~L0 and R0~R7.

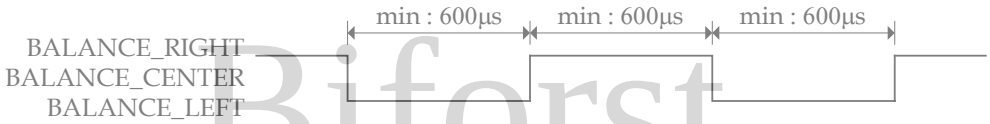


Figure 31. BALANCE_RIGHT, BALANCE_CENTER & BALANCE_LEFT Input Timing Diagram

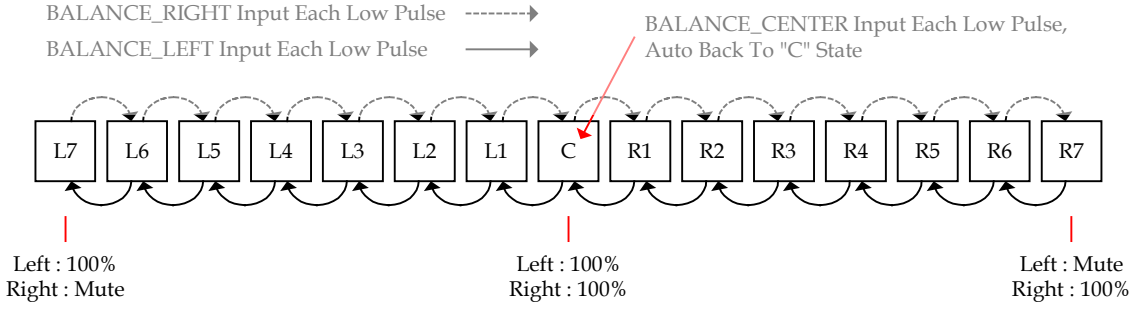


Figure 32. Balance Control State Machine

Table 39. Balance Control

Level	Left Channel Output Level	Right Channel Output Level
L7	100%	0% (Mute)
L6	100%	1.5625%
L5	100%	3.125%
L4	100%	6.25%
L3	100%	12.5%
L2	100%	25%
L1	100%	50%
L0/R0	100%	100%
R1	50%	100%
R2	25%	100%
R3	12.5%	100%
R4	6.25%	100%
R5	3.125%	100%
R6	1.5625%	100%
R7	0% (Mute)	100%

Treble & Bass Control

BI30020B provides the function of adjustment of Treble and Bass via the external pins of TRE_BASS_INC, TRE_BASS_DEC, TRE_BASS_SEL and TRE_BASS_CLR. To input Low Pulse will activate the actions of TRE_BASS_INC, TRE_BASS_DEC, TRE_BASS_SEL and TRE_BASS_CLR. Figure 33 illustrates the Timing Diagram of input signal. The minimum low pulse is 600μs, and so is the interval. The Application Circuit is shown in Figure 34.

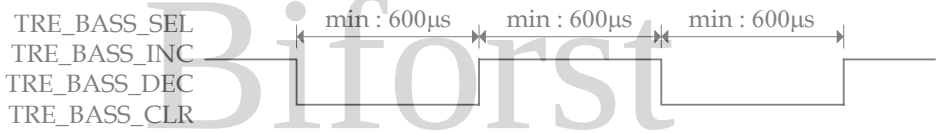


Figure 33. TRE_BASS_SEL, TRE_BASS_INC, TRE_BASS_DEC & TRE_BASS_CLR Input Timing Diagram

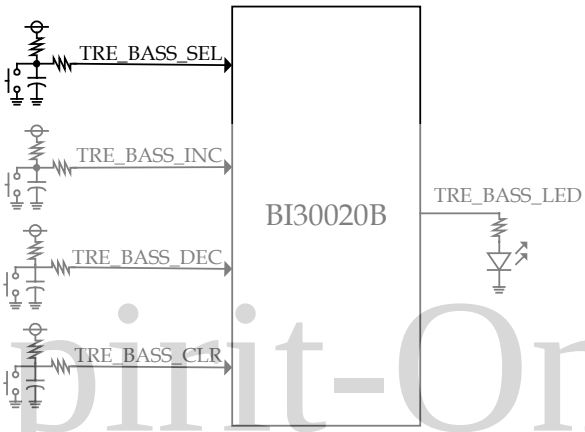


Figure 34. Treble & Bass Control with Indication LED Application Circuit

BI30020B provides the external pin of TRE_BASS_LED to connect a LED, which indicates the current serving function being Treble or Bass. TRE_BASS_SEL is to switch the function to adjust Treble or Bass. Table 40 lists the configurations of TRE_BASS_SEL. While triggering TRE_BASS_SEL to output TRE_BASS_LED to High, BI30020B is serving the function of Bass adjustment. While triggering TRE_BASS_ SEL to output TRE_BASS_LED to Low, BI30020B is serving the function of Treble adjustment.

Table 40. TRE_BASS_SEL Configuration

TRE_BASS_SEL	TRE_BASS_LED	Treble or Bass Adjust Enable
Initial	1	Adjust Bass Level Enable
Low Pulse (1)	0	Adjust Treble Level Enable
Low Pulse (2)	1	Adjust Bass Level Enable

BI30020B adjust the Levels of Treble and Bass via external pins of TRE_BASS_INC and TRE_BASS_DEC. Figure 35 illustrates the State Machine controlled by TRE_BASS_INC and TRE_BASS_DEC to adjust the Levels of Treble. Figure 36 illustrates the State Machine controlled by TRE_BASS_INC and TRE_BASS_DEC to adjust the Levels of Bass. TRE_BASS_INC is to increase the Levels of Treble or Bass and TRE_BASS_ DEC is to decrease the Levels of Treble or Bass. Table 41 shows the configurations of increasing/decreasing of each Level of Treble. Table 42 shows the configurations of increasing/decreasing of each Level of Bass.

BI30020B also provides TRE_BASS_CLR to input signal to trigger the Levels of Treble and Bass back to 100% (no adjustment). Besides, after reset BI30020B, the Levels of Treble and Bass will come back to 100% (no adjustment), TRE_BASS_LED will output to High, and the serving function is Bass adjustment.

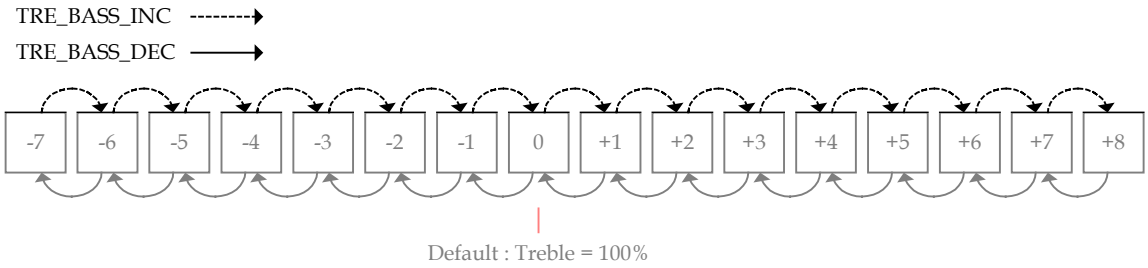


Figure 35. Treble Control State Machine

Table 41. Treble Control Output Level

Level	Output Treble Level
-7	50%
-6	
-5	
-4	
-3	62.5%
-2	75%
-1	87.5%
0 (Default)	100%
+1	112.5%
+2	125%
+3	137.5%
+4	150%
+5	162.5%
+6	175%
+7	187.5%
+8	200%

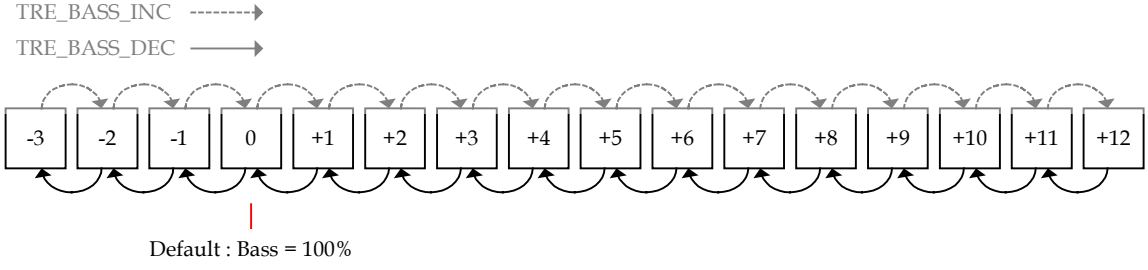


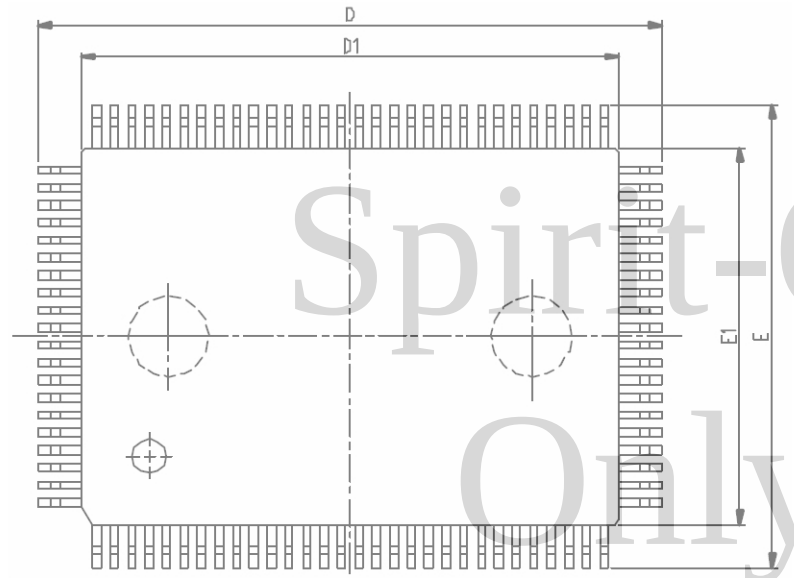
Figure 36. Bass Control State Machine

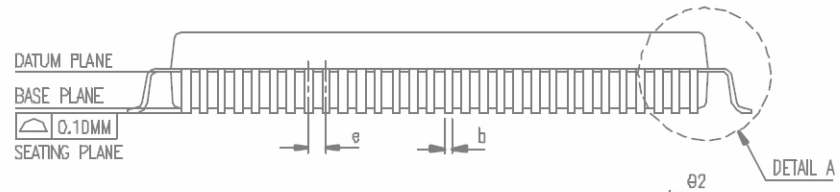
Table 42. Bass Control Output Level

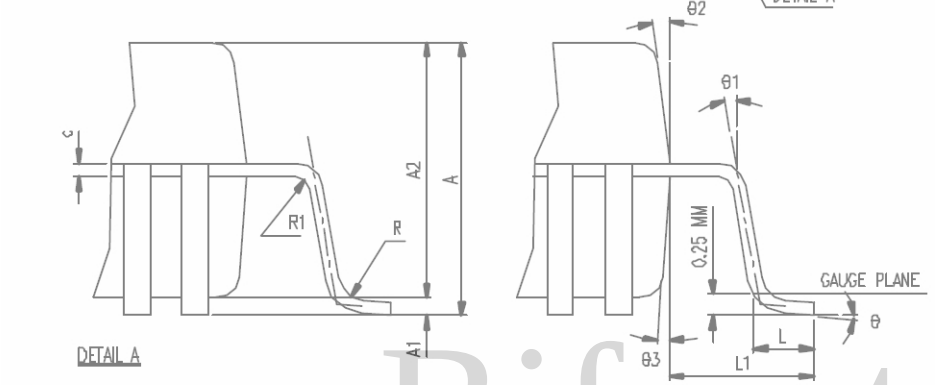
Level	Output Bass Level
-3	25%
-2	50%
-1	75%
0 (Default)	100%
+1	125%
+2	150%
+3	175%
+4	200%
+5	225%
+6	250%
+7	275%
+8	300%
+9	325%
+10	350%
+11	375%
+12	400%

PACKAGE DIMENSION

HQFP100







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			3.40			0.134
A1	0.25			0.01		
A2	2.55	2.80	3.05	0.100	0.110	0.120
b	0.22	0.30	0.33	0.009	0.012	0.013
c	0.13		0.17	0.005		0.007
e	0.65 BASIC			0.026 BASIC		
D	22.95	23.20	23.45	0.904	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
L	0.73	0.88	1.03	0.029	0.035	0.040
L1	1.60 REF.			0.063 REF.		
R1	0.13			0.005		
R	0.13		0.3	0.005		0.012
θ	0		7	0		7
θ1	0			0		
θ2	5		16	5		16
θ3	5		16	5		16
JEDEC	MO-108 (CC-1)					

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Version History

Version	Date	Page	Description
1.0	June 21, 2005		Initial issue
1.1	Sept. 8, 2005	3-31, 16-62	Update Pin Assignment, Pin list (#17, 40-41, 59, 64 & 68-70) Modify Treble & Bass Adjustment Update I2C Control Register Address 0 & 11
1.2	Sept. 16, 2005	4-9	Change Pin 96's Type from "Bi-Direction" to "Output". Update "Can Flatting & Ignore Setting Value in I^2C Control Mode" to "Must Set To VDD or Ground in I^2C Control Mode". Update Pin 60 ~ 63's Type to "Driver (3.3V) and I/O Pad Function to "Output Voltage Level Dependent On VDD".
1.3	Jan. 26, 2006	17-22	Update Charts of Driving Capability
1.4	Feb. 10, 2006	4-6	Add Data of Device Characteristics