2.1 Channel Digital Amplifier

BI3010AP1

Data Sheet

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Biforst Technology Inc.

2.1 Channel Digital Amplifier

BI3010AP1

GENERAL DESCRIPTION

The BI3010AP1 is the very right choice for 2.1 channel audio systems. The BI3010AP1 is a newest generation of pure digital amplifier that is embedded with Digital Electronic Crossover and Speaker Driver. Directly input 2 channel digital audio data, the BI3010AP1 will generate 3 sets of signal for Left, Right and Sub-Woofer Channels. Each set of signal can select crossover frequency to drive speakers without external complicated Filter circuit. The powerful Audio Volume Control includes power-on Initial volume function, 32-Level Audio Volume Control and Mute Control. It also provides Volume Level Boost and Output Anti-Clipping function. The quality of sound is pure and full which is much different from the traditional Class AB Amplifier.

APPLICATION

- Note-book/Desktop PC/LCD Monitor/TV Surround Sound Systems
- Portable DVD/VCD/CD/MP3 Speakers and Headphones
- Video Game Speakers

FEATURE

- Operation Voltage:
  - Digital Part: 3.0 ~ 3.6V
  - Speaker Driver: 3.0 ~ 5.5V
- Operation Frequency:
  - Accept 256xFS or 45.1584 ~ 49.152MHz For Operation
  - Provide On Chip OSC Circuit For 45.1584 ~ 49.152MHz Crystal Connect
- Audio Data Input Interface:
  - When Use Internal SRC, Accept 29 ~ 96KHz Wide Continue Sample Rate Range (when System Clock at 49.152MHz)
  - When Use External 256xFS Clock Source, Accept below 96KHz Sample Rate
  - Support I^2S, Left-Justified, & Right-Justified Format
  - Auto Adapt Word Length For Left & Right Channel In I2S & Left-Justified Mode
  - Provide 24-Bits Word Length Select For Left & Right Channel In Right-Justified Mode
  - Provide Left/Right Frame Select Exchange Function
  - Provide Serial Clock Positive or Negative Edge Latch Data Select
- Crossover Frequency Select:
  - 8 Crossover Frequency Selects Through External Pin

  - Crossover Frequency from 150Hz To 800 Hz, 100Hz For Each Step
- Speaker Driver:
  - Main Channel:
    - Output Can Select Bypass or Through Internal Digital High Pass Filter Circuit
    - Provide Embedded Left/Right Channel Speaker Driver (1W@5V Per Channel)
  - Sub-Woofer Channel:
    - Generate Sub-Woofer Channel Data From Main Channel Data
    - Proved Embedded Sub-Woofer Channel Speaker Driver (1.5W@5V Per Channel)
  - Earphone Channel
    - Provide 3 or 4-Wire Type Earphone Connection Select
    - Switch Speaker Driver or Earphone Driver Output Through One External Pin
- Audio Volume Control:
  - Provide 32 Level Volume Select
  - Set Power-On Initial Volume Value Through External Pin (Volume Value: 0 & 16)
  - Main & Sub-Woofer Channel Volume Adjust Dependent or Together Through External Pin
  - Main & Sub-Woofer Channel Have Digital Audio Volume Control Separately
  - Main Channel & Earphone Use Same Volume Control
  - Provide Volume Level Boost & Output Anti-Clipping Function Enable/Disable For Play DVD Movie
- Mute Control:
  - Set Main & Sub-Woofer Mute Enable/Disable Through External Pin
  - Provide Main & Sub-Woofer Channel Mute Enable LED Indication Output Pin
- Package Type:
  - LQFP 64pins

ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	PARAMETER	VALUE	UNIT
V_{DDA}	Speaker Driver Power Supply Voltage	-0.3 to 5.5	V
V_{DD}	Digital Amplifier Kernel Power Supply Voltage	-0.3 to 3.6	V
V_{IN}	Input Signal Voltage	-0.3 to V_{DD} +0.3	V
Ta	Operating Temperature	-40 ~ +85	℃
Tst	Storage Temperature	-40 ~ +150	℃

Note 1: Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DDA}	Speaker Driver Supply Voltage	3.0		5.5	V
V_{DD}	Digital Part Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.5			V
V_{IL}	Input Low Voltage			0.5	V
V_{OH}	Output High Voltage	V_{DD} -0.5			V
V_{OL}	Output Low Voltage			0.6	V
Ta	Operating Temperature	-40		85	℃

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Ta=25℃, V_{DDA} =5V, V_{DD}=3.3V)

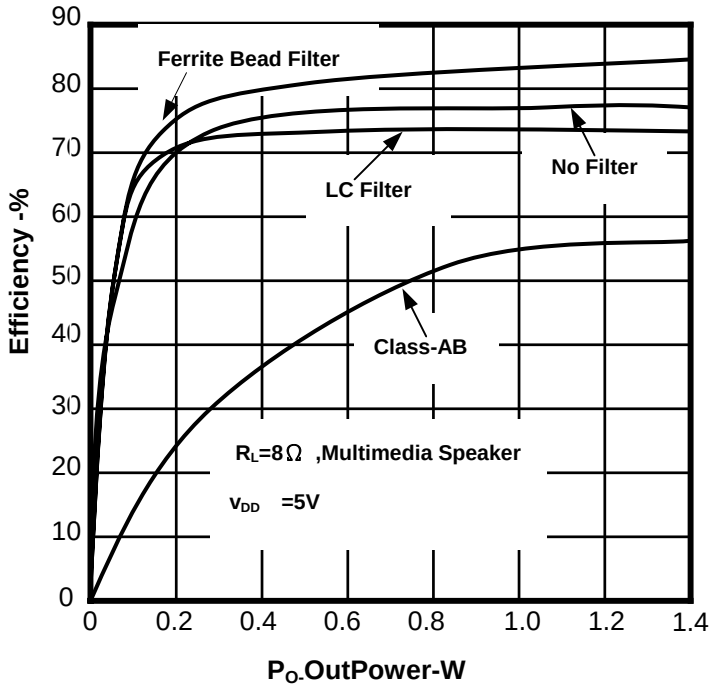
SYMBOL	PARAMETER	TEST CONDITIONS	SPECIFICATION			UNIT
			MIN	TYP	MAX	
PSRR	Power supply rejection ratio	P V_{DDA} =4.5V to 5.5V		-70		dB
$\lvert I_{IH} \rvert$	High-level input current	P V_{DDA} =3.3V, V_I =P V_{DDA}			1	uA
$\lvert I_{IL} \rvert$	Low -level input current	P V_{DDA} =3.3V, V_I =0V			1	uA
I_{PWDN}	Power Down Current	Sysclk halt Audio output disable			1	uA

OPERATING CHARACTERISTICS – MAIN CHANNEL (Ta=25℃, V_{DDA} =5V, V_{DD}=3.3V, R_L=8Ω; unless otherwise specified)

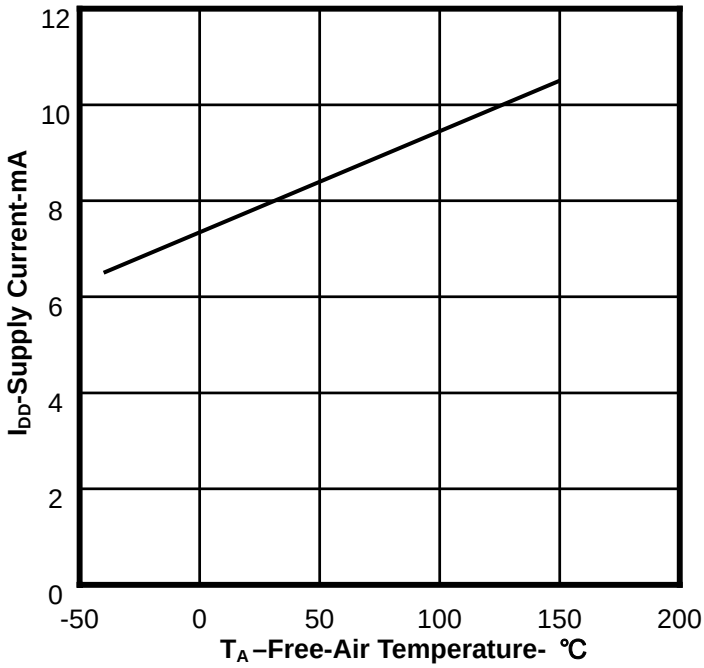
SYMBOL	PARAMETER	TEST CONDITIONS	SPECIFICATION			UNIT
I_{DDA}	DC Operating Current	VR or VL		320		mA
I_{DD}	DC Operating Current	I^2S input active		2		mA
P_O	Output Power	THD = 1%, R_L=4Ω		1.0		W
THD+N	Total Harmonic Distortion plus Noise	P_O = 1W			1%	
k_{SVR}	Supply ripple rejection ratio			-71		dB
SNR	Signal-to Noise Ratio	VR or VL Po = 0.6 W / one channel		80		dB
V_n	Noise output voltage			20		μV_{Rms}

TYPICAL CHARACTERISTICS

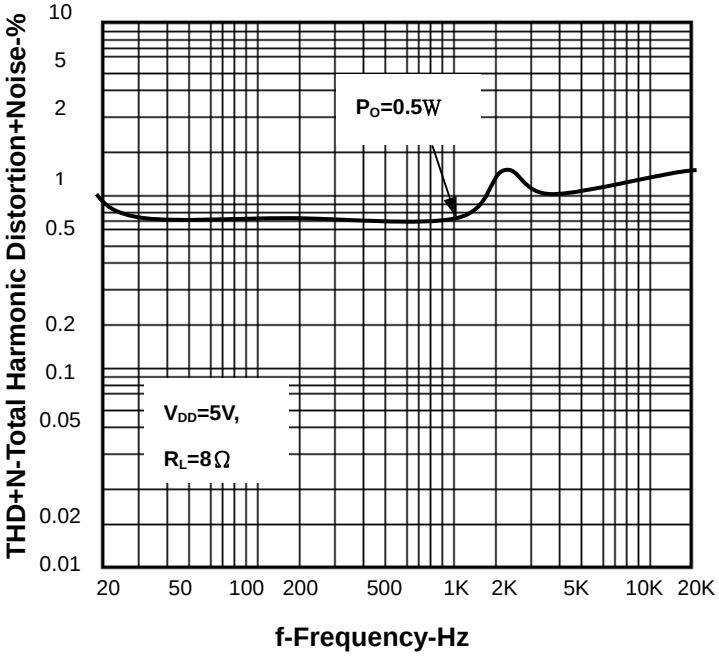
EFFICIENCY vs OUTPUT POWER



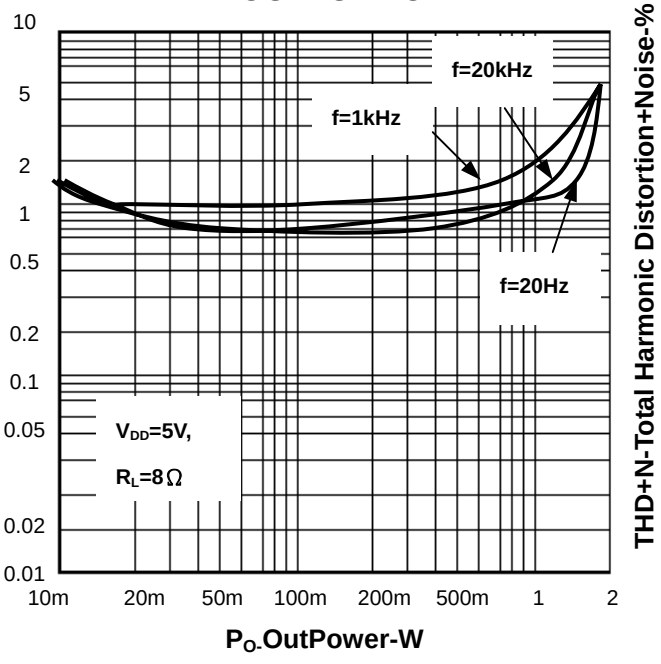
SUPPLY CURRENT vs FREE-AIR TEMPERATURE



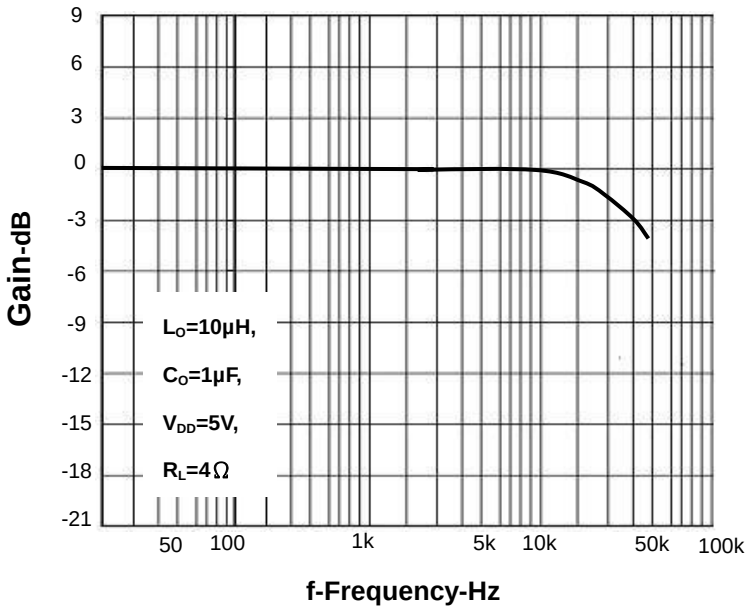
TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



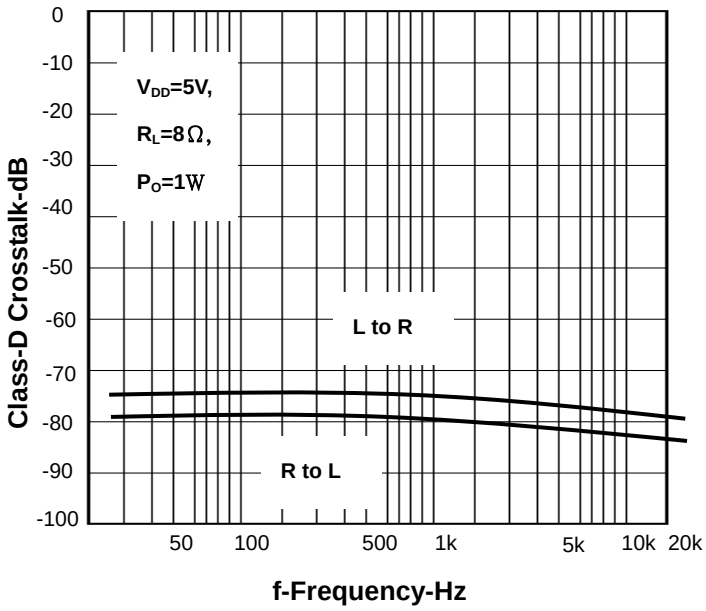
TOTAL HARMONIC DISTORTION+NOISE vs OUTPUT POWER



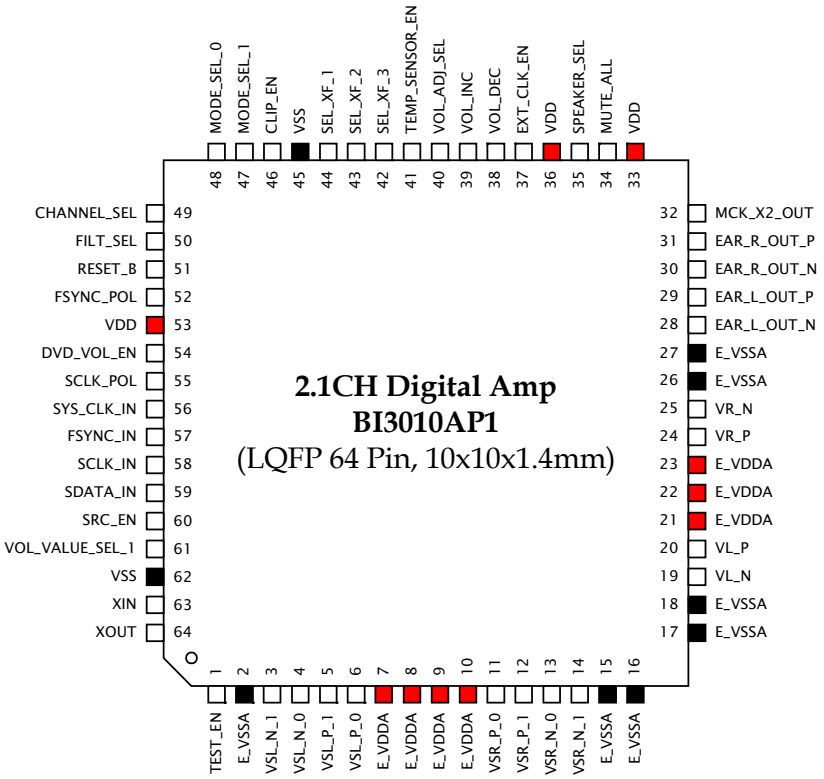
FREQUENCY CHARACTERISTICS [V_{DD}=5.0V]



CROSSTALK



PIN ASSIGNMENTS



PIN LIST & DESCRIPTION

Pin No.	Pin	Type	I/O Pad Function
1	TEST_EN	Input (3.3V)	Test Mode Enable *0 : Test Mode Disable* *1 : Test Mode Enable*
2	E_VSSA	Power	Speaker & Earphone Driver Ground Input
3	VSL_N_1	Output (5.0V)	Sub-Woofer Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
4	VSL_N_0	Output (5.0V)	Sub-Woofer Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
5	VSL_P_1	Output (5.0V)	Sub-Woofer Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
6	VSL_P_0	Output (5.0V)	Sub-Woofer Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
7	E_VDDA	Power (5.0V)	Speaker & Earphone Driver 3.3 ~ 5.0V Power Input
8	E_VDDA		
9	E_VDDA		
10	E_VDDA		
11	VSR_P_0	Output (5.0V)	Sub-Woofer Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
12	VSR_P_1	Output (5.0V)	Sub-Woofer Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
13	VSR_N_0	Output (5.0V)	Sub-Woofer Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
14	VSR_N_1	Output (5.0V)	Sub-Woofer Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
15	E_VSSA	Power	Speaker & Earphone Driver Ground Input
16	E_VSSA		
17	E_VSSA		
18	E_VSSA		
19	VL_N	Output (5.0V)	Left Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
20	VL_P	Output (5.0V)	Left Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
21	E_VDDA	Power (5.0V)	Speaker & Earphone Driver 3.3 ~ 5.0V Power Input
22	E_VDDA		
23	E_VDDA		
24	VR_P	Output (5.0V)	Right Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
25	VR_N	Output (5.0V)	Right Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
26	E_VSSA	Power	Speaker & Earphone Driver Ground Input
27	E_VSSA		
28	EAR_L_OUT_N	Output (5.0V)	Earphone Left Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
29	EAR_L_OUT_P	Output (5.0V)	Earphone Left Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*

Pin No.	Pin	Type	I/O Pad Function
30	EAR_R_OUT_N	Output (5.0V)	Earphone Right Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
31	EAR_R_OUT_P	Output (5.0V)	Earphone Right Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
32	MCK_X2_OUT	Output (3.3V)	XIN_CLK or XIN_CLK/2 Clock Output
33	VDD	Power	3.3V Power Input
34	MUTE_ALL	Input (3.3V)	All Channel Mute Trigger Signal Input *Low Level Pulse Trigger Active*
35	SPEAKER_SEL	Input (3.3V)	Earphone Type Select *0 : 4 Wire Earphone Mode Select* *1 : 3 Wire Earphone Mode Select*
36	VDD	Power	3.3V Power Input
37	EXT_CLK_EN	Input (3.3V)	External 49.152MHz Clock Input Enable *0 : Internal Crystal OSC Enable* *1 : When SRC_EN = 1, Use External Clock to XIN Pin*
38	VOL_DEC	Input (3.3V)	Audio Volume Decrease Input *Low Level Pulse Trigger Active*
39	VOL_INC	Input (3.3V)	Audio Volume Increase Input *Low Level Pulse Trigger Active*
40	VOL_ADJ_SEL	Input (3.3V)	Select Main Channel & Sub-Woofer Channel Volume Adjust Independently or Adjust Together *Initial → Adjust Together → Adjust Main Channel → Adjust Sub-Woofer Channel → Loop Again*
41	TEMP_SENSOR_EN	Input (3.3V)	Temp. Sensor Enable *0 : Temp. Sensor Disable* *1 : Temp. Sensor Enable*
42	SEL_XF_3	Input (3.3V)	Cross Over Frequency Select *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 000 : 150Hz* *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 001 : 250Hz* *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 010 : 350Hz* *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 011 : 450Hz* *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 100 : 550Hz* *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 101 : 650Hz* *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 110 : 750Hz* *(SEL_XF_3, SEL_XF_2, SEL_XF_1) = 111 : 800Hz*
43	SEL_XF_2		
44	SEL_XF_1		
45	VSS	Power	3.3V Ground Input
46	CLIP_EN	Input (3.3V)	Speaker Output Anti-Clipping Enable *0 : Internal Speaker Output Anti-Clipping Function Disable* *1 : Internal Speaker Output Anti-Clipping Function Enable*

Pin No.	Pin	Type	I/O Pad Function
47	MODE_SEL_1	Input (3.3V)	Serial Audio Data Input Format Select *(MODE_SEL_1, MODE_SEL_0 = 00) : I^2S Format Mode Select* *(MODE_SEL_1, MODE_SEL_0 = 01) : I^2S Format Mode Select* *(MODE_SEL_1, MODE_SEL_0 = 10) : Left-Justified Mode Select* *(MODE_SEL_1, MODE_SEL_0 = 11) : Right-Justified Mode Select*
48	MODE_SEL_0		
49	CHANNEL_SEL	Input (3.3V)	2.1 Channel Speaker or Earphone Output Select *0 : 2.1 Channel Speaker Signal Output* *1 : Earphone Signal Output*
50	FILT_SEL	Input (3.3V)	Main Channel Digital High Pass Filter Bypass Enable Signal Input *0 : Digital High Pass Filter Active, Cross Over Frequency Set from SEL_XF_1 ~ SEL_XF_3* *1 : Digital High Pass Filter Bypass*
51	RESET_B	Input (3.3V)	Reset Signal Input *0 : Reset Active (Must Maintain Low Level Great than 1ms)* *1 : Normal Operation*
52	FSYNC_POL	Input (3.3V)	Serial Audio Data Signal “FSYNC_IN” Left/Right Frame Select *0 : Low Level = Right Channel, High Level = Left Channel* *1 : Low Level = Left Channel, High Level = Right Channel*
53	VDD	Power	3.3V Power Input
54	DVD_VOL_EN	Input (3.3V)	Volume Boost Function Enable *0 : Volume Boost Function Disable* *1 : Volume Boost Function Enable (Loud than DVD_VOL_EN = 0)*
55	SCLK_POL	Input (3.3V)	Serial Audio Data Signal “SCLK_IN” Polarity Select *0 : Falling Edge Latch Audio Data* *1 : Rising Edge Latch Audio Data*
56	SYS_CLK_IN	Input (3.3V)	When SRC_EN = 0, 256xFS System Clock Input
57	FSYNC_IN	Input (3.3V)	Serial Audio Data Left/Right Frame Input
58	SCLK_IN	Input (3.3V)	Serial Audio Data Latch Clock Input
59	SDATA_IN	Input (3.3V)	Serial Audio Data Input
60	SRC_EN	Input (3.3V)	Internal SRC Circuit Enable *0 : SRC Disable* *1 : SRC Enable*
61	VOL_VALUE_SEL_1	Input (3.3V)	Initial Volume Value Select *(VOL_VALUE_SEL_1 = 0) : Volume 0* *(VOL_VALUE_SEL_1 = 1) : Volume 16*
62	VSS	Power	3.3V Ground Input
63	XIN	Input (3.3V)	When EXT_CLK_EN = 0, 45.1584 ~ 49.152MHz Crystal OSC Input Path When EXT_CLK_EN = 1, External 45.1584 ~ 49.152MHz Clock Input Path
64	XOUT	Output	49.152MHz Crystal OSC Output Path

FUNCTION DESCRIPTION

Operation Clock Select

BI3010AP1 requires a clock for internal circuit operation. There are two types of clocks can be accepted. One is external input of 256xFS and the other is generated by BI3010AP1 itself by connecting a Crystal of 45.1584 ~ 49.152MHz.

The use and detail description is illustrated as below.

- **256xFS –**256xFS clock is used when the system can provide the clock and this clock can syncronally generate the input audio data. To use the clock, the external pin of BI3010AP1 “SRC_EN” is set to LOW, “EXT_CLK_EN” set to HIGH and “XIN” set to LOW. The BI3010AP1 will disable the internal SRC (Sample Rate Converter) and input 256xFS clock to “SYS_CLK_IN” for BI3010AP1’s operation. The setting of “SRC_EN” is as Table 1 and “EXT_CLK_EN” as Table 2.

(*The FS is the Sample Rate of Input Audio Data. For example, FS is 44.1KHz and 256xFS is 11.2896MHz. Table 3 lists the Operation Clock most frequently used)

Table 1. SRC_EN Configuration

SRC_EN	SRC Circuit Enable
0	SRC Disable
1	SRC Enable

Table 2. EXT_CLK_EN Configuration

EXT_CLK_EN	OSC External Clock Input Enable
0	OSC Enable
1	External Clock Input Enable (Clock Input Through XIN Pin)

Table 3. General BI3010AP1 Operation Clock (256xFS) List

FS (Sample Rate)	BI3010AP1 Operation Clock: 256xFS
32K	8.192MHz
44.1K	11.2896MHz
48K	12.288MHz
88.2K	22.5792MHz
96K	24.576MHz

- **Crystal –** When system cannot provide 256xFS Clock to BI3010AP1, “SRC_EN” must be set to HIGH and “EXT_CLK_EN” set to LOW. The BI3010AP1 is required to connect a Crystal of 45.1584 ~ 49.152MHz, so BI3010AP1 can generate internal clock. 49.152Mhzfor System Clock is highly recommended. The external pin of “SYS_CLK_IN” can then be set to LOW. Only directly input Audio Data to BI3010AP1, BI3010AP1 will automatically judge and adjust the best condition for operation according to the input Audio Data.

Digital Audio Data Input Format Select

BI3010AP1 is to drive speaker just by inputting the Digital Audio Data. It supports the PCM Format from CD player, DVD decoded chip or DSP decoder such as Portable MP3 Player.

BI3010AP1 can receive Digital Audio Data input format by setting the external pins of MODE_SEL_1, MODE_SEL_0, FSYNC_POL, and SCLK_POL. MODE_SEL_1 and MODE_SEL_0 are to set MSB starting position of Digital Audio Data. BI3010AP1 supports popular formats such as I2S, Left-Justified and Right-Justified. Table 4 illustrates the setup list. FSYNC_POL is to adjust Serial Audio Data Left/Right Frame and SCLK_POL is to select Audio Data Signal “SCLK_IN” Polarity. Table 5 and Table 6 are the lists.

Figure 1 illustrates how the actual receiving data format relates to the pin setup. While in Left-Justified Mode, each Audio Data’s MSB position is left aligned to Rising/Falling Edge of FSYNC_IN’s signal. While in Right-Justified Mode, each Audio Data’s LSB position is right aligned to Rising/Falling Edge of FSYNC_IN’s signal. Compared to Left-Justified Mode, one Clock Cycle shift of SCLK_IN is occurred for each Audio Data’s MSB position under I^2S Mode.

When BI3010AP1 is set to I^2S and Left-Justified Modes, BI3010AP1 can automatically latch the data following the signal change of FSYNC_IN and SCLK_IN. However, when BI3010AP1 is set to Right-Justified Mode, it accepts only 24-bits of the word length of the input data format. Therefore, if the input word length is not consistent, BI3010AP1 will outburst the noise or fail to operate.

Table 4. Digital Audio Data Input Format Select

MODE_SEL_1	MODE_SEL_0	Audio Data Input Select
0	0	I^2S Audio Data Format Input
0	1	
1	0	Left-Justified Audio Data Format Input
1	1	Right-Justified Audio Data Format Input

Table 5. Digital Audio Data Left/Right Frame Select

FSYNC_POL	Digital Audio Data Left/Right Frame Select
0	FSYNC_IN = 1 : Left Channel / FSYNC_IN = 0 : Right Channel
1	FSYNC_IN = 1 : Right Channel / FSYNC_IN = 0 : Left Channel

Table 6. Digital Audio Data Latch Clock Select

SCLK_POL	Digital Audio Data Left/Right Frame Select
0	Falling Edge Latch Audio Data
1	Rising Edge Latch Audio Data

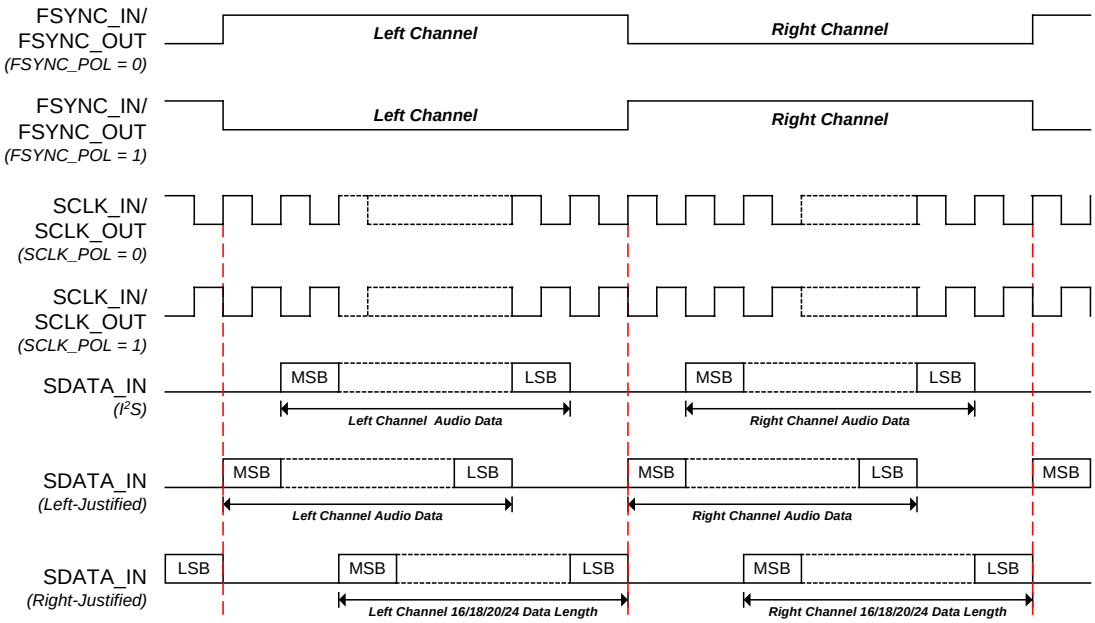


Figure 1. Digital Audio Data Input Format

Crossover Frequency Configuration

BI3010AP1 is embedded an Electronic Digital Crossover. By setting the external pins of SEL_XF_1, SEL_XF_2, and SEL_XF_3 to select the crossover frequency for output signals. In addition, by setting “FILT_SEL”, the Main Channel can be determined if the output signals pass through High Pass Filter or not. However, Sub-Woofer Channel will pass through High Pass Filter.

Table 7 lists the FILT_SEL setup. When FILT_SEL is set to LOW, Main Channel’s signal will pass through High Pass Filter. The output frequency is selected through the setup of SEL_XF_1, SEL_XF_2, and SEL_XF_3. When FILT_SEL is set to HIGH, Main Channel’s signal will not pass through High Pass Filter but directly output the full range of frequency.

Table 7. FILT_SEL Configuration

FILT_SEL	Main Channel Digital High Pass Filter Bypass Enable
0	Disable, Through High Pass Filter
1	Enable, Bypass High Pass Filter

Table 8 lists the Crossover Frequency setup for BI3010AP1 Main Channel & Sub-Woofer Channel. The crossover frequency is selected by setup the external pins of SEL_XF_1, SEL_XF_2, and SEL_XF_3. The frequency is ranging from 150Hz to 800Hz with 8 classes. For example, when SEL_XF_3 = 0, SEL_XF_2 = 1, SEL_XF_1 = 0, and FILT_SEL = 0, BI3010AP1 will only output the audio signal greater than 350 Hz and deliver the audio signal less than 350Hz to Sub-Woofer Channel. The setup of crossover frequency is determined by speaker's characteristics that require the hearing test to decide the appropriate setting.

Table 8. Cross Over Frequency Select

FILT_SEL	SEL_XF_3	SEL_XF_2	SEL_XF_1	Left/Right Main Channel Output Frequency Range	Sub-Woofer Channel Output Frequency Range
0	0	0	0	> 150 Hz	< 150 Hz
	0	0	1	> 250 Hz	< 250 Hz
	0	1	0	> 350Hz	< 350Hz
	0	1	1	> 450 Hz	< 450 Hz
	1	0	0	> 550 Hz	< 550 Hz
	1	0	1	> 650 Hz	< 650 Hz
	1	1	0	> 750 Hz	< 750 Hz
	1	1	1	> 800 Hz	< 800 Hz
1	0	0	0	Full Range	< 150 Hz
	0	0	1		< 250 Hz
	0	1	0		< 350Hz
	0	1	1		< 450 Hz
	1	0	0		< 550 Hz
	1	0	1		< 650 Hz
	1	1	0		< 750 Hz
	1	1	1		< 800 Hz

Speaker & Earphone Driver

BI3010AP1 is embedded with a set of 2.1 CH Speaker Driver, which connects to 2 speakers of Left/Right Main Channel and one speaker of Sub-Woofer Channel. It also provide a set of Earphone Driver, which can select to output through Speaker Driver or Earphone Driver by setting the external pin of CHANNEL_SEL. Table 9 is the setup for CHANNEL_SEL. While CHANNEL_SEL is set to LOW, Speaker Driver is chosen to be the output. While CHANNEL_SEL is set to HIGH, Earphone Driver is the output to the full range without the effect of internal digital crossover circuit.

Table 10 and Table 11 are the connection relationship of Speaker Driver and Earphone Driver.

The pins listed in the same field of the table are the same output signals, which require connecting together. For example, pins of VL_P_0 and VL_P_1 require connecting together for Speaker Driver Left Channel + listed in Table 10. Furthermore, BI3010AP1 requires Low Pass Filter and the optional circuit in between the Speaker Driver & Earphone Driver and Speakers. Please refer to BI3010AP1 Application Note Schematic Drawing for detail Low Pass Filer and optional circuit design.

Table 9. CHANNEL_SEL Configuration

CHANNEL_SEL	Speaker Driver & Earphone Driver Select
0	Speaker Driver Output Active, Earphone Output Disable
1	Speaker Driver Output Disable, Earphone Output Active

Table 10. Speaker Driver Output Pin

Channel	Speaker Driver Output Pin Name
Left Channel +	VL_P_0, VL_P_1
Left Channel -	VL_N_0, VL_N_1
Right Channel +	VR_P_0, VR_P_1
Right Channel -	VR_N_0, VR_N_1
Sub-Woofer Channel +	VSL_P_0, VSL_P_1, VSR_P_0, VSR_P_1
Sub-Woofer Channel -	VSL_N_0, VSL_N_1, VSR_N_0, VSR_N_1

Table 11. Earphone Driver Output Pin

Channel	Earphone Driver Output Pin
Left Channel +	EAR_L_OUT_P
Left Channel -	EAR_L_OUT_N
Right Channel +	EAR_R_OUT_P
Right Channel -	EAR_R_OUT_N

The Earphone Driver of BI3010AP1 can be set through SPEAKER_SEL to output from 3-wire or 4-wire. Table 12 lists the configuration.

Table 12. SPEAKER_SEL Configuration

SPEAKER_SEL	Earphone Type
0	4-Wire
1	3-Wire

Temperature Sensor Configuration

Temperature Sensor is built in BI3010AP1 for detecting the temperature of embedded Speaker Driver. It can be turned on or off via pin of TEMP_SENSOR_EN. When TEMP_SENSOR_EN is set to LOW, the Temperature Sensor is disable. While TEMP_SENSOR_ EN is set to HIGH, the Temperature Sensor will be turned on. If the temperature of Speaker Driver is greater than 125℃, BI3010AP1 will automatically shut down the Speaker Drive. After the temperature comes back to normal operation range, BI3010AP1 will automatically start the operation. Table 13 is the setup for Temperature Sensor.

Table 13. Temperature Sensor Configuration

TEMP_SENSOR_EN	Temperature Sensor Status
0	Disable
1	Enable, Speaker driver will auto shut-down when temperature sensor detect speaker driver over 125℃, & auto turn-on when speaker driver cool down

Power-On Initial Volume Configuration

BI3010AP1 provides the function to setup the initial volume value when power-on. The setup is via external pin of VOL_VALUE_SEL_1 to determine the initial volume value of Main Channel and Sub-Woofer Channel. There are two values for setup: 0 (Mute) and 16. Table 14 is the corresponding list for setup.

Table 14. VOL_VALUE_SEL Configuration

VOL_VALUE_SEL_1	Initial Volume Value
0	0 (Mute)
1	16

Volume Control Configuration

BI3010AP1 has 32-Level digital volume control individually for each Main Channel and Sub-Woofer Channel by setup pins of VOL_INC, VOL_DEC, and VOL_ADJ_SEL. The Earphone volume is controlled by Main Channel. VOL_INC is used for the increase of the volume and VOL_DEC for decrease of the volume. VOL_ADJ_SEL is thus to select if the volume control of

Main Channel and Sub-Woofer Channel is dependent and independent adjustment.

Table 15 lists the continuous Low Pulse into VOL_ADJ_SEL to control Main Channel and Sub-Woofer Channel volume adjustment.

Table 15. VOL_ADJ_SEL Configuration

VOL_ADJ_SEL	Volume Control Status
Initial Value	Main Channel & Sub-Woofer Channel Volume Control Together
Low Pulse (1)	Main Channel Volume Control Only
Low Pulse (2)	Sub-Woofer Channel Volume Control Only
Low Pulse (3)	Main Channel & Sub-Woofer Channel Volume Control Together

VOL_INC, VOL_DEC and VOL_ADJ_SEL are to input Low Pulse to activate the action. Figure 2 is the Timing Diagram of input signal. The minimum low pulse is 200μs, and so is the interval.

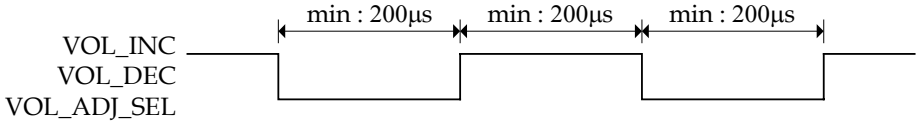


Figure 2. VOL_DEC、VOL_INC & VOL_ADJ_SEL Input Timing Diagram

Mute Configuration

BI3010AP1 provides Mute trigger pin of MUTE_ALL for Main Channel and Sub-Woofer while Earphone is controlled together with Main Channel. MUTE_ALL is to input Low Pulse to activate the action. Figure 3 illustrates the Timing Diagram of input signal. The minimum low pulse is 200μs, and so is the interval. Table 16 lists the mute status of BI3010AP1 while the continuous Low Pulse input to MUTE_ALL. Further, when mute function is activated and then deactivated, the previous volume value will not be changed.

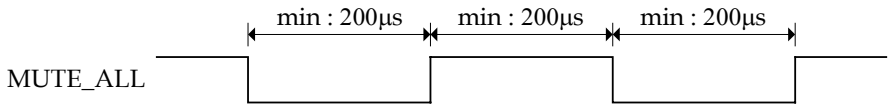


Figure 3. MUTE_ALL Input Timing Diagram

Table 16. MUTE_ALL Configuration

MUTE_ALL	Mute Control Status
Initial Value	All Channel Mute Disable
Low Pulse (1)	All Channel Mute Enable
Low Pulse (2)	All Channel Mute Disable

Volume Boost & Output Anti-Clipping Function Configuration

BI3010AP1 provides Volume Boost and Output Anti-Clipping functions through external pin of DVD_VOL_EN to control enable/disable of Volume Boost and CLIP_EN for Output Anti-Clipping. The setups are listed in Table 17 and 18.

The function of Volume Boost is to double the output volumes of BI3010AP1. For example, if volume set to 9 and DVD_VOL_EN is set to LOW, BI3010AP1 will actually output the volume of 9. When DVD_VOL_EN is set to HIGH, BI3010AP1 will actually output the volume of 18 to enhance the auditory sensation.

The function of Output Anti-Clipping is to control the wow effect when output signal is over the maximum amplitude. For example, when CLIP_EN is set to LOW, BI3010AP1 will automatically control and decrease the wow effect by internal circuit design to eliminate sound of clip. When CLIP_EN is set to HIGH, BI3010AP1 will allow the wow effect and hear the sound of clip. Therefore, it is highly recommended to set both HIGH for DVD_VOL_EN and CLIP_EN when play DVD Movie, set to LOW when listening to CD for better performance of auditory sensation.

Table 17. DVD_VOL_EN Configuration

DVD_VOL_EN	Volume Boost Enable
0	Disable
1	Enable

Table 18. CLIP_EN Configuration

CLIP_EN	Output Anti-Clipping Enable
0	Disable
1	Enable

Reset

RESET_B pin of BI3010AP1 is the Global Reset for all internal circuit. Table 19 is the setup of RESET_B. When reset BI3010AP1, RESET_B must be set to LOW, and remain LOW at least 1ms.Then return to HIGH to complete the process of Reset.

Table 19. RESET_B Configuration

RESET_B	BI3010AP1 Status
0	Reset
1	Normal Operation

Crystal Connection

In previous section mentioned that BI3010AP1 can connect a Crystal of 45.1584 ~ 49.152MHz to generate the clock for internal operation. Figure 4 recommends the application circuit to connect a 49.152MHz Crystal. In Figure 4, to set external pin of EXT_CLK_EN to LOW, TEST_EN to LOW and I2S_OUT_EN_B to HIGH, the Crystal oscillation status can be monitored by Pin 54

(OSC_CLK_OUT). Notice: Because the specifications and characteristics of various Crystal, the surrounding optional circuit should be tuned accordingly.

Further, if no connecting to Crystal, EXT_CLK_EN can set to HIGH and input Clock of 45.1584 ~ 49.152MHz via “XIN”. Figure 5 illustrates the example of application circuit of BI3010AP1 and 49.152MHz OSC.

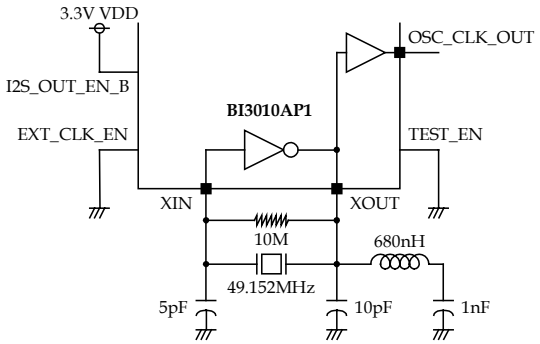


Figure 4. 49.152MHz Crystal Application Circuit

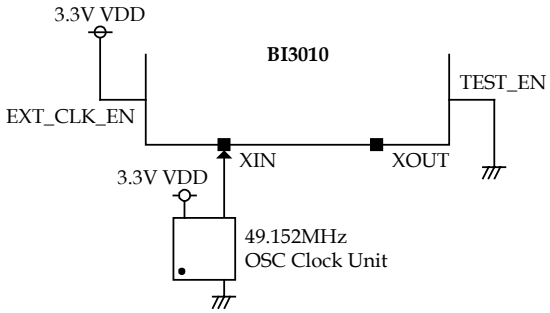


Figure 5. 49.152MHz OSC Application Circuit

Pin 32 MCK_X2_OUT

Table 20 lists the status of Pin 32 (MCK_X2_OUT) under different condition of SRC_EN. Table 21 lists the clock output when SRC_EN is set to HIGH and use 49.152MHz as the max. operation frequency. After reset BI3010AP1, Pin 32 (MCK_X2_OUT) will output 24.576MHz.

Table 20. Pin 32 – MCK_X2_OUT

Pin No	Pin Name	SRC_EN = 1	SRC_EN = 0
32	MCK_X2_OUT	XIN_CLK or XIN_CLK/2 Clock Output	Output Low Level

XIN_CLK is clock frequency from XIN pin

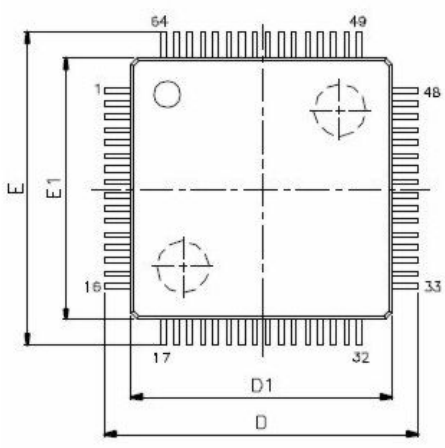
Table 21. Pin 32 – MCK_X2_OUT Default Clock Output Frequency

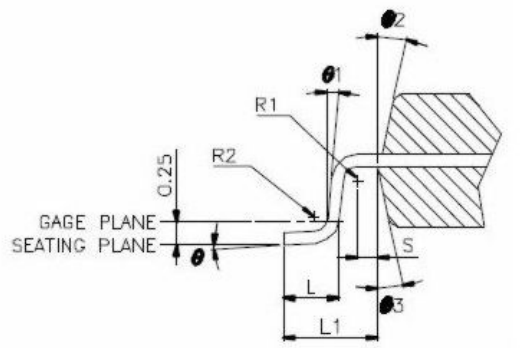
Pin No	Pin Name	Clock Output	Example
32	MCK_X2_OUT	XIN_CLK/2	49.152MHz/2 = 24.576MHz

XIN_CLK is clock frequency from XIN pin

PACKAGE DIMENSION

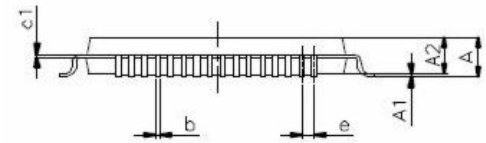
LQFP64





VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c1	0.09	–	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20 REF		
θ	3.5° REF		
θ1	5.0° REF		
θ2	12° REF		
θ3	12° REF		
R1	0.16 REF		
R2	0.15 REF		



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Version History

Version	Date	Page	Description
1.0	Apr. 20 2005		Initial issue
1.1	June 20, 2005	2~6, 12	Add Data of Device Characteristics & Update Figure 1