

**Silicon PNP Power Transistors****2SA1067****DESCRIPTION**

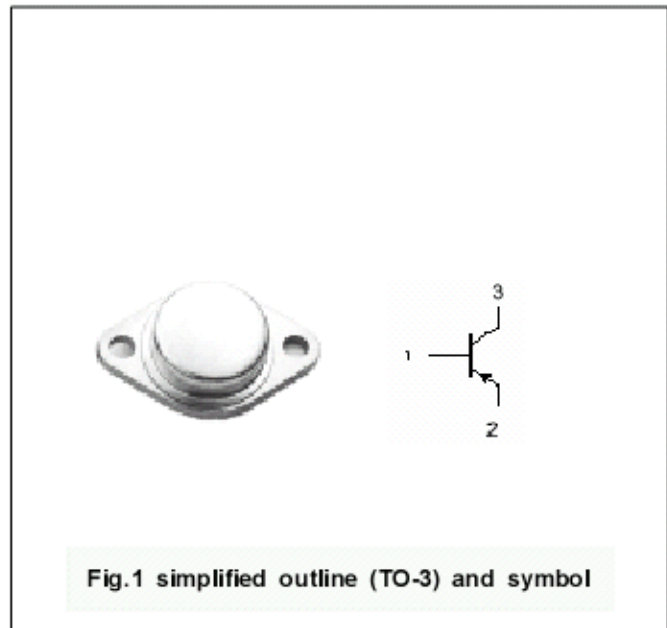
- With TO-3 package
- Low collector saturation voltage
- High transition frequency

APPLICATIONS

- For audio and general purpose amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

**Fig.1 simplified outline (TO-3) and symbol****Absolute maximum ratings(Ta=℃)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-120	V
V_{CEO}	Collector-emitter voltage	Open base	-120	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-10	A
I_{CM}	Collector current-peak		-14	A
P_C	Collector power dissipation	$T_C=25^{\circ}\text{C}$	100	W
T_j	Junction temperature		150	℃
T_{stg}	Storage temperature		-65~150	℃

**Silicon PNP Power Transistors****2SA1067****CHARACTERISTICS**

Tj=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	$I_C=-25mA ; I_B=0$	-120			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=-5A ; I_B=-0.5A$			-2.0	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=-5A ; I_B=-0.5A$			-2.5	V
I_{CBO}	Collector cut-off current	$V_{CB}=-120V ; I_E=0$			-0.1	mA
I_{EBO}	Emitter cut-off current	$V_{EB}=-5V ; I_C=0$			-0.1	mA
h_{FE}	DC current gain	$I_C=-3A ; V_{CE}=-4V$	60		150	
f_T	Transition frequency	$I_C=-0.5A ; V_{CE}=-10V$		50		MHz



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PACKAGE OUTLINE

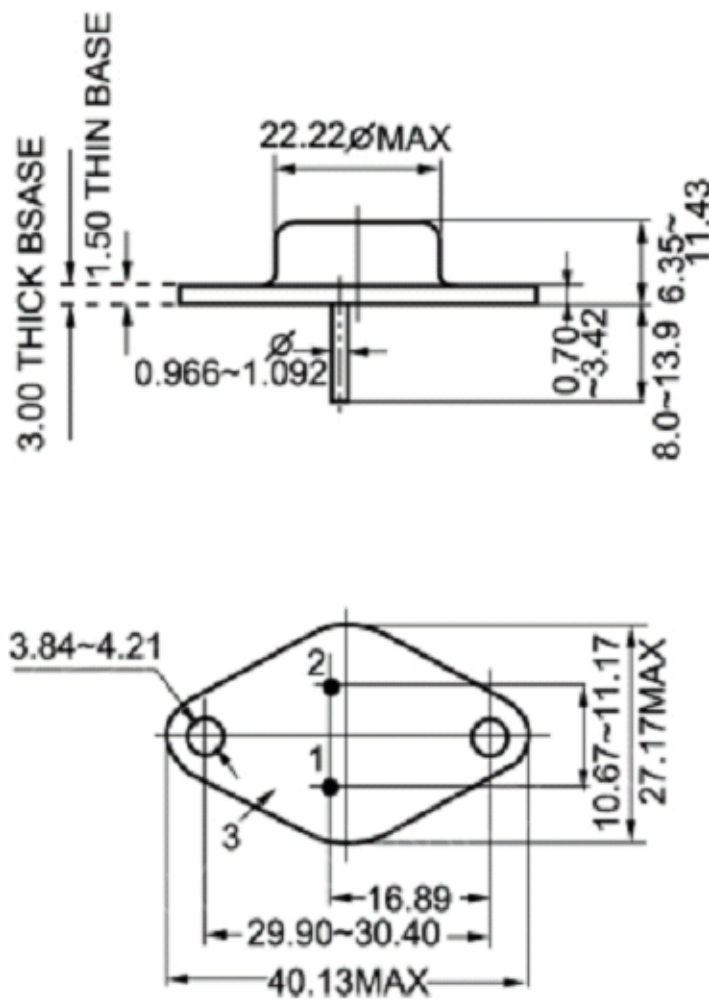


Fig.2 outline dimensions (unindicated tolerance: $\pm 0.1\text{mm}$)