Azoteq
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REGULATOR DESIGN NOTE **AZD0001**

Grant Harker

1 Introduction

The IQS17 is a fully integrated capacitive sensor with differentiated touch and proximity sensitivity, user interface and load controller IC. A number of fully integrated onboard regulators and controllers enhances the IC's performance and greatly reduces cost by eliminating any external regulators. The regulators help to ensure a stable operating voltage for reliable operation of the charge transfer circuit in both AC line and DC applications for excellent proximity sensitivity.

The purpose of this document is to assist the designer using the IQS17 in designing the regulator needed for the circuit. A variety of regulator topologies are featured, briefly describing their functional working. The advantages and disadvantages of each of these circuits are also highlighted. These circuits also function as reference design examples. Refer to the IQS17 datasheet for any additional information required. For the latest documents please refer to the AZOTEQ website at www.azoteq.com.

2 General Regulator Overview

The IQS17 has a digital filter that constantly adapts according to varying environmental factors. The filter will track slow changes like temperature drift, component aging and humidity and compensate for it. The filter is unable to suppress and adapt to any sudden shifts or sags in the supply voltage and will ultimately detect such variations as proximity conditions. For this reason it is important to design a stable regulator circuit for reliable and trouble-free operation of proximity and touch detections. The IQS17 regulators are specifically designed to input high voltage directly to the device pins by only limiting the input current to the IC.

The regulators can also be configured to operate in two- or three-wire applications. Both these setups will be discussed individually.

2.1 Series Regulator

The device has an internal series regulator to convert the input voltage V_{DDHI} to a stable regulated output voltage of 3.3V (V_{DD}). A bypass capacitor of about 100nF is required between the VDD and VSS pins. Care should be taken to limit these track lengths to the device pins. It is of utmost importance that the V_{DD} voltage must be stable at all times for reliable proximity and touch detections. For this reason this regulator is not suited to power any other external circuitry. The V_{DDHI} voltage should always be higher than the minimum specified value of 4.5V to ensure the series regulator is operating above the device's drop-out voltage.

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2.2 Shunt Regulator

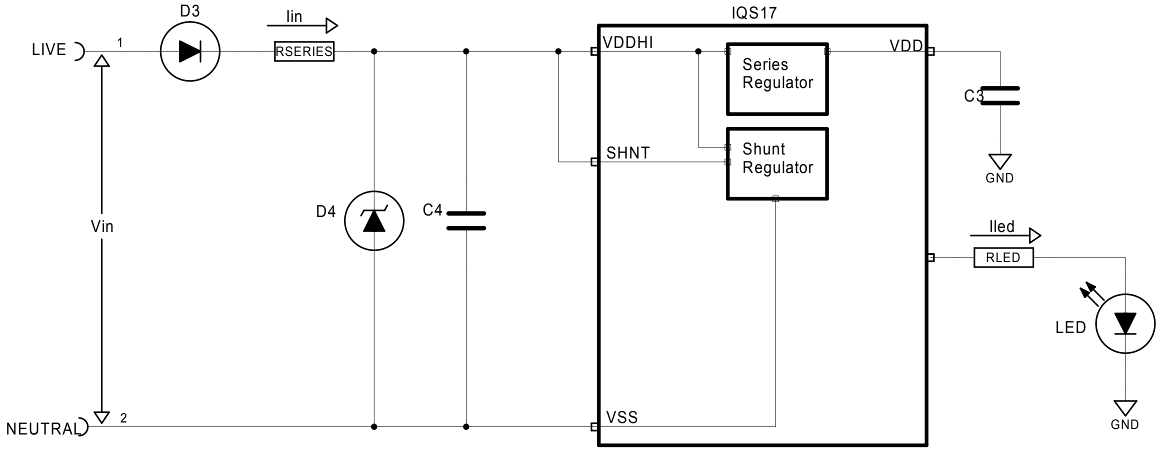

Figure 2-1

Figure 2-1 depicts a basic circuit to understand the functionality of the IQS17's SHNT pin.

A shunt regulator is formed by connecting the VDDHI and SHNT pins to each other. The input voltage will be regulated to a voltage V_{DDHI}. A series resistor connected between the supply voltage and the VDDHI pin is required to limit the shunt current to within 10mA (I_{SHNT_MAX}). If this value is exceeded, stable operation of the device is not guaranteed and false detections might occur. If a larger current needs to be shunted, the SHNT pin can be left unconnected and an external zener diode shown as D4 in Figure 2-1 can be used to replace the internal shunt regulator. The serial regulator will regulate V_{DDHI} to a stable V_{DD}. This will ensure a stable operating voltage for trouble free proximity and touch detections.

This power supply circuit is not current efficient, but is a very cost-effective solution. This circuit is recommend for three-wire DC and AC applications. The neutral connection shown above must be connected to the negative terminal for a DC powered application. This simple but elegant design eliminates the need for any costly three-terminal regulators needed for many other capacitive sensing IC's.

Table 2-1 will assist the designer in selecting the right component values for the circuit shown above. All resistor values through out this document are chosen to comply with standard SMT 1206 device ratings. For this reason more than one resistor is needed at higher operating voltages to limit the component's power consumption and maximum device voltage to an acceptable value.

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Table 2-1

Design Constraints				Design Variables			
Voltage		Current					
Type	Vin (V)	Iin (mA)	Iled (mA)	D3	C4 (µF)	RSERIES (Ω)	RLED (Ω)
DC	5	3	1	-	1	1k6	2k
DC	12	3	1	-	1	2k	3k
AC	12	3	1	BAT54	100	1k8	260
AC	110	3	1	1N4007	100	2x12k's	260
AC	220	3	1	1N4007	100	4x12k's	260

2.2.1 Series Shunt Regulator

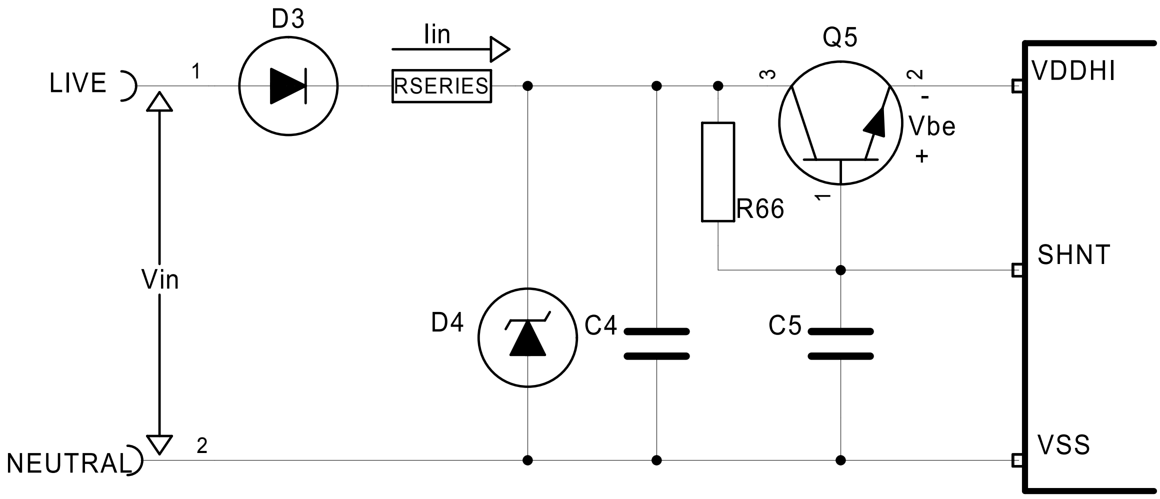

Figure 2-2

Figure 2-2 illustrates how the shunt regulator can be connected to implement a series shunt regulator. An NPN transistor is connected between the current-limiting resistor (R_{SERIES}) and the VDDHI input pin of the IC, with the base of the transistor connected to the SHNT pin. V_{DDHI} will be regulated to V_{DDHI} -V_{BE}, which is about 5.5V. This supply topology will be more power efficient, as less current will be wasted through the SHNT pin. It is very important to populate a bypass capacitor (C5) between the SHNT and VSS pins for stability reasons. A value in the region of 1uF will reduce the ripple voltage to less than 10mV. R66 should be in the order of about 100kΩ and any NPN transistor can be used as long as the device's V_{CE} and I_C ratings are not exceeded.

By using this setup a zener diode (D4) can be chosen to regulate at a higher voltage, thus achieving a two stage regulator. The higher this zener voltage the smaller the value of C4 can be. This can help reduce the size of the overall design. The advantage of this configuration is that V_{DD} is basically regulated by three stages ensuring maximum stability against any voltage

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drops or sudden current surges. Unfortunately the excess current will be dumped through D4, limiting the efficiency of the supply.

The same values provided in Table 2-1 applies to the circuit of Figure 2-2.

2.3 Boost Regulator

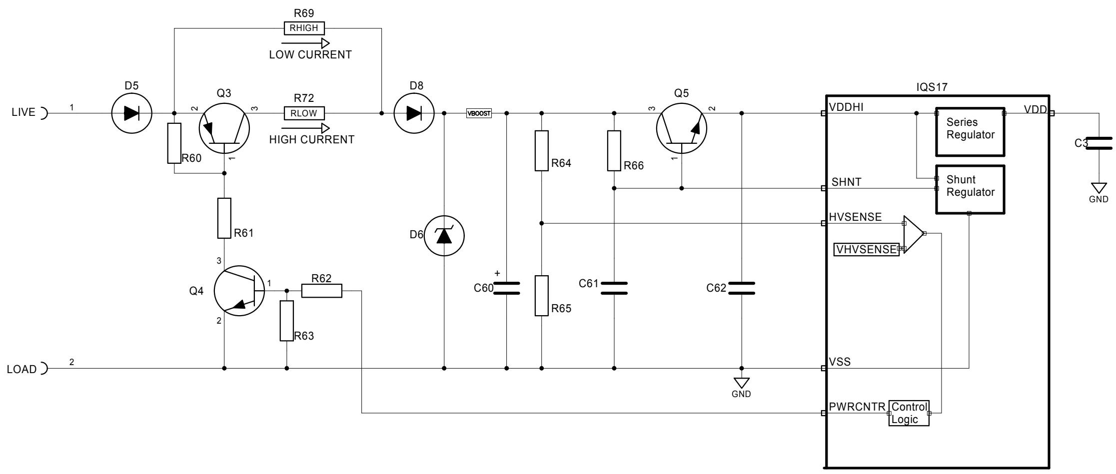

Figure 2-3

The IQS17 also contains a very power efficient regulator referred to as the boost regulator. Figure 2-3 indicates a conceptual circuit for this regulator which will be used to explain the basic functionality. This configuration is used in most two-wire applications. Refer to section 3 for an overview of the two-wire topology.

The basic idea of this circuit is to regulate the VBOOST voltage node at any adjustable level. A voltage is setup on this node and monitored by the HVSENSE input pin by means of a voltage divider circuit (formed by R64 and R65). If this voltage drops below 1.1V ($V_{HVSENSE}$) the PWRCNTR pin will become active high, switching on transistor Q4 which in turn switches on transistor Q3. This transistor then provides a low impedance high current path, allowing the voltage on the storage capacitor (C60) to rise again to the selected VBOOST voltage level.

The pulse on the PWRCNTR pin can be compared to a PWM signal adjusting the length of the ON time to the amount of current needed in the storage capacitor. If two-wire mode is selected by connecting a pull down resistor to the REOCNTR pin, the PWRCNTR pin is only activated during the T_{BOOST} period, which is at the start of every half cycle.

Once the voltage has risen higher than $V_{HVSENSE}$, the PWRCNTR will become inactive, disabling the high current path. The majority of the total current needed to power the device is supplied through this path. The function of the high impedance low current path is to supply the device with current during the start-up phase of the device.

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The function of D5 is to half-wave rectify the AC line supply while D8 protects Q3 against a high negative voltage. The purpose of D6 is to limit the maximum VBOOST voltage to an acceptable value, purely as a safety precaution for any over-voltages. If too much current is supplied through the low current path the voltage on this node may rise above the intended design value. D6 will shunt the excess current and limit the maximum voltage. The value of this zener diode should always be higher than the VBOOST voltage node.

The VBOOST voltage is regulated down to a lower voltage by means of a series shunt regulator as explained earlier.

The advantage of this supply configuration is that it conserves current, unlike the normal shunt regulator dumping any excess current. Current is only supplied when needed, minimizing the overall power consumption. It is advisable to use this regulator in most two-wire applications to ensure the device is provided with enough power when the load is on. This regulator circuit can also be used in any three-wire application if current conservation is important, but will be more costly than the normal shunt regulator circuit.

3 Two-wire Overview

Lighting wall switches are most often connected between the LIVE and the LOAD terminals as there is no access to the NEUTRAL conductor, hence the name two-wire. Figure 3-1 below illustrates a normal two-wire wall switch found in most buildings. Figure 3-2 indicates how the IQS17 replaces a standard wall switch. The IQS17 module must be connected between the LIVE and the LOAD terminals as indicated in the figure below.

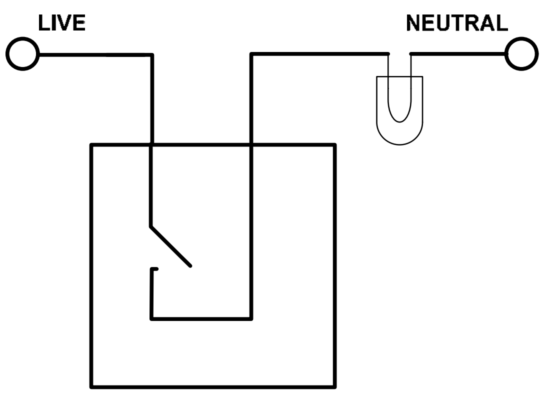

Figure 3-1

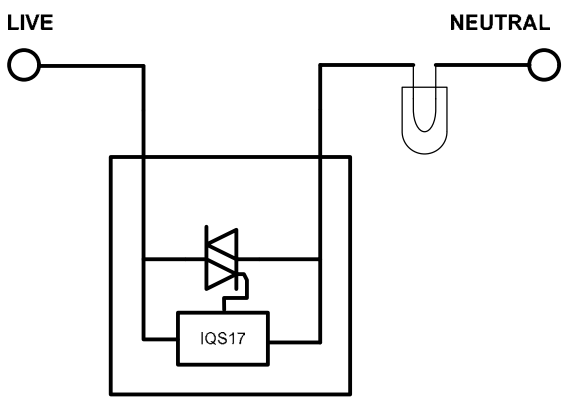

Figure 3-2

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Due to this connection type the device is not powered when the load is ON and needs to be turned OFF at discrete intervals to keep the device powered at all times. By configuring the device in two-wire, the regulators control the timing by which the load is turned ON and OFF to keep the unit powered as shown in Figure 3-2.

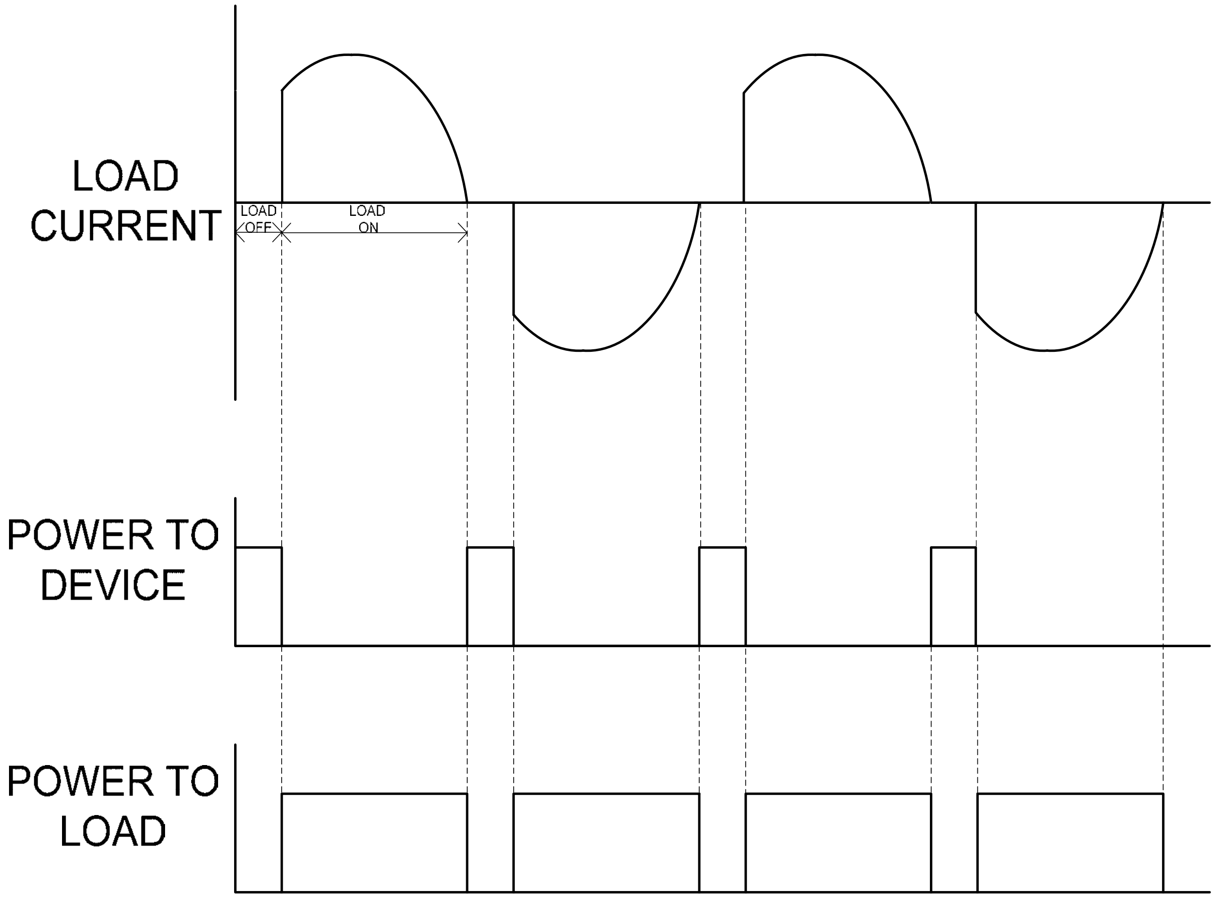

Figure 3-2

4 Reference Two-wire Schematic

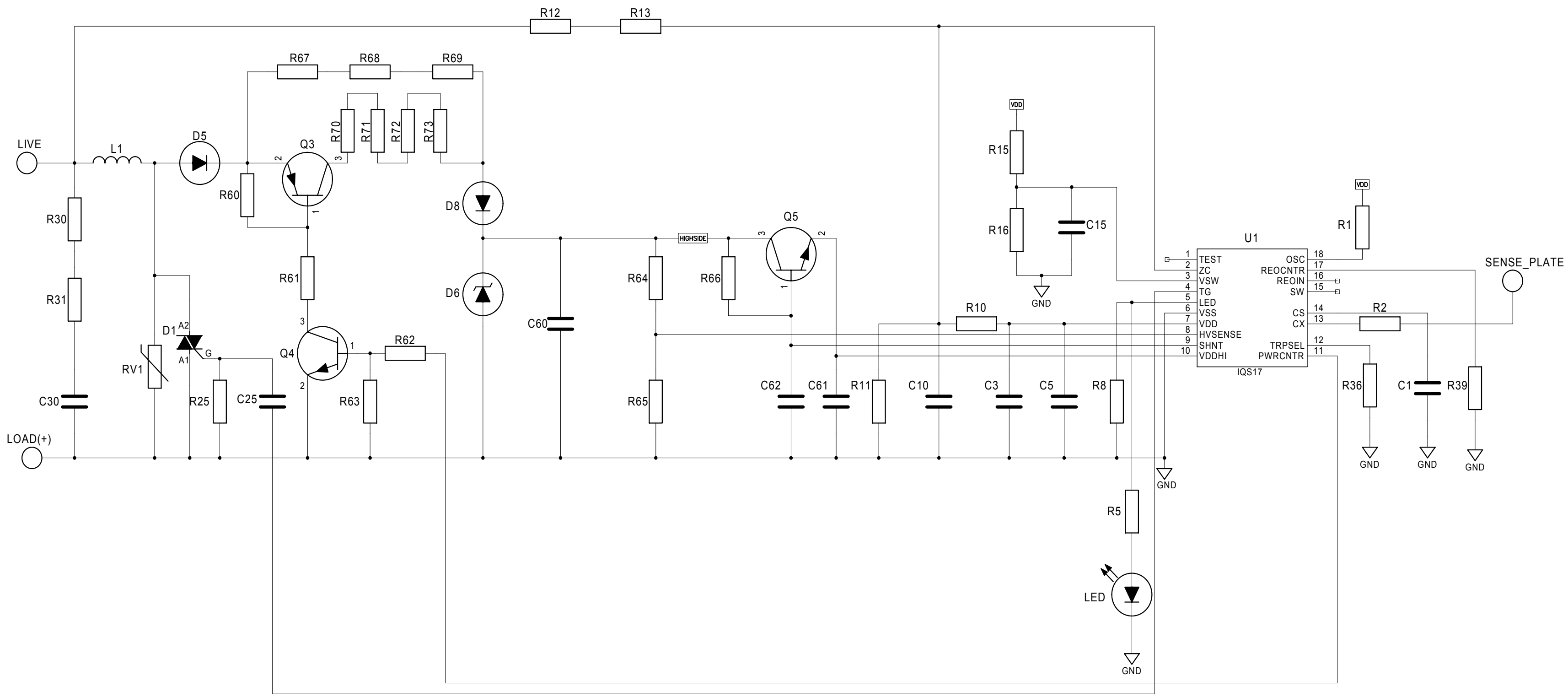

Figure 4-1

5 Reference Two-wire Design Values

220V 50Hz						115V 60Hz				
Refdes	Footprint	Value	Tollerance	Rating		Refdes	Footprint	Value	Tollerance	Rating
R 1	RES-0603	18k	5%			R 1	RES-0603	18k	5%	
R 2	RES-0603	2k	5%			R 2	RES-0603	2k	5%	
R 5	RES-0603	1k	5%			R 5	RES-0603	1k	5%	
R 8	RES-0603	100k	5%			R 8	RES-0603	100k	5%	
R 10	RES-0603	1M	1%			R 10	RES-0603	1M	1%	
R 11	RES-0603	1M	1%			R 11	RES-0603	1M	1%	
R 12	RES-1206	510k	5%			R 12	RES-1206	510k	5%	
R 13	RES-1206	510k	5%			R 13	RES-1206	510k	5%	
R 15	RES-0603	1M	1%			R 15	RES-0603	1M	1%	
R 16	RES-0603	1M	1%			R 16	RES-0603	1M	1%	
R 25	RES-0603	10k	5%			R 25	RES-0603	10k	5%	
R 30	RES-1206	2k7	5%			R 30	RES-1206	2k7	5%	
R 31	RES-1206	2k7	5%			R 31	RES-1206	2k7	5%	
R 36	RES-0603	DNP	5%			R 36	RES-0603	DNP	5%	
R 39	RES-0603	10k	5%			R 39	RES-0603	10k	5%	
R 60	RES-0603	30k	5%			R 60	RES-0603	30k	5%	
R 61	RES-1206	6k2	5%			R 61	RES-1206	6k2	5%	
R 62	RES-0603	10k	5%			R 62	RES-0603	10k	5%	
R 63	RES-0603	100k	5%			R 63	RES-0603	100k	5%	
R 64	RES-0603	820k	5%			R 64	RES-0603	820k	5%	
R 65	RES-0603	39k	5%			R 65	RES-0603	39k	5%	
R 66	RES-1206	100k	5%			R 66	RES-1206	100k	5%	
R 67	RES-1206	22k	5%			R 67	RES-1206	11k	5%	
R 68	RES-1206	22k	5%			R 68	RES-1206	11k	5%	
R 69	RES-1206	22k	5%			R 69	RES-1206	11k	5%	
R 70	RES-1206	68	5%			R 70	RES-1206	15	5%	
R 71	RES-1206	68	5%			R 71	RES-1206	15	5%	
R 72	RES-1206	68	5%			R 72	RES-1206	15	5%	
R 73	RES-1206	68	5%			R 73	RES-1206	15	5%	
C1	CAP-0603	220nF	20%	50V X7R		C1	CAP-0603	220nF	20%	50V X7R
C3	CAP-0603	100pF	20%	16V X7R		C3	CAP-0603	100pF	20%	16V X7R
C5	CAP-0603	100nF	20%	50V X7R		C5	CAP-0603	100nF	20%	50V X7R
C10	CAP-0603	1nF	20%	50V X7R		C10	CAP-0603	1nF	20%	50V X7R
C15	CAP-0603	100pF	20%	16V X7R		C15	CAP-0603	100pF	20%	16V X7R
C25	CAP-0603	100nF	20%	50V X7R		C25	CAP-0603	100nF	20%	50V X7R
C30*	Discrete			275VAC Type X2		C30*	Discrete			275VAC Type X2
C60	Electrolytic	4.7uF	20%	EXR 50V		C60	Electrolytic	4.7uF	20%	EXR 50V
C61	CAP-0603	100nF	20%	16V X7R		C61	CAP-0603	100nF	20%	16V X7R
C62	CAP-0603	1uF	20%	50V X7R		C62	CAP-0603	1uF	20%	50V X7R
D1	TO220	BTA08-800				D1	TO220	BTA08-800		
D5	MELF	1N4007				D5	MELF	1N4007		
D6	SOD123	33V				D6	SOD123	33V		
D8	MELF	1N4007				D8	MELF	1N4007		
Q3	SOT23	MMBTA94				Q3	SOT23	MMBTA94		
Q4	SOT23	MMBTA44				Q4	SOT23	MMBTA44		
Q5	SOT23	S9014				Q5	SOT23	S9014		
RV1	Discrete	07D391k				RV1	Discrete	07D391k		
L1*	Toroid					L1*	Toroid			
LED	3mm					LED	3mm			
U1	SSOP	IQS17				U1	SSOP	IQS17		

* Dependant on local EMC regulations

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6 Three-wire Overview

If it is possible to access the LIVE and NEUTRAL conductors as shown in Figure 6-1 the device can be operated in three-wire mode. Figure 6-2 depicts how the IQS17 is connected in a standard three-wire setup. The IQS17 must be connected between the LIVE and NEUTRAL terminals. Unlike in the two-wire supply setup, the unit will constantly be powered in the three-wire configuration. This greatly reduces the supply complexity and cost.

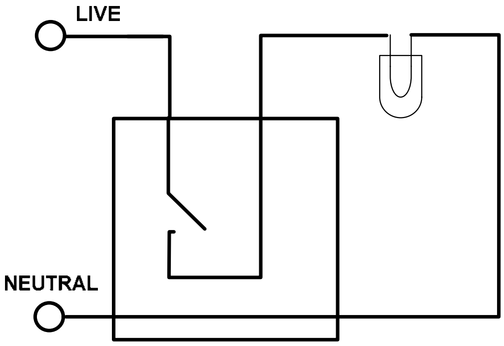

Figure 6-1

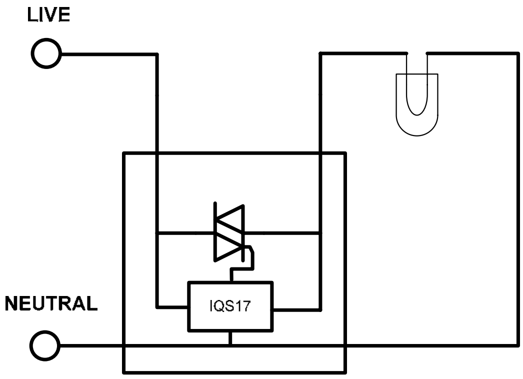

Figure 6-2

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7 Reference Three-wire Schematic

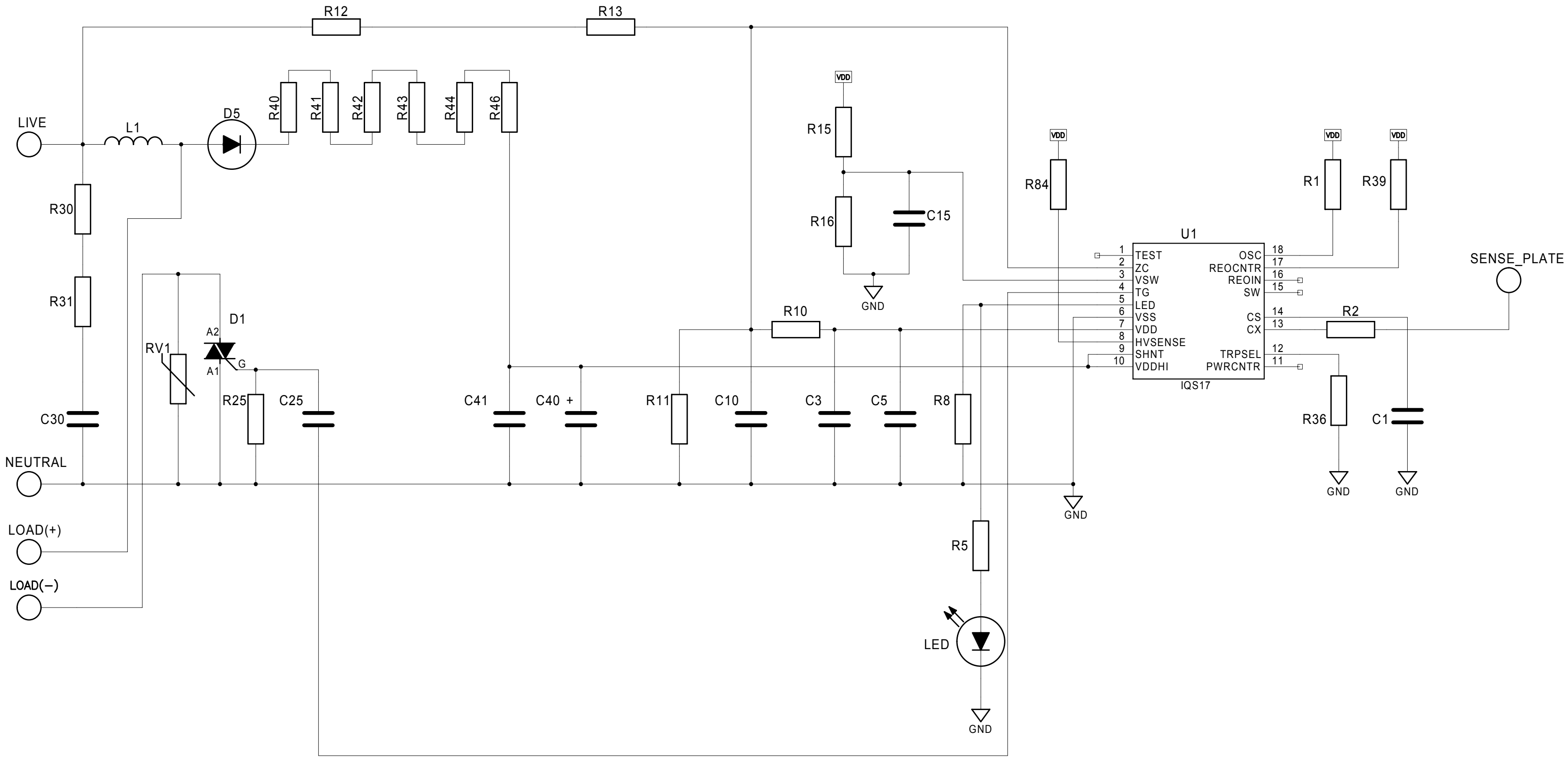

Figure 7-1

8 Reference Three-wire Design Values

220V 50Hz						115V 60Hz				
Refdes	**Footprint**	**Value**	**Tollerance**	**Rating**		**Refdes**	**Footprint**	**Value**	**Tollerance**	**Rating**
R 1	RES-0603	18k	5%			R 1	RES-0603	18k	5%	
R 2	RES-0603	2k	5%			R 2	RES-0603	2k	5%	
R 5	RES-0603	260	5%			R 5	RES-0603	260	5%	
R 8	RES-0603	100k	5%			R 8	RES-0603	100k	5%	
R 10	RES-0603	1M	1%			R 10	RES-0603	1M	1%	
R 11	RES-0603	1M	1%			R 11	RES-0603	1M	1%	
R 12	RES-1206	510k	5%			R 12	RES-1206	510k	5%	
R 13	RES-1206	510k	5%			R 13	RES-1206	510k	5%	
R 15	RES-0603	1M	1%			R 15	RES-0603	1M	1%	
R 16	RES-0603	1M	1%			R 16	RES-0603	1M	1%	
R 25	RES-0603	10k	5%			R 25	RES-0603	10	5%	
R 30	RES-1206	2k7	5%			R 30	RES-1206	2k7	5%	
R 31	RES-1206	2k7	5%			R 31	RES-1206	2k7	5%	
R 36	RES-0603	DNP	5%			R 36	RES-0603	DNP	5%	
R 39	RES-0603	10k	5%			R 39	RES-0603	10k	5%	
R 40	RES-1206	6k2	5%			R 40	RES-1206	3k	5%	
R 41	RES-1206	6k2	5%			R 41	RES-1206	3k	5%	
R 42	RES-1206	6k2	5%			R 42	RES-1206	3k	5%	
R 43	RES-1206	6k2	5%			R 43	RES-1206	3k	5%	
R 44	RES-1206	6k2	5%			R 44	RES-1206	3k	5%	
R 46	RES-1206	6k2	5%			R 46	RES-1206	3k	5%	
R 84	RES-0603	18k	5%			R 84	RES-0603	18k	5%	
C1	CAP-0603	220nF	20%	50V X7R		C1	CAP-0603	220nF	20%	50V X7R
C3	CAP-0603	100pF	20%	16V X7R		C3	CAP-0603	100pF	20%	16V X7R
C5	CAP-0603	100nF	20%	50V X7R		C5	CAP-0603	100nF	20%	50V X7R
C10	CAP-0603	1nF	20%	50V X7R		C10	CAP-0603	1nF	20%	50V X7R
C15	CAP-0603	100pF	20%	16V X7R		C15	CAP-0603	100pF	20%	16V X7R
C25	CAP-0603	100nF	20%	50V X7R		C25	CAP-0603	100nF	20%	50V X7R
C30*	Discrete			275VAC Type X2		C30	Discrete	100nF	20%	275VAC
C40	Electrolytic	100uF	20%	EXR 16V		C40	Electrolytic	100uF	20%	EXR 16V
C41	CAP-0603	1nF	20%	50V X7R		C41	CAP-0603	1nF	20%	50V X7R
D1	TO220	BTA08-800				D1	TO220	BTA08-800		
D5	MELF	1N4007				D5	MELF	1N4007		
RV1	Discrete	07D391k				RV1	Discrete	07D391k		
L1*	Toroid					L1	Toroid	1mH		
LED	3mm					LED	3mm			
U1	SSOP	IQS17				U1	SSOP	IQS17		

* Dependant on local EMC regulations

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Design Note Revision History

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This is a new document containing the production silicon parameters

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This device is covered by the following patents; US6984900, US6952084, US6650066, US6621225, US6249089, EP1530178B1, EP1308913B1, EP1206168B1, EP1120018B1. More patents are pending.

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