Application

- IEEE 802.11b
- 2.4GHz Cordless Phones

Features

- Fully designed and tested 802.11b transmitter front-end using the SE2520L power amplifier
- Demonstrates the capabilities of the SE2520L in 802.1b applications
- Optimized matching networks and harmonic filter
- Power Detector, Rx/Tx Switch and Diversity Switch included
- Ready to be designed into production.

Product Description

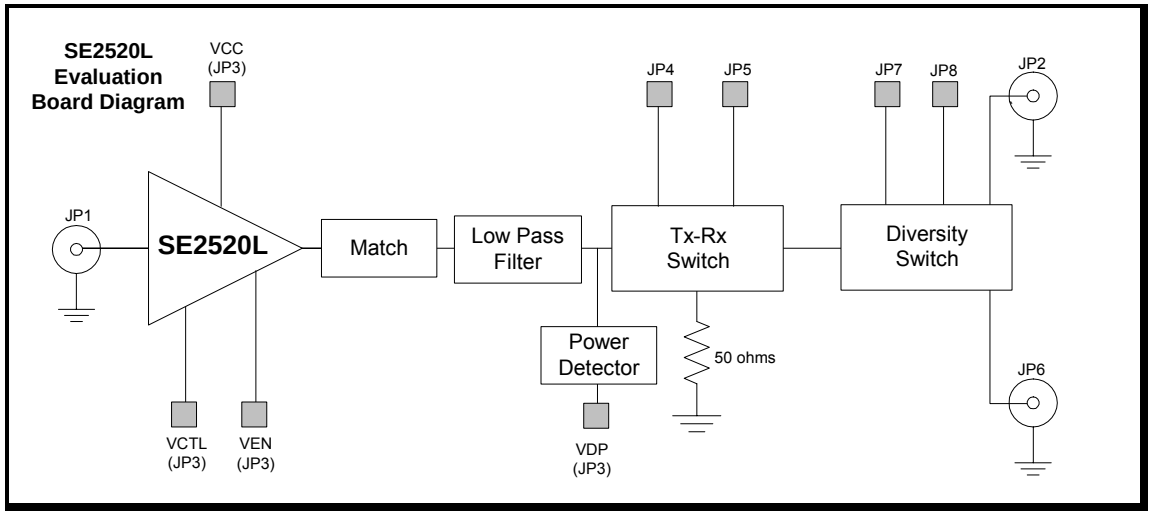
The SE2520L-EK3 Evaluation Kit is a tool that is intended to demonstrate the advantages of the RangeCharger™ SE2520L Power Amplifier and assist customers into full-scale production. The board facilitates evaluation, experimentation and investigation with various modes of operation of the SE2520L. The board demonstrates the SE2520L in an application where matching, filtering, and switching are employed. The SE2520L-EK3 design and layout can be quickly and easily transferred into a production design.

The SE2520L-EK3 Evaluation Kit comprises of an SE2520L-EV3 evaluation board with 50Ω termination, an SE2520L-EK3 datasheet, and an SE2520L datasheet.

Order Information

Type	Package	Remark
SE2520L-EK3	N/A	None

Functional Block Diagram



Picture

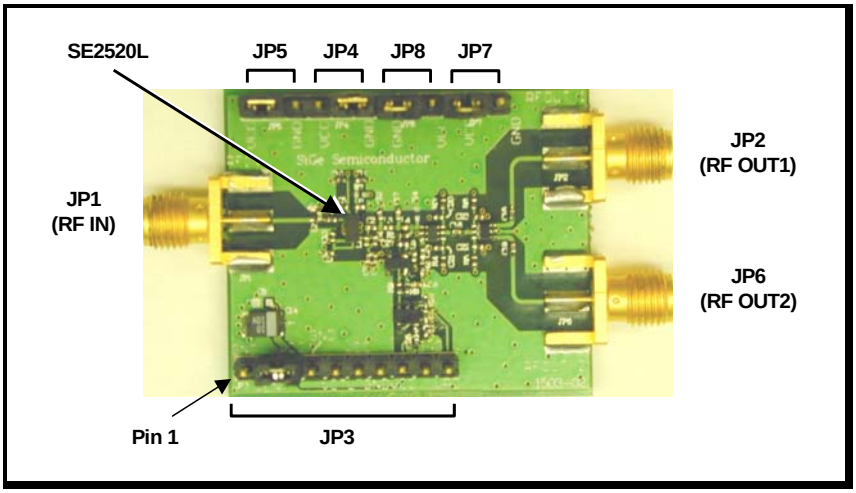


Figure 1: SE2520L-EV3

Contents Of Evaluation Kit

Quantity	Description	Reference
1	SE2520L Evaluation Board	SE2520L-EV3
1	SE2520L Evaluation Kit Datasheet	15-DST-02
1	SE2520L Datasheet	15-DST-01
1	50Ω Termination	

Table 1: Contents of Evaluation Kit

Configuration

Tables 2, 3 and 4 describe how the evaluation board can be configured. The evaluation kit is pre-configured when shipped to operate with the SE2520L enabled, in transmit mode, at maximum gain, with the signal output on JP2, and a 50Ω termination on JP6.

RF Input

A signal generator can be connected on header JP1 to drive the SE2520L which is matched to 50Ω. The recommended power level for 802.11b operation is approximately -8dBm. It is recommended to keep the input power level to a maximum of +8dBm to avoid potential damage of the SE2520L.

RF Outputs

The RF output can be measured on either JP2 or JP6 pending the setting of a diversity switch included on the evaluation board. The diversity switch settings are described in Table 4. It is recommended to terminate the unused RF output port with a 50Ω termination to avoid possible reflections.

A receive mode can be emulated where RF outputs JP2 or JP3 are routed to a 50Ω termination via an Rx/Tx switch on the evaluation board. Table 3 describes how to control the Rx/Tx switch.

Power and DC Controls

The board is powered from a single 3.3V supply that is connected to the 4mm connectors on the board. +3.3V should be connected to pin 8 (V_{CC}) on JP3 and GND to pin 7 on JP3.

The SE2520L offers an analog power control and a digital enable/disable feature. To enable the SE2520L, jumper pins 2 and 3 on JP3. To disable the SE2520L, jumper pins 1 and 2 on JP3. A control voltage between 0V and 3.3V can also be applied on pin 5 of JP3 to set the amplifier gain thereby controlling the output power. Refer to the SE2520L data sheet for the relationship between power control pin voltage and output power. Jumper settings can also be employed to control gain. For maximum gain, jumper pins 5 and 6 on JP3. For minimum gain, jumper pins 4 and 5.

JP3 Header Pins	Description
8	3.3V (V_{CC}) Supply Connection
7	Ground (GND) Connection
5	Gain Control Connection (VCTL), 0 – 3.3V
Jumper Pins 5 and 6	Maximum Gain
Jumper Pins 4 and 5	Minimum Gain
Jumper Pins 2 and 3	Enables SE2520L
Jumper Pins 1 and 2	Disables SE2520L

Table 2: JP3 Header Settings

Receive or transmit mode can be selected via an Rx/Tx switch on the evaluation board. Settings are described in Table 3 below.

Mode	Short JP4 To	Short JP5 To
Transmit	GND	V_{CC}
Receive	V_{CC}	GND
Illegal Mode	GND	GND
Illegal Mode	V_{CC}	V_{CC}

Table 3: Rx/Tx Switch Jumper Settings

The evaluation board includes an antenna diversity switch. The RF output (JP2 or JP6) selection is described in Table 4 below.

RF Output	Short JP7 To	Short JP8 To
JP2 (Antenna 1)	V_{CC}	GND
JP6 (Antenna 2)	GND	V_{CC}
Illegal Mode	GND	GND
Illegal Mode	V_{CC}	V_{CC}

Table 4: RF Output Selection Jumper Settings

Power Detector Output

As shown in Figure 1, pin 10 (VPD) of header JP3 on the evaluation board is used to measure the output power. This output level is a voltage that changes with respect to the output power level, as shown in Figure 2. This detector can be used to monitor the average output power of the antenna connector, allowing the dynamic control of its output.

Note: The transfer function shown in Figure 2 is valid when the evaluation board is operating with a 3.3 volt DC supply with its output terminated in 50Ω.

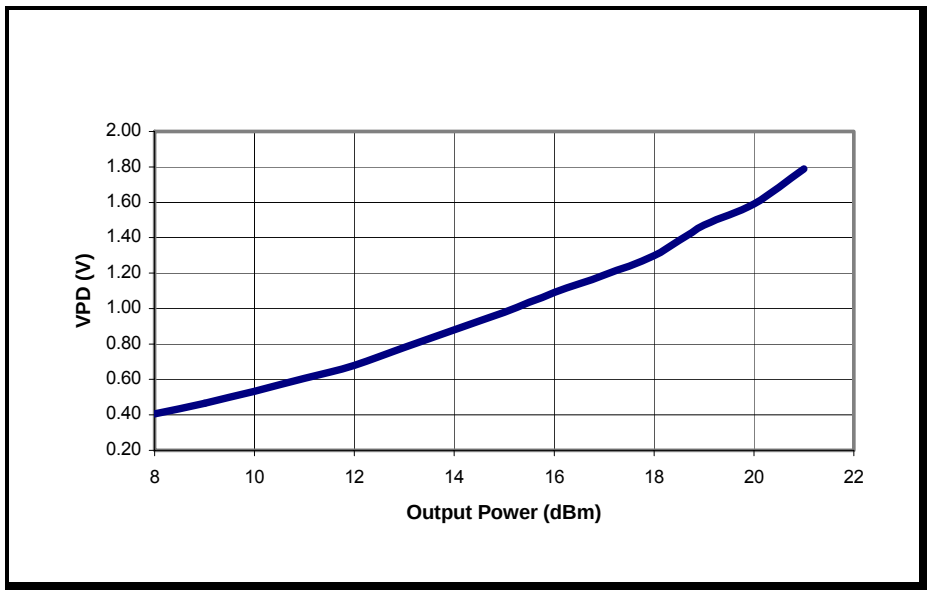


Figure 2: Typical Power Detector Output (VPD) vs. Output Power Characteristic

Evaluation Board Schematic

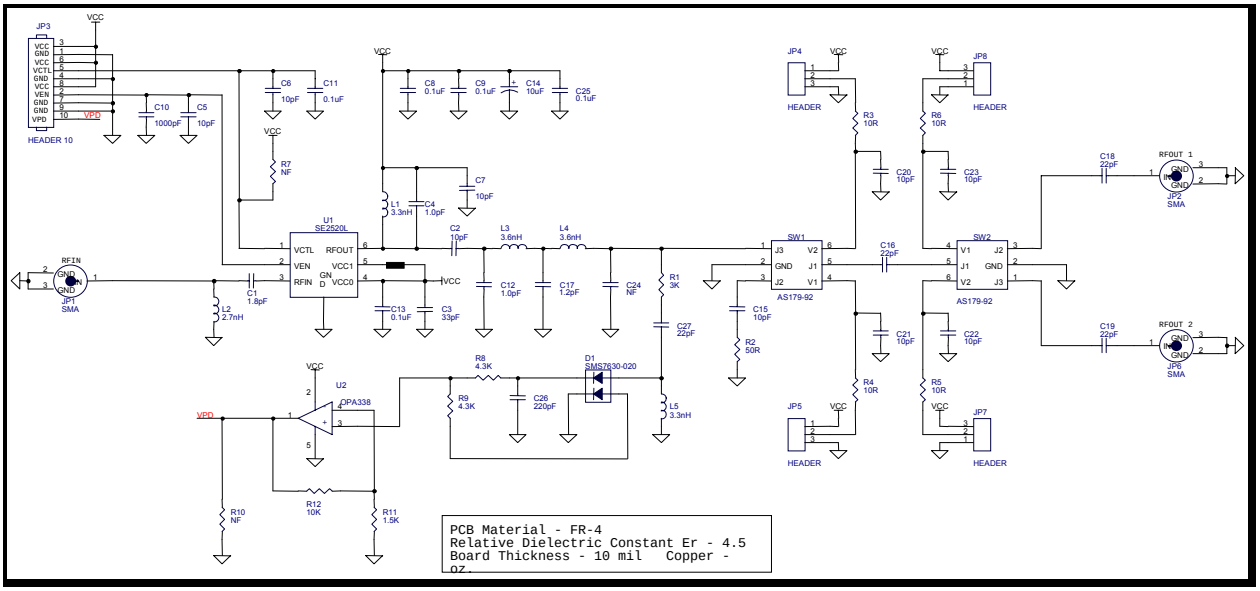


Figure 3: Evaluation Board Schematic Diagram

Evaluation Board Bill Of Materials

Item	Qty	Reference	Part Description	Supplier Information
1	5	C11,C13,C25,C8,C9	0.1uF	Murata - GRP155R61A104KA01
2	2	C12,C4	1.0pF	Murata - GRP1555C1H1R0CZ01
3	1	C17	1.2pF	Murata - GRP1555C1H1R2CZ01
4	1	C1	1.8pF	Murata - GRP1555C1H1R8CZ01
5	1	C10	1000pF	Murata - GRP155R71H102KA01
6	9	C15,C2,C20,C21,C22,C23, C5,C6,C7	10pF	Murata - GRP1555C1H100JZ01
7	1	C14	10uF	Panasonic - ECST1AX106R
8	1	C26	220pF	Murata - GRP155R71H221KA01
9	4	C16,C18,C19,C27	22pF	Murata - GRP1555C1H220JZ01
10	1	C3	33pF	Murata - GRP1555C1H330JZ01
11		C24	NF	
12	1	L2	2.7nH	Murata - LQP15MN2N7B02B
13	2	L1,L5	3.3nH	Murata - LQP15MN3N3B02B
14	2	L3,L4	3.6nH	Murata - LQP15MN3N6B02B
15	1	R11	1.5KΩ	N/A
16	4	R3,R4,R5,R6	10KΩ	N/A
17	1	R12	6.8KΩ	N/A
18	1	R1	3KΩ	N/A
19	2	R8,R9	4.3KΩ	N/A
20	1	R2	50Ω	N/A
21		R10	Not Fitted (NF)	
22		R7	Not Fitted (NF)	
23	1	D1	Diode	Alpha - SMS7630-020
24	3	JP1, JP2, JP6	SMA RF Connector	Johnson - 142-0701-886
25	22 pins	JP3,JP4,JP5,JP7,JP8	10 and 12 pin 0.1" pitch through header	3M - 929647-09-36-I
26	2	SW1, SW2	RF Switch	Alpha - AS179-92
27	1	U1	Power Amplifier	SiGe - SE2520L
28	1	U2	Op Amp	TI - OPA338
29	1		PCB - FR4	
30	1		50Ω Termination	

Table 5: Evaluation Kit Bill of Materials

Evaluation Board Layout

Optimum layout of the evaluation board is critical. The input and output matching networks are dependent on the layout for the values of the output power, power added efficiency, current consumption, and harmonics generation.

RF tracks should be as short as possible to reduce losses and minimize RF power emissions. The exposed pad at the bottom of the package is the ground connection for the IC. The ground vias should be placed as close as possible to this pad. All V_{CC} lines should be decoupled as close as possible to the IC pins, and the ground end of the decoupling capacitors should have the shortest path to the IC ground possible.

The SE2520L requires three matching networks: input matching, inter-stage matching via its V_{CC1} pin and output matching. In total, only 7 critical components are required: 5 capacitors and 2 inductors. For specific performance tuning and power supply decoupling, additional components may be used.

Input Matching	The SE2520L's input impedance (Zin) at Pin = -8dBm and F=2.45GHz is Zin = (12+j*1.2)Ω. For maximum gain, the input of the SE2520L should be conjugately matched, i.e. Zs = (Zin)* = (12-j*1.2)Ω.
Interstage Matching	The matching of the output of the first stage and input of the second stage is merged and requires the use of only one capacitor. The capacitor shown in the schematic on page 1, C3, is required for decoupling only. The dimensions of the microstrip line shown on Vcc1 is 10mils x 100mils. (FR4, 10mil thickness, top-ground).
Output Matching	The SE2520L-EK3 is designed as to maximize the SE2520L's 1dB Compression Point (P1dB). A load impedance of ZL = (31.9+j*14.6)Ω is presented to the output of the PA. This is achieved with components L1, C2 and C4. Components C12, L3 and L4 form a low-pass filter to reduce the harmonics below FCC regulations.

Table 6: Evaluation Board Matching Arrangement

Note: Layout diagrams shown in Figures 4, 5, 6, 7, 8 and 9 are for information purposes only. They may not correctly show all traces, and are not to scale. Please contact your SiGe Semiconductor sales representative for the proper layout files.

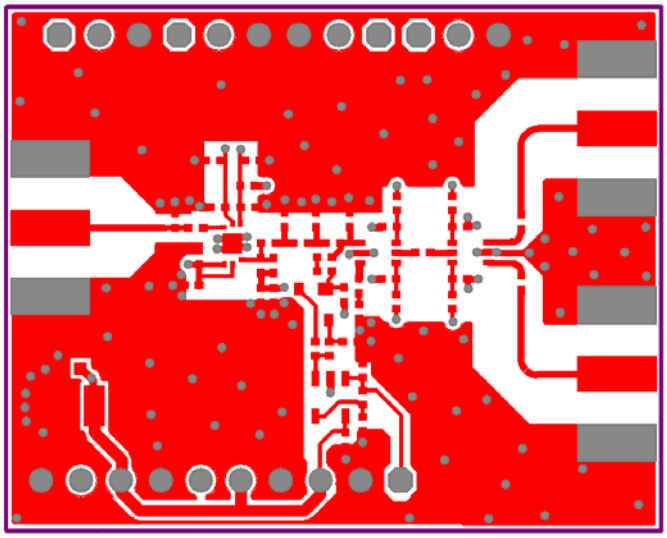


Figure 4: Copper Layer 1

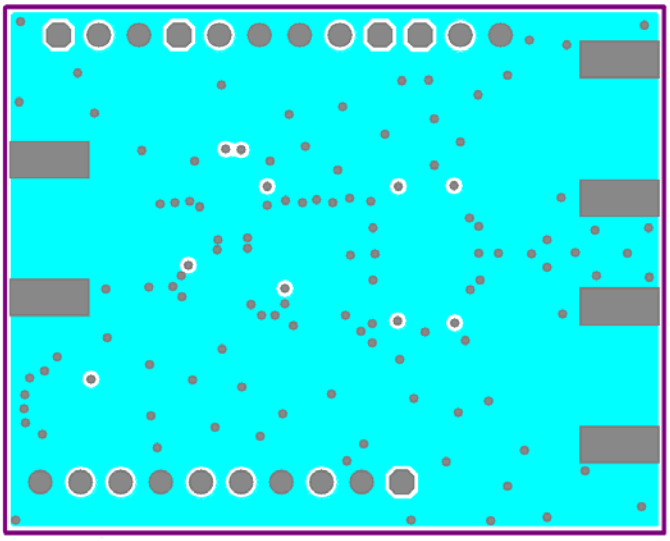


Figure 5: Copper Layer 2 (Ground Plane)

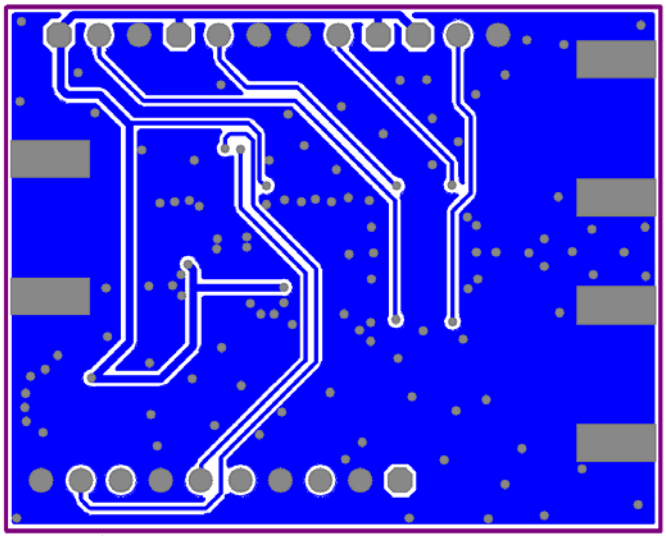


Figure 6: Copper Layer 3

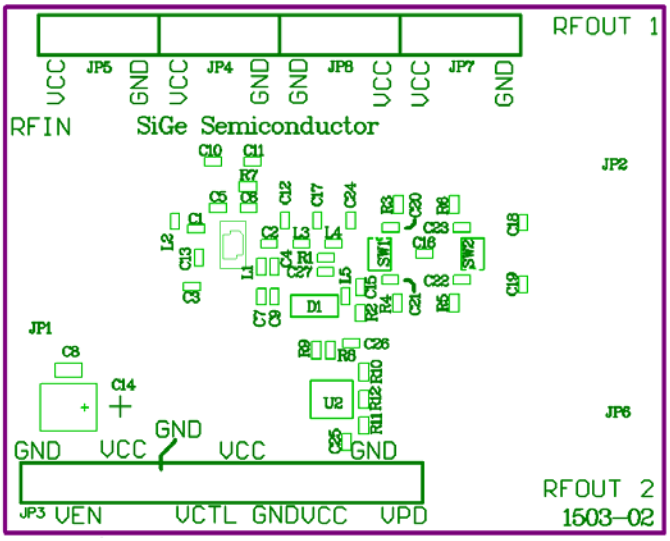


Figure 7: Component Placement

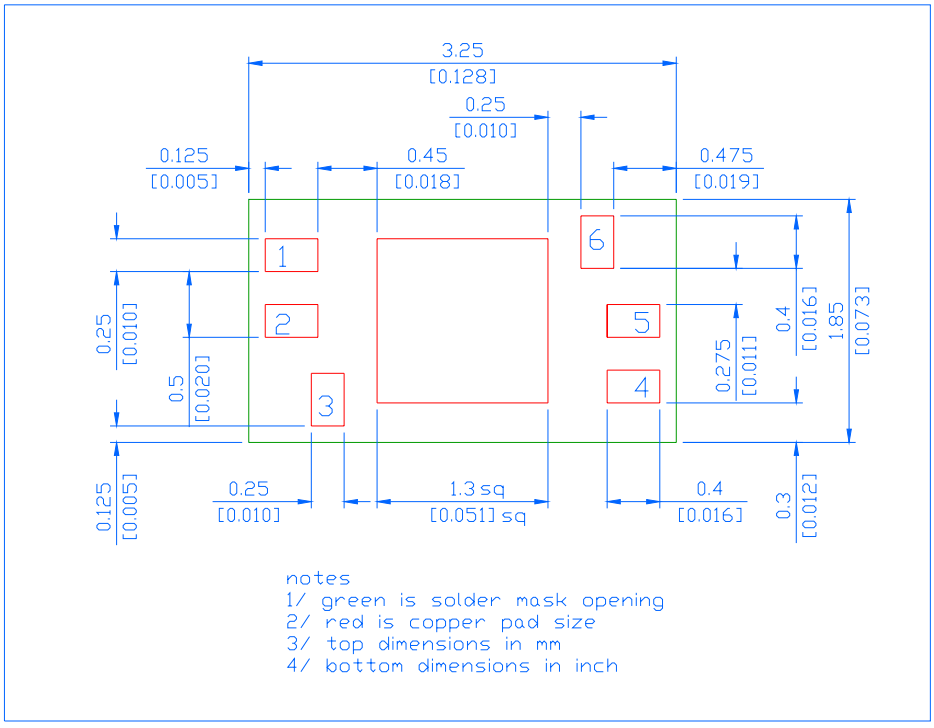
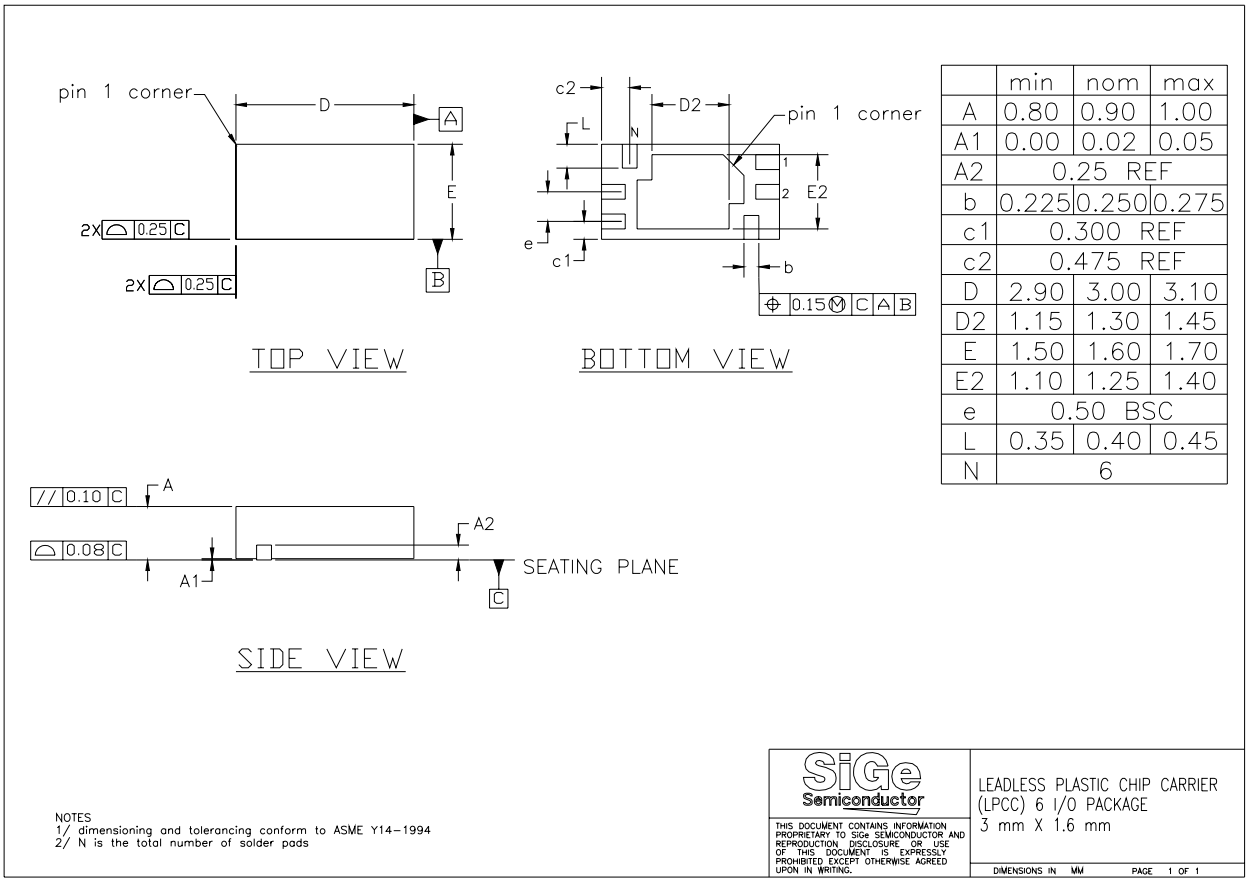


Figure 8: 6-Pin LPCC Printed Circuit Board Footprint



	min	nom	max
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.25 REF	
b	0.225	0.250	0.275
c1		0.300 REF	
c2		0.475 REF	
D	2.90	3.00	3.10
D2	1.15	1.30	1.45
E	1.50	1.60	1.70
E2	1.10	1.25	1.40
e		0.50 BSC	
L	0.35	0.40	0.45
N		6	

Figure 9: 6-Pin LPCC Package Drawing

Notes:
1. Dimensions are in millimeters
2. Tolerance 0.1mm unless otherwise specified
3. Moisture/ Reflow Sensitivity Classification: Level 1 (IPC/JEDEC-J-STD-020A)
4. Exposed heat/electrical ground pad at bottom of package
5. Lead finish is 100% lead-free electrolytic tin.

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