



## Frequency Generator & Integrated Buffers for PIII & Tualatin™

### Recommended Application:

815B Solano B step style chipset

### Output Features:

- 2 - CPUs @ 2.5V, up to 133MHz.
- 13 - SDRAM @ 3.3V, up to 133MHz.
- 3 - 3V66 @ 3.3V, 2x PCI MHz.
- 8 - PCI @ 3.3V
- 1 - 48MHz, @ 3.3V fixed
- 1 - 24/48MHz @ 3.3V
- 1 - REF @ 3.3V, 14.318MHz.
- 1 - IOAPIC @ 2.5V 16.67MHz.

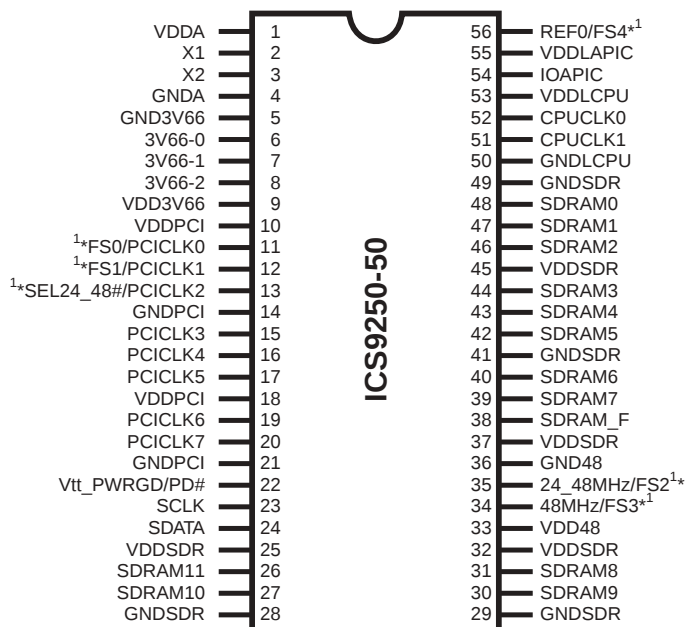
### Features:

- Support PC133 SDRAM.
- Up to 133MHz frequency support
- Support power management through PD#
- Spread spectrum for EMI control ( $\pm 0.25\%$  Center Spread or 0 to  $-0.5\%$  down spread)
- Uses external 14.318MHz crystal
- FS pins for frequency select

### Key Specifications:

- CPU Output Jitter: <250ps
- CPU Output Skew: <175ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <175ps
- For group skew timing, please refer to the Group Timing Relationship Table.

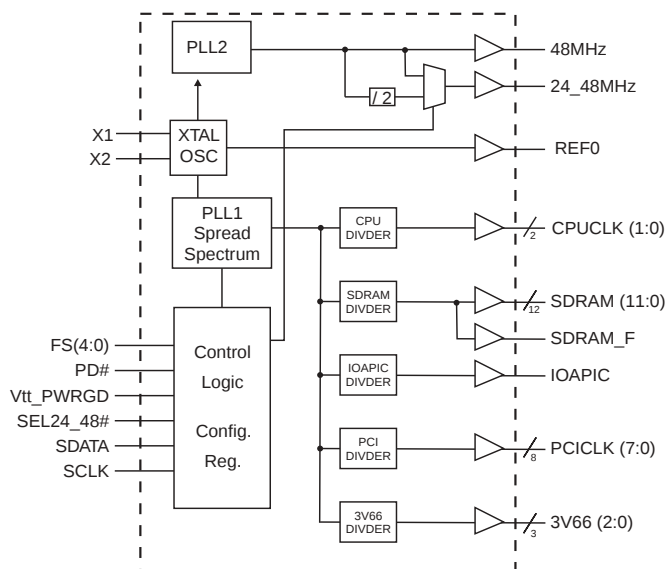
### Pin Configuration



### 56-Pin 300 mil SSOP

1. These pins will have 1.5 to 2X drive strength.  
\* 120K ohm pull-up to VDD on indicated inputs.

### Block Diagram



### Functionality

| FS4 | FS3 | FS2 | FS1 | FS0 | CPU    | SDRAM  | 3V66  | PCI   |
|-----|-----|-----|-----|-----|--------|--------|-------|-------|
| 0   | 0   | 0   | 0   | 0   | 66.67  | 100.00 | 66.67 | 33.33 |
| 0   | 1   | 0   | 0   | 0   | 100.00 | 100.00 | 66.67 | 33.33 |
| 1   | 0   | 0   | 0   | 0   | 133.33 | 133.33 | 66.67 | 33.33 |
| 1   | 1   | 0   | 0   | 0   | 133.33 | 100.00 | 66.67 | 33.33 |

For other hardware/I<sup>2</sup>C selectable frequencies please refer to Byte 0 frequency select register.

### Power Groups

VDD48 = Fixed PLL power  
GND48 = Fixed PLL GND  
VDDA = Power for CPU PLL  
GNDA = GND for CPU PLL



## General Description

The **ICS9250-50** is a single chip clock solution for desktop designs using the 810/810E, Solano and Solano B- Step style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I<sup>2</sup>C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-50 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I<sup>2</sup>C interface allows changing functions, stop clock programming and frequency selection.

## Pin Configuration

| PIN NUMBER                                     | PIN NAME     | TYPE | DESCRIPTION                                                                                                                                                                                                                   |
|------------------------------------------------|--------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                              | VDDA         | PWR  | 3.3V analog power supply for fixed PLL                                                                                                                                                                                        |
| 9, 10, 18, 25, 32, 33, 37, 45                  | VDD          | PWR  | 3.3V power supply                                                                                                                                                                                                             |
| 2                                              | X1           | IN   | Crystal input, has internal load cap (33pF) and feedback resistor from X2                                                                                                                                                     |
| 3                                              | X2           | OUT  | Crystal output, nominally 14.318MHz. Has internal load cap (33pF)                                                                                                                                                             |
| 4                                              | GNDA         | PWR  | Analog Ground pin for 3.3V supply for fixed PLL                                                                                                                                                                               |
| 5, 14, 21, 28, 29, 36, 41, 49                  | GND          | PWR  | Ground pins for 3.3V supply                                                                                                                                                                                                   |
| 8, 7, 6                                        | 3V66 (2:0)   | OUT  | 3.3Vclock outputs for HUB @ 2X PCI frequency                                                                                                                                                                                  |
| 11                                             | PCICLK0      | OUT  | 3.3V PCI clock outputs                                                                                                                                                                                                        |
|                                                | FS0          | IN   | Logic input frequency select bit. Input latched at power on.                                                                                                                                                                  |
| 12                                             | PCICLK1      | OUT  | 3.3V PCI clock outputs.                                                                                                                                                                                                       |
|                                                | FS1          | IN   | Logic input frequency select bit. Input latched at power on.                                                                                                                                                                  |
| 20, 19, 17, 16, 15                             | PCICLK (7:3) | OUT  | 3.3V PCI clock outputs.                                                                                                                                                                                                       |
| 13                                             | PCICLK2      | OUT  | 3.3V PCI clock output.                                                                                                                                                                                                        |
|                                                | SEL24_48#    | IN   | Input logic select. When logic "0" is selected pin 35 = 48MHz<br>When logic "1" is selected pin 35 = 24MHz.                                                                                                                   |
| 22                                             | Vtt_PWRGD    | IN   | This pin acts as a dual function input pin for Vtt_PWRGD and PD# signal. When Vtt_PWRGD goes high the frequency select will be latched at power on thereafter the pin is an asynchronous active low power down pin.           |
|                                                | PD#          | IN   | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 23                                             | SCLK         | IN   | Clock input of I <sup>2</sup> C serial input.                                                                                                                                                                                 |
| 24                                             | SDATA        | IN   | Data input for I <sup>2</sup> C serial input.                                                                                                                                                                                 |
| 34                                             | 48MHz        | OUT  | 3.3V Fixed 48MHz clock output for USB.                                                                                                                                                                                        |
|                                                | FS3          | IN   | Logic input frequency select bit. Input latched at power on.                                                                                                                                                                  |
| 35                                             | FS2          | IN   | Logic input frequency select bit. Input latched at power on.                                                                                                                                                                  |
|                                                | 24_48MHz     | OUT  | 3.3V 24 or 48MHz output.                                                                                                                                                                                                      |
| 38                                             | SDRAM_F      | OUT  | 3.3V free running 100MHz SDRAM not affected by I <sup>2</sup> C                                                                                                                                                               |
| 48, 47, 46, 44, 43, 42, 40, 39, 31, 30, 27, 26 | SDRAM (11:0) | OUT  | 3.3V output running 100MHz. All SDRAM outputs can be turned off through I <sup>2</sup> C.                                                                                                                                     |
| 50                                             | GNDL         | PWR  | Ground for 2.5V power supply for CPU & APIC.                                                                                                                                                                                  |
| 51, 52                                         | CPUCLK (1:0) | OUT  | 2.5V Host bus clock output. Output frequency derived from FS pins.                                                                                                                                                            |
| 53, 55                                         | VDDL         | PWR  | 2.5V power supply for CPU, IOAPIC.                                                                                                                                                                                            |
| 54                                             | IOAPIC       | OUT  | 2.5V clock outputs running at 16.67MHz.                                                                                                                                                                                       |
| 56                                             | FS4          | IN   | Logic input frequency select bit. Input latched at power on.                                                                                                                                                                  |
|                                                | REF0         | OUT  | 3.3V, 14.318MHz reference clock output.                                                                                                                                                                                       |



**Group Timing Relationship Table<sup>1</sup>**

| Group         | CPU 66MHz<br>SDRAM 100MHz |           | CPU 100MHz<br>SDRAM 100MHz |           | CPU 133MHz<br>SDRAM 100MHz |           | CPU 133MHz<br>SDRAM 133MHz |           |
|---------------|---------------------------|-----------|----------------------------|-----------|----------------------------|-----------|----------------------------|-----------|
|               | Offset                    | Tolerance | Offset                     | Tolerance | Offset                     | Tolerance | Offset                     | Tolerance |
| CPU to SDRAM  | 2.5ns                     | 500ps     | 5.0ns                      | 500ps     | 0.0ns                      | 500ps     | 3.75ns                     | 500ps     |
| CPU to 3V66   | 7.5ns                     | 500ps     | 5.0ns                      | 500ps     | 0.0ns                      | 500ps     | 0.0ns                      | 500ps     |
| SDRAM to 3V66 | 0.0ns                     | 500ps     | 0.0ns                      | 500ps     | 0.0ns                      | 500ps     | 3.75ns                     | 500ps     |
| 3V66 to PCI   | 1.5-3.5ns                 | 500ps     | 1.5-3.5ns                  | 500ps     | 1.5-3.5ns                  | 500ps     | 1.5 -3.5ns                 | 500ps     |
| PCI to PCI    | 0.0ns                     | 1.0ns     | 0.0ns                      | 1.0ns     | 0.0ns                      | 1.0ns     | 0.0ns                      | 1.0ns     |
| USB & DOT     | Asynch                    | N/A       | Asynch                     | N/A       | Asynch                     | N/A       | Asynch                     | N/A       |

**Byte 0: Functionality and frequency select register (Default=0)**  
(1 = enable, 0 = disable)

| Bit             | Description                                                                                         |       |       |       |       |                |              |             |        |               |                        | PWD             |
|-----------------|-----------------------------------------------------------------------------------------------------|-------|-------|-------|-------|----------------|--------------|-------------|--------|---------------|------------------------|-----------------|
| Bit<br>(2, 7:4) | Bit 2                                                                                               | Bit 7 | Bit 6 | Bit 5 | Bit 4 | CPUCCLK<br>MHz | SDRAM<br>MHz | 3V66<br>MHz | PCICLK | IOAPIC<br>MHz | Spread Percentage      | 00001<br>Note 1 |
|                 | FS4                                                                                                 | FS3   | FS2   | FS1   | FS0   |                |              |             |        |               |                        |                 |
|                 | 0                                                                                                   | 0     | 0     | 0     | 0     | 66.67          | 100.01       | 66.67       | 33.34  | 16.67         | 0 to -0.5% Down Spread |                 |
|                 | 0                                                                                                   | 1     | 0     | 0     | 0     | 100.00         | 100.00       | 66.67       | 33.33  | 16.67         | 0 to -0.5% Down Spread |                 |
|                 | 1                                                                                                   | 0     | 0     | 0     | 0     | 133.33         | 133.33       | 66.67       | 33.33  | 16.67         | 0 to -0.5% Down Spread |                 |
|                 | 1                                                                                                   | 1     | 0     | 0     | 0     | 133.33         | 100.00       | 66.67       | 33.33  | 16.67         | 0 to -0.5% Down Spread |                 |
| Bit 3           | 0-Frequency is selected by hardware select, latched inputs<br>1- Frequency is selected by Bit 2,7:4 |       |       |       |       |                |              |             |        |               |                        | 0               |
| Bit 1           | 0- Normal<br>1- Spread spectrum enable                                                              |       |       |       |       |                |              |             |        |               |                        | 1               |
| Bit 0           | 0- Running<br>1- Tristate all outputs                                                               |       |       |       |       |                |              |             |        |               |                        | 0               |

**Notes:**

- Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
- The I<sup>2</sup>C readback for Bit 2, 7:4 indicate the revision code.



**Byte 1: Control Register**  
(1 = enable, 0 = disable)

| Bit   | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | -    | X   | FS3#        |
| Bit 6 | -    | X   | FS0#        |
| Bit 5 | -    | X   | FS2#        |
| Bit 4 | 35   | 0   | 24_48MHz #  |
| Bit 3 | -    | 1   | (Reserved)  |
| Bit 2 | 34   | 1   | 48MHz       |
| Bit 1 | -    | 1   | (Reserved)  |
| Bit 0 | 38   | 1   | SDRAM_F     |

**Byte 2: Control Register**  
(1 = enable, 0 = disable)

| Bit   | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | 39   | 1   | SDRAM7      |
| Bit 6 | 40   | 1   | SDRAM6      |
| Bit 5 | 42   | 1   | SDRAM5      |
| Bit 4 | 43   | 1   | SDRAM4      |
| Bit 3 | 44   | 1   | SDRAM3      |
| Bit 2 | 46   | 1   | SDRAM2      |
| Bit 1 | 47   | 1   | SDRAM1      |
| Bit 0 | 48   | 1   | SDRAM0      |

**Byte 3: Control Register**  
(1 = enable, 0 = disable)

| Bit   | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | 20   | 1   | PCICLK7     |
| Bit 6 | 19   | 1   | PCICLK6     |
| Bit 5 | 17   | 1   | PCICLK5     |
| Bit 4 | 16   | 1   | PCICLK4     |
| Bit 3 | 15   | 1   | PCICLK3     |
| Bit 2 | 13   | 1   | PCICLK2     |
| Bit 1 | 12   | 1   | PCICLK1     |
| Bit 0 | 11   | 1   | PCICLK0     |

**Byte 4: Control Register**  
(1 = enable, 0 = disable)

| Bit   | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | 8    | 1   | 3V66_2      |
| Bit 6 | 6    | 1   | 3V66_0      |
| Bit 5 | 7    | 1   | 3V66_1      |
| Bit 4 | -    | X   | FS4#        |
| Bit 3 | 54   | 1   | IOAPIC      |
| Bit 2 | -    | X   | FS1#        |
| Bit 1 | 51   | 1   | CPUCLK1     |
| Bit 0 | 52   | 1   | CPUCLK0     |

**Byte 5: Control Register**  
(1 = enable, 0 = disable)

| Bit   | Pin# | PWD | Description |
|-------|------|-----|-------------|
| Bit 7 | -    | 1   | (Reserved)  |
| Bit 6 | -    | 1   | (Reserved)  |
| Bit 5 | -    | 1   | (Reserved)  |
| Bit 4 | -    | X   | 24_48MHz#   |
| Bit 3 | 26   | 1   | SDRAM11     |
| Bit 2 | 27   | 1   | SDRAM10     |
| Bit 1 | 30   | 1   | SDRAM9      |
| Bit 0 | 31   | 1   | SDRAM8      |

**Byte 6: Peripheral , Active/Inactive Register**  
(1= enable, 0 = disable)

| Bit  | Pin# | PWD | Description     |
|------|------|-----|-----------------|
| Bit7 | -    | 0   | Reserved (Note) |
| Bit6 | -    | 0   | Reserved (Note) |
| Bit5 | -    | 0   | Reserved (Note) |
| Bit4 | -    | 0   | Reserved (Note) |
| Bit3 | -    | 0   | Reserved (Note) |
| Bit2 | -    | 1   | Reserved (Note) |
| Bit1 | -    | 1   | Reserved (Note) |
| Bit0 | -    | 0   | Reserved (Note) |

**Note: Don't write into this register, writing into this register can cause malfunction**

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default



## Absolute Maximum Ratings

|                               |                                |
|-------------------------------|--------------------------------|
| Core Supply Voltage           | 4.6 V                          |
| I/O Supply Voltage            | 3.6V                           |
| Logic Inputs                  | GND –0.5 V to $V_{DD} + 0.5$ V |
| Ambient Operating Temperature | 0°C to +70°C                   |
| Storage Temperature           | –65°C to +150°C                |
| Case Temperature              | 115°C                          |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input / Supply / Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3$  V +/-5%,  $V_{DDL} = 2.5$  V +/-5% (unless otherwise stated)

| PARAMETER                                | SYMBOL             | CONDITIONS                                       | MIN      | TYP   | MAX            | UNITS         |
|------------------------------------------|--------------------|--------------------------------------------------|----------|-------|----------------|---------------|
| Input High Voltage<br>(Latched Inputs)   | $V_{IH}$           | $V_{DD} \leq 2.5$ V                              | 0.9      | 0.75  | $V_{DD} + 0.3$ | V             |
|                                          |                    | $V_{DD} = 3.15 - 3.45$ V                         | 1.15     | 0.85  |                |               |
| Input Low Voltage<br>(Latched Inputs)    | $V_{IL}$           | $V_{DD} \leq 2.5$ V                              | $V_{SS}$ | 0.72  | 0.60           | V             |
|                                          |                    | $V_{DD} = 3.15 - 3.45$ V                         | - 0.3    | 0.82  | 0.65           |               |
| Input High Voltage<br>(Real-Time Inputs) | $V_{IH}$           | $V_{DD} \leq 2.5$ V                              | 1.4      | 1.05  | $V_{DD} + 0.3$ | V             |
|                                          |                    | $V_{DD} = 3.15 - 3.45$ V                         | 2        | 1.45  |                |               |
| Input Low Voltage<br>(Real Time Inputs)  | $V_{IL}$           | $V_{DD} \leq 2.5$ V                              | $V_{SS}$ | 0.95  | 0.60           | V             |
|                                          |                    | $V_{DD} = 3.15 - 3.45$ V                         | - 0.3    | 1.35  | 0.80           |               |
| $V_{DD}3.3$ Supply Power <sup>2</sup>    | $I_{RAMP}$         | $V_{DD} = 0$ to 2.0 V                            | 50       |       |                | $\mu\text{s}$ |
| Input High Current                       | $I_{IH}$           | $V_{IN} = V_{DD}$                                | -5       |       | 5              | mA            |
| Input Low Current                        | $I_{IL1}$          | $V_{IN} = 0$ V; Inputs with no pull-up resistors | -5       |       |                | mA            |
| Input Low Current                        | $I_{IL2}$          | $V_{IN} = 0$ V; Inputs with pull-up resistors    | -200     |       |                | mA            |
| Operating Supply Current                 | $I_{DD3.3OP}$      | Cl = max cap loads; Select @ 66MHz               |          | 350   | 400            | mA            |
|                                          | $I_{DDL2.5OP}$     | Cl = max cap loads; Select @ 66MHz               |          | 13    | 20             |               |
| Power Down Current                       | $I_{DD3.3PD}$      | Cl = 0 pF; With Input to Vdd or Gnd              |          | 275   | 600            | $\mu\text{A}$ |
| Input frequency                          | $F_i$              | $V_{DD} = 3.3$ V                                 |          | 14.32 |                | MHz           |
| Pin Inductance                           | $L_{pin}$          |                                                  |          |       | 7              | nH            |
| Input Capacitance <sup>1</sup>           | $C_{IN}$           | Logic Inputs                                     |          |       | 5              | pF            |
|                                          | $C_{out}$          | Output pin capacitance                           |          |       | 6              | pF            |
|                                          | $C_{INX}$          | X1 & X2 pins                                     | 27       |       | 45             | pF            |
| Transition Time <sup>1</sup>             | $T_{Trans}$        | To 1st crossing of target Freq.                  |          |       | 3              | ms            |
| Settling Time <sup>1</sup>               | $T_S$              | From 1st crossing to 1% target Freq.             |          |       | 3              | ms            |
| Clk Stabilization <sup>1</sup>           | $T_{Stab}$         | From $V_{DD} = 3.3$ V to 1% target Freq.         |          |       | 3              | ms            |
| Delay <sup>1</sup>                       | $T_{PZH}, T_{PZL}$ | output enable delay(all outputs)                 | 1        |       | 10             | ns            |
|                                          | $T_{PHZ}, T_{PLZ}$ | output disable delay(all outputs)                | 1        |       | 10             | ns            |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>2</sup>When 2.5V and PD# pins are high before or simultaneous with  $V_{DD}3.3$  reaching 2V.



## Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20 \text{ pF}$  (unless otherwise specified)

| PARAMETER                           | SYMBOL          | CONDITIONS                                          | MIN  | TYP | MAX | UNITS    |
|-------------------------------------|-----------------|-----------------------------------------------------|------|-----|-----|----------|
| Output Impedance <sup>1</sup>       | $R_{DSP2B}$     | $V_O = V_{DD}^*(0.5)$                               | 13.5 |     | 45  | $\Omega$ |
| Output Impedance <sup>1</sup>       | $R_{DSN2B}$     | $V_O = V_{DD}^*(0.5)$                               | 13.5 |     | 45  | $\Omega$ |
| Output High Voltage                 | $V_{OH2B}$      | $I_{OH} = -1 \text{ mA}$                            | 2    |     |     | V        |
| Output Low Voltage                  | $V_{OL2B}$      | $I_{OL} = 1 \text{ mA}$                             |      |     | 0.4 | V        |
| Output High Current                 | $I_{OH2B}$      | $V_{OH @ MIN} = 1.0 \text{ V}$                      | -27  |     |     | mA       |
|                                     |                 | $V_{OH @ MAX} = 2.375 \text{ V}$                    |      |     | -27 |          |
| Output Low Current                  | $I_{OL2B}$      | $V_{OL @ MIN} = 1.2 \text{ V}$                      | 27   |     |     | mA       |
|                                     |                 | $V_{OL @ MAX} = 0.3 \text{ V}$                      |      |     | 30  |          |
| Rise Time <sup>1</sup>              | $t_{r2B}$       | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.0 \text{ V}$ | 0.4  | 0.8 | 1.6 | ns       |
| Fall Time <sup>1</sup>              | $t_{f2B}$       | $V_{OH} = 2.0 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ | 0.4  | 0.9 | 1.6 | ns       |
| Duty Cycle <sup>1</sup>             | $d_{t2B}$       | $V_T = 1.25 \text{ V}$ , 66, 100 MHz                | 45   | 51  | 55  | %        |
| Skew window <sup>1</sup>            | $t_{sk2B}$      | $V_T = 1.25 \text{ V}$                              |      | 98  | 175 | ps       |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{jcy-cyc2B}$ | $V_T = 1.25 \text{ V}$                              |      | 115 | 250 | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20 \text{ pF}$  (unless otherwise specified)

| PARAMETER                           | SYMBOL         | CONDITIONS                                          | MIN | TYP  | MAX  | UNITS    |
|-------------------------------------|----------------|-----------------------------------------------------|-----|------|------|----------|
| Output Impedance                    | $R_{DSP1}^1$   | $V_O = V_{DD}^*(0.5)$                               | 12  | 17   | 55   | $\Omega$ |
| Output Impedance                    | $R_{DSN1}^1$   | $V_O = V_{DD}^*(0.5)$                               | 12  | 18   | 55   | $\Omega$ |
| Output High Voltage                 | $V_{OH1}$      | $I_{OH} = -1 \text{ mA}$                            | 2.4 |      |      | V        |
| Output Low Voltage                  | $V_{OL1}$      | $I_{OL} = 1 \text{ mA}$                             |     |      | 0.55 | V        |
| Output High Current                 | $I_{OH1}$      | $V_{OH @ MIN} = 1.0 \text{ V}$                      | -33 | -108 |      | mA       |
|                                     |                | $V_{OH @ MAX} = 3.135 \text{ V}$                    |     | -9   | -33  |          |
| Output Low Current                  | $I_{OL1}$      | $V_{OL @ MIN} = 1.95 \text{ V}$                     | 30  | 95   |      | mA       |
|                                     |                | $V_{OL @ MAX} = 0.4 \text{ V}$                      |     | 29   | 38   |          |
| Rise Time <sup>1</sup>              | $t_{r1}$       | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ | 0.4 | 1    | 1.6  | ns       |
| Fall Time <sup>1</sup>              | $t_{f1}$       | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ | 0.4 | 1    | 1.6  | ns       |
| Duty Cycle <sup>1</sup>             | $d_{t1}$       | $V_T = 1.5 \text{ V}$                               | 45  | 50   | 55   | %        |
| Skew window <sup>1</sup>            | $t_{sk1}$      | $V_T = 1.5 \text{ V}$                               |     | 75   | 175  | ps       |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{jcy-cyc1}$ | $V_T = 1.5 \text{ V}$                               |     | 155  | 500  | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - IOAPIC

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20 \text{ pF}$  (unless otherwise specified)

| PARAMETER                           | SYMBOL                  | CONDITIONS                                          | MIN | TYP  | MAX | UNITS    |
|-------------------------------------|-------------------------|-----------------------------------------------------|-----|------|-----|----------|
| Output Impedance <sup>1</sup>       | $R_{DSP4B}$             | $V_O = V_{DD}^*(0.5)$                               | 9   | 21.5 | 30  | $\Omega$ |
| Output Impedance <sup>1</sup>       | $R_{DSN4B}$             | $V_O = V_{DD}^*(0.5)$                               | 9   | 23   | 30  | $\Omega$ |
| Output High Voltage                 | $V_{OH4B}$              | $I_{OH} = -1 \text{ mA}$                            | 2   |      |     | V        |
| Output Low Voltage                  | $V_{OL4B}$              | $I_{OL} = 1 \text{ mA}$                             |     |      | 0.4 | V        |
| Output High Current                 | $I_{OH4B}$              | $V_{OH @ MIN} = 1.0 \text{ V}$                      | -27 | -68  |     | mA       |
|                                     |                         | $V_{OH @ MAX} = 2.375 \text{ V}$                    |     | -9   | -27 |          |
| Output Low Current                  | $I_{OL4B}$              | $V_{OL @ MIN} = 1.2 \text{ V}$                      | 27  | 54   |     | mA       |
|                                     |                         | $V_{OL @ MAX} = 0.3 \text{ V}$                      |     | 11   | 30  |          |
| Rise Time <sup>1</sup>              | $t_{r4B}$               | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.0 \text{ V}$ | 0.4 | 1.2  | 1.6 | ns       |
| Fall Time <sup>1</sup>              | $t_{f4B}$               | $V_{OH} = 2.0 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.3  | 1.6 | ns       |
| Duty Cycle <sup>1</sup>             | $d_{t4B}$               | $V_T = 1.25 \text{ V}$                              | 45  | 50.6 | 55  | %        |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{j\text{cyc-cyc}4B}$ | $V_T = 1.25 \text{ V}$                              |     | 210  | 500 | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 20\text{-}30 \text{ pF}$  (unless otherwise specified)

| PARAMETER                           | SYMBOL                 | CONDITIONS                                          | MIN | TYP  | MAX | UNITS    |
|-------------------------------------|------------------------|-----------------------------------------------------|-----|------|-----|----------|
| Output Impedance <sup>1</sup>       | $R_{DSP3}$             | $V_O = V_{DD}^*(0.5)$                               | 10  | 14   | 24  | $\Omega$ |
| Output Impedance <sup>1</sup>       | $R_{DSN3}$             | $V_O = V_{DD}^*(0.5)$                               | 10  | 18   | 24  | $\Omega$ |
| Output High Voltage                 | $V_{OH3}$              | $I_{OH} = -1 \text{ mA}$                            | 2.4 |      |     | V        |
| Output Low Voltage                  | $V_{OL3}$              | $I_{OL} = 1 \text{ mA}$                             |     |      | 0.4 | V        |
| Output High Current                 | $I_{OH3}$              | $V_{OH @ MIN} = 2.0 \text{ V}$                      | -54 | -92  |     | mA       |
|                                     |                        | $V_{OH @ MAX} = 3.135 \text{ V}$                    |     | -16  | -46 |          |
| Output Low Current                  | $I_{OL3}$              | $V_{OL @ MIN} = 1.0 \text{ V}$                      | 54  | 68   |     | mA       |
|                                     |                        | $V_{OL @ MAX} = 0.4 \text{ V}$                      |     | 29   | 53  |          |
| Rise Time <sup>1</sup>              | $t_{r3}$               | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ | 0.4 | 1    | 1.6 | ns       |
| Fall Time <sup>1</sup>              | $t_{f3}$               | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.5  | 1.6 | ns       |
| Duty Cycle <sup>1</sup>             | $d_{t3}$               | $V_T = 1.5 \text{ V}$                               | 45  | 52.5 | 55  | %        |
| Skew window <sup>1</sup>            | $t_{sk3}$              | $V_T = 1.5 \text{ V}$                               |     | 58   | 250 | ps       |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{j\text{cyc-cyc}3}$ | $V_T = 1.5 \text{ V}$ , 66, 100 MHz                 |     | 170  | 250 | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 10\text{-}30\text{ pF}$  (unless otherwise specified)

| PARAMETER                           | SYMBOL         | CONDITIONS                                        | MIN | TYP  | MAX  | UNITS    |
|-------------------------------------|----------------|---------------------------------------------------|-----|------|------|----------|
| Output Impedance <sup>1</sup>       | $R_{DSP1}$     | $V_O = V_{DD} \cdot (0.5)$                        | 12  | 14   | 55   | $\Omega$ |
| Output Impedance <sup>1</sup>       | $R_{DSN1}$     | $V_O = V_{DD} \cdot (0.5)$                        | 12  | 18   | 55   | $\Omega$ |
| Output High Voltage                 | $V_{OH1}$      | $I_{OH} = -1\text{ mA}$                           | 2.4 |      |      | V        |
| Output Low Voltage                  | $V_{OL1}$      | $I_{OL} = 1\text{ mA}$                            |     |      | 0.55 | V        |
| Output High Current                 | $I_{OH1}$      | $V_{OH @ MIN} = 1.0\text{ V}$                     | -33 | -106 |      | mA       |
|                                     |                | $V_{OH @ MAX} = 3.135\text{ V}$                   |     | -14  | -33  |          |
| Output Low Current                  | $I_{OL1}$      | $V_{OL @ MIN} = 1.95\text{ V}$                    | 30  | 94   |      | mA       |
|                                     |                | $V_{OL @ MAX} = 0.4\text{ V}$                     |     | 29   | 38   |          |
| Rise Time <sup>1</sup>              | $t_{r1}$       | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$ | 0.5 | 1.5  | 2    | ns       |
| Fall Time <sup>1</sup>              | $t_{f1}$       | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$ | 0.5 | 1.6  | 2    | ns       |
| Duty Cycle <sup>1</sup>             | $d_{t1}$       | $V_T = 1.5\text{ V}$                              | 45  | 51.9 | 55   | %        |
| Skew window <sup>1</sup>            | $t_{sk1}$      | $V_T = 1.5\text{ V}$                              |     | 328  | 500  | ps       |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{jcy-cyc1}$ | $V_T = 1.5\text{ V}$                              |     | 170  | 500  | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - REF, 24,48MHz

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

| PARAMETER                           | SYMBOL         | CONDITIONS                                        | MIN | TYP  | MAX  | UNITS    |
|-------------------------------------|----------------|---------------------------------------------------|-----|------|------|----------|
| Output Impedance <sup>1</sup>       | $R_{DSP5}$     | $V_O = V_{DD} \cdot (0.5)$                        | 12  | 17   | 55   | $\Omega$ |
| Output Impedance <sup>1</sup>       | $R_{DSN5}$     | $V_O = V_{DD} \cdot (0.5)$                        | 12  | 18   | 55   | $\Omega$ |
| Output High Voltage                 | $V_{OH15}$     | $I_{OH} = -1\text{ mA}$                           | 2.4 |      |      | V        |
| Output Low Voltage                  | $V_{OL5}$      | $I_{OL} = 1\text{ mA}$                            |     |      | 0.55 | V        |
| Output High Current                 | $I_{OH5}$      | $V_{OH @ MIN} = 1.0\text{ V}$                     | -33 | -108 |      | mA       |
|                                     |                | $V_{OH @ MAX} = 3.135\text{ V}$                   |     | -9   | -33  |          |
| Output Low Current                  | $I_{OL5}$      | $V_{OL @ MIN} = 1.95\text{ V}$                    | 30  | 95   |      | mA       |
|                                     |                | $V_{OL @ MAX} = 0.4\text{ V}$                     |     | 29   | 38   |          |
| Rise Time <sup>1</sup>              | $t_{r5}$       | $V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$ | 0.4 | 1.2  | 4    | ns       |
| Fall Time <sup>1</sup>              | $t_{f5}$       | $V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$ | 0.4 | 1.2  | 4    | ns       |
| Duty Cycle <sup>1</sup>             | $d_{t5}$       | $V_T = 1.5\text{ V}$                              | 45  | 52   | 55   | %        |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{jcy-cyc5}$ | $V_T = 1.5\text{ V}$ , Fixed clocks               |     | 310  | 500  | ps       |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{jcy-cyc5}$ | $V_T = 1.5\text{ V}$ , Ref clocks                 |     | 720  | 1000 | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming.  
For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte **one at a time**.
- Controller (host) sends a Stop bit

| How to Write:                |                      |
|------------------------------|----------------------|
| Controller (Host)            | ICS (Slave/Receiver) |
| Start Bit                    |                      |
| Address<br>D2 <sub>(H)</sub> |                      |
|                              | <b>ACK</b>           |
| Dummy Command Code           |                      |
|                              | <b>ACK</b>           |
| Dummy Byte Count             |                      |
|                              | <b>ACK</b>           |
| Byte 0                       |                      |
|                              | <b>ACK</b>           |
| Byte 1                       |                      |
|                              | <b>ACK</b>           |
| Byte 2                       |                      |
|                              | <b>ACK</b>           |
| Byte 3                       |                      |
|                              | <b>ACK</b>           |
| Byte 4                       |                      |
|                              | <b>ACK</b>           |
| Byte 5                       |                      |
|                              | <b>ACK</b>           |
| Stop Bit                     |                      |

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read:                 |                      |
|------------------------------|----------------------|
| Controller (Host)            | ICS (Slave/Receiver) |
| Start Bit                    |                      |
| Address<br>D3 <sub>(H)</sub> |                      |
|                              | <b>ACK</b>           |
|                              | <b>Byte Count</b>    |
| ACK                          |                      |
|                              | <b>Byte 0</b>        |
| ACK                          |                      |
|                              | <b>Byte 1</b>        |
| ACK                          |                      |
|                              | <b>Byte 2</b>        |
| ACK                          |                      |
|                              | <b>Byte 3</b>        |
| ACK                          |                      |
|                              | <b>Byte 4</b>        |
| ACK                          |                      |
|                              | <b>Byte 5</b>        |
| ACK                          |                      |
| Stop Bit                     |                      |

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only **"Block-Writes"** from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

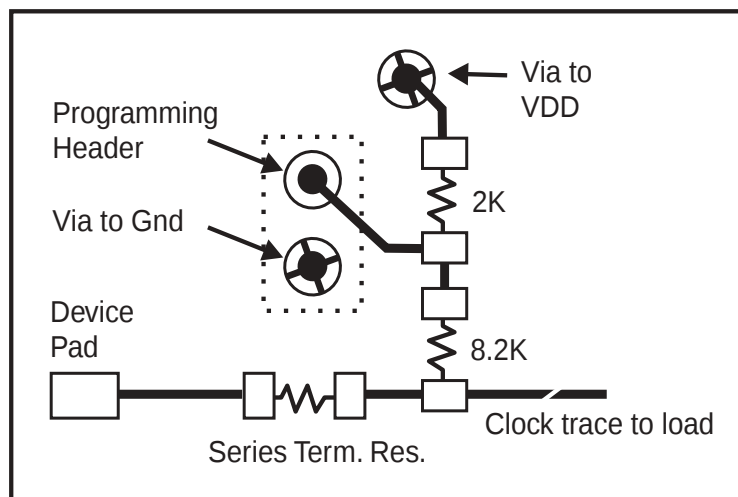


## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

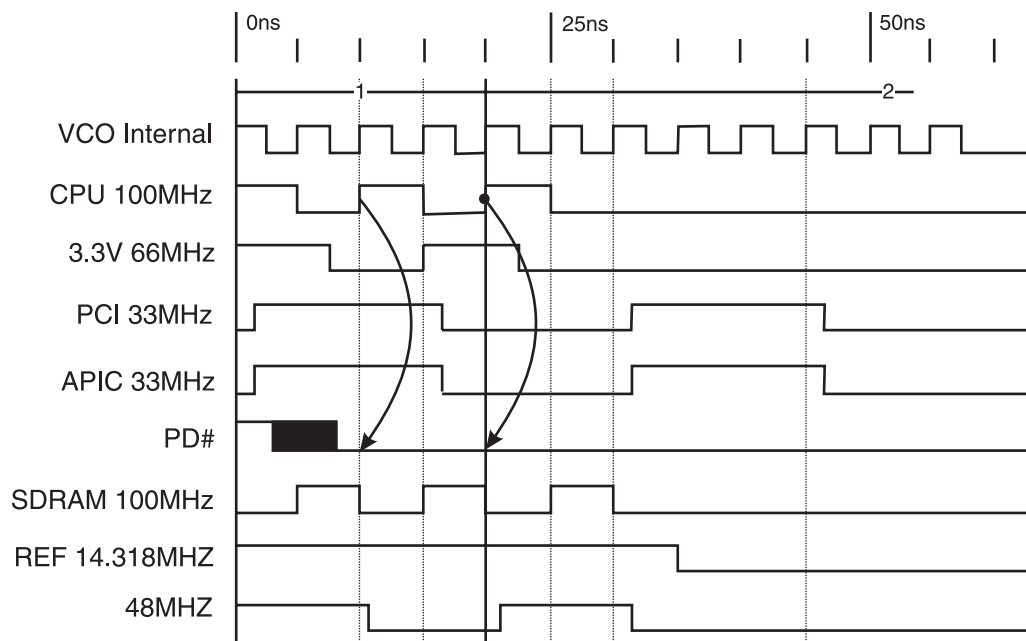
Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.



**Fig. 1**

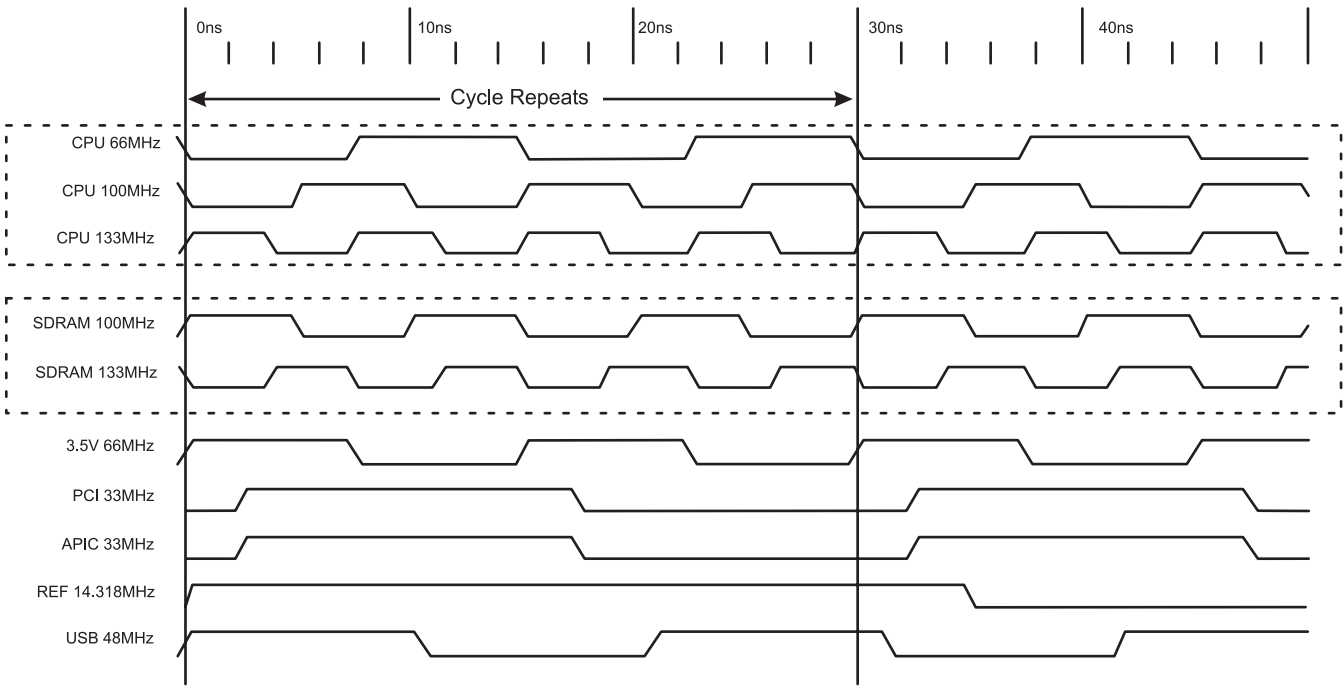


## Power Down Waveform

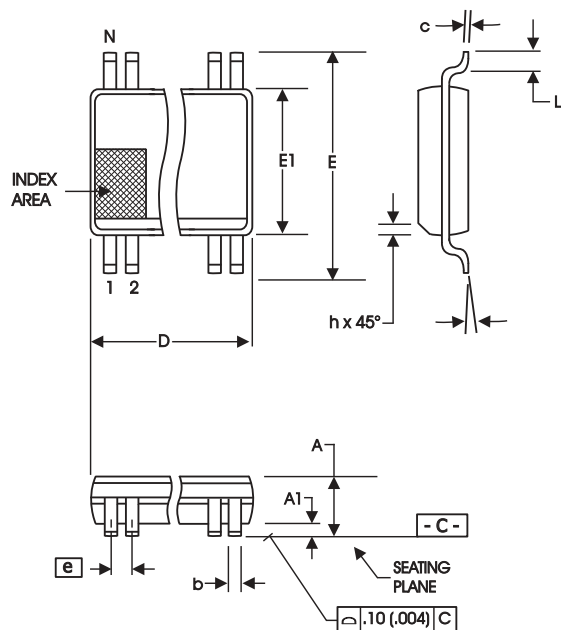


### Note

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low transition.
2. Power-up latency <3ms.
3. Waveform shown for 100MHz



Group Offset Waveforms



| SYMBOL   | In Millimeters    |       | In Inches         |       |
|----------|-------------------|-------|-------------------|-------|
|          | COMMON DIMENSIONS |       | COMMON DIMENSIONS |       |
|          | MIN               | MAX   | MIN               | MAX   |
| A        | 2.41              | 2.80  | .095              | .110  |
| A1       | 0.20              | 0.40  | .008              | .016  |
| b        | 0.20              | 0.34  | .008              | .0135 |
| c        | 0.13              | 0.25  | .005              | .010  |
| D        | SEE VARIATIONS    |       | SEE VARIATIONS    |       |
| E        | 10.03             | 10.68 | .395              | .420  |
| E1       | 7.40              | 7.60  | .291              | .299  |
| e        | 0.635 BASIC       |       | 0.025 BASIC       |       |
| h        | 0.38              | 0.64  | .015              | .025  |
| L        | 0.50              | 1.02  | .020              | .040  |
| N        | SEE VARIATIONS    |       | SEE VARIATIONS    |       |
| $\alpha$ | 0°                | 8°    | 0°                | 8°    |

## VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 56 | 18.31 | 18.55 | .720     | .730 |

Reference Doc.: JEDEC Publication 95, M O-118

10-0034

## Ordering Information

ICS9250yF-50-T

Example:

ICS XXXX y F - PPP - T

Designation for tape and reel packaging

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type  
F=SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type

Prefix

ICS, AV = Standard Device